

NCS2302

Headset Detection Interface with Send/End Detect

The NCS2302 is a compact and cost effective headset detection interface IC. It integrates several circuit blocks to detect the presence of a stereo headset with a microphone and whether the send/end button has been pressed. The NMOS transistor on the MIC pin mutes the signal when the headset is not present. The built in resistor divider provides the reference voltage for detecting the left audio channel. When L_DET and GND_DET are pulled low, the logic low output of the OR gate indicates the headset has been connected properly and the MIC pull-down is disabled. A comparator is integrated for detecting the send/end button press. The NCS2302 comes in a space-saving UQFN10 package (1.4 x 1.8 mm).

Features

- Wide Supply Voltage Ranges:
 - For Headset Detection Circuit: $V_{DD} = 1.6\text{ V to }2.5\text{ V}$
 - For S/E Comparator Circuit: $V_{DD2} = 1.6\text{ V to }2.8\text{ V}$
- Low Quiescent Supply Current: 17 μA typical
- Low Impedance MIC Pull-Down Reduces Pop & Click Noise:
 $R_{DS(ON)} = 0.45\ \Omega$ Typical
- Space Saving UQFN10 Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Cell Phones, Smartphones
- Tablets
- Notebooks



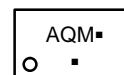
ON Semiconductor®

<http://onsemi.com>



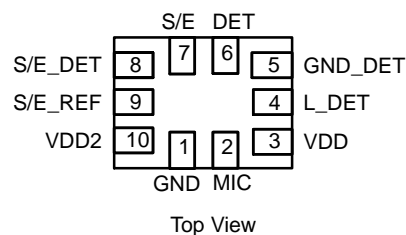
UQFN10
MU SUFFIX
CASE 488AT

MARKING DIAGRAM



AQ = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCS2302MUTAG	UQFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCS2302

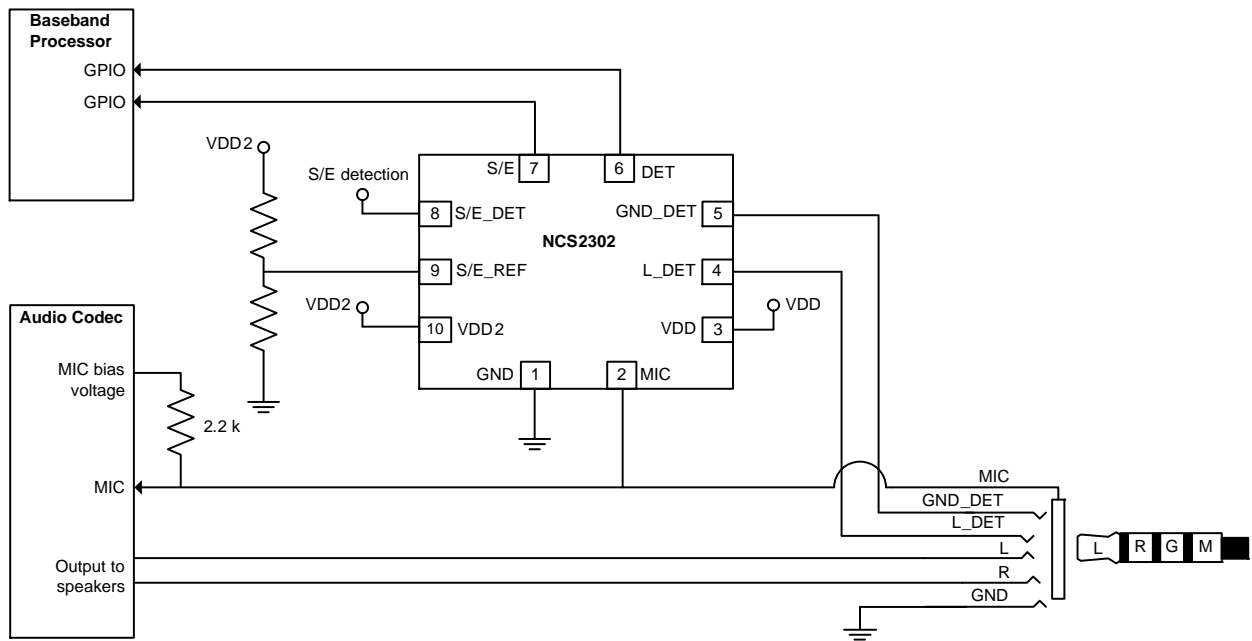


Figure 1. Simplified Application Schematic

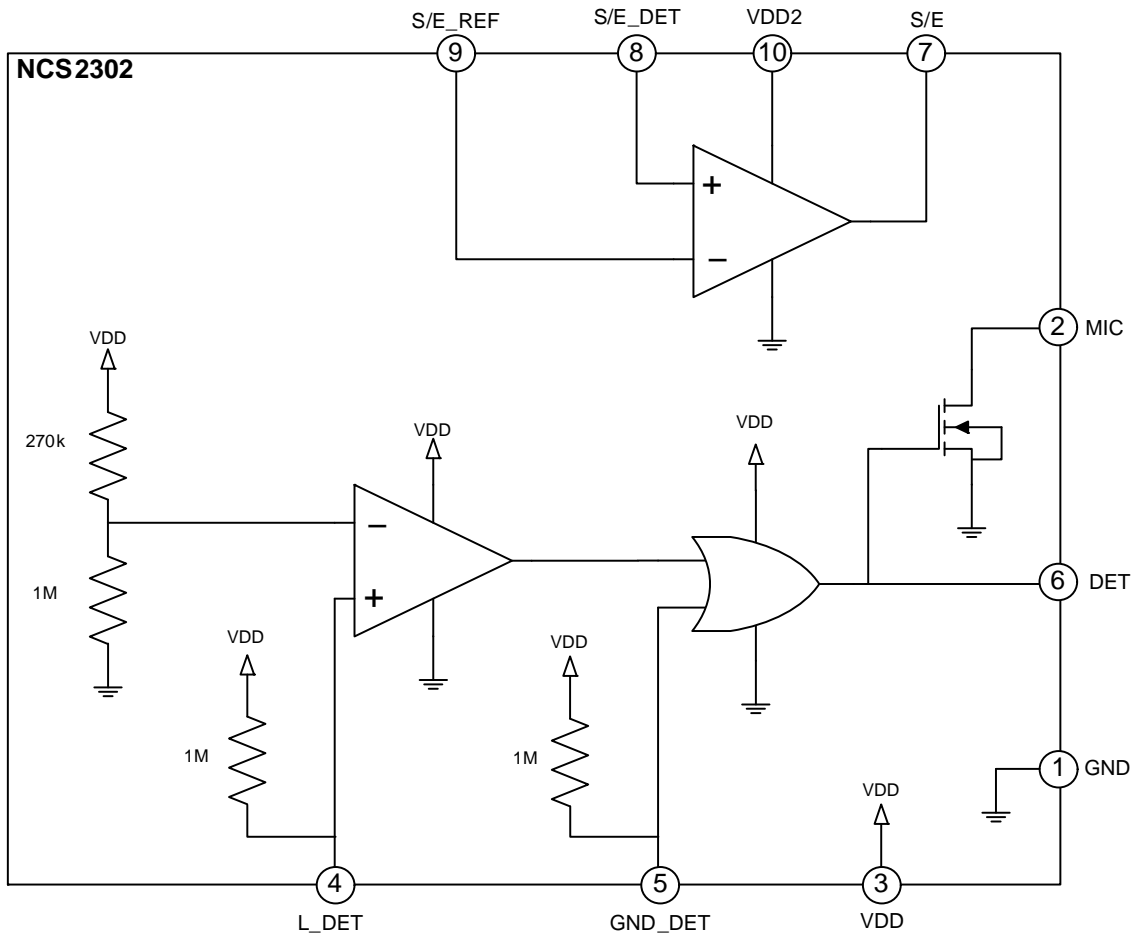


Figure 2. Block Diagram

NCS2302

Table 1. OUTPUT LOGIC

Inputs		Outputs		Headset
L_detect	GND_detect	DET	MIC	
0	0	0	1 (external pull-up)	Detected
0	1	1	0	Not Detected
1	0	1	0	
1	1	1	0	

Table 2. PIN DESCRIPTION

Pin	Name	Type	Description
1	GND	Power	Connects to system ground.
2	MIC	Output	The open drain MIC pin is connected to the audio jack MIC pin. The MIC pin will pull low when the headset is not connected. When the headset is detected, the internal pull-down is disabled and the external pull-up biases the microphone.
3	VDD	Power	Supply voltage pin for headset detection circuit. A bypass capacitor of 0.1 μ F is recommended as close as possible to this pin.
4	L_DET	Input	Connect to audio jack L_DET. This pin is pulled low when the headset is present.
5	GND_DET	Input	Connect to audio jack GND_DET. This pin is pulled low when the headset is present.
6	DET	Output	Indicates whether headset has been detected. Headset is detected when DET is low.
7	S/E	Output	Indicates whether send/end button press has been detected. Button press is detected when S/E is low.
8	S/E_DET	Input	Non-inverting input of the comparator detects whether the send/end button has been pressed.
9	S/E_REF	Input	Inverting input of the comparator sets a voltage reference with an external resistor divider
10	VDD2	Power	Supply voltage pin for S/E detection comparator. A bypass capacitor of 0.1 μ F is recommended as close as possible to this pin.

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage Range of Headset Detection Circuit	V_{DD}	0 to 2.75	V
Supply Voltage Range of S/E Detection Comparator	V_{DD2}	0 to 2.95	V
Input Pin Voltage Range (L_DET, GND_DET)	V_{IN}	-0.1 to $V_{DD} + 0.1$	V
Input Pin Voltage Range (S/E_REF, S/E_DET) (Note 4)	V_{IN}	-0.1 to $\min(V_{DD2} + 0.6, 3.3)$	V
MIC Output Pin Voltage Range	V_{MIC}	0 to 6.0	V
Max Current on MIC Pin	I_{MIC}	2	mA
Maximum Junction Temperature	$T_{J(max)}$	+125	$^{\circ}$ C
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}$ C
Latch-up Current (Note 2)	I_{LU}	800	mA
Moisture Sensitivity Level (Note 3)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Latch-up Current tested per JEDEC standard: JESD78
3. Moisture Sensitivity Level tested per IPC/JEDEC standard: J-STD-020A
4. The maximum voltage on the S/E_REF and S/E_DET pins must be the lesser of $V_{DD2} + 0.6$ and 3.3 V.

Table 4. RECOMMENDED OPERATING RANGES

Rating	Conditions	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	Headset Detection Circuit	V_{DD}	1.6	1.8	2.5	V
	S/E Detection Comparator	V_{DD2}	1.6		2.8	V
Input Voltage	L_DET, GND_DET	V_{IN}	0		V_{DD}	V
	S/E_DET, S/E_REF		0		V_{DD2}	V
Input Transition Rise or Fall Rate	GND_DET pin	$\Delta t / \Delta V$	0		10	ns/V
MIC Bias Voltage		V_{MIC}	0		2.95	V
Ambient Temperature		T_A	-40		85	°C
Junction Temperature		T_J	-40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS Typical values are referenced to $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$, $V_{DD2} = 2.1\text{ V}$, unless otherwise noted. Min/max values apply from $T_A = -40^\circ\text{C}$ to 85°C , unless otherwise noted. (Notes 5, 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
-----------	-----------------	--------	-----	-----	-----	-------

SUPPLY CHARACTERISTICS

Quiescent Supply Current	Headset Detection Circuit, $V_{GND_DET} = 1.8\text{ V}$, $V_{L_DET} = 1.8\text{ V}$	I_{DD}		7	8.5	μA
	S/E Detection Comparator, $V_{SE_REF} = 0\text{ V}$, $V_{SE_DET} = 2.1\text{ V}$	I_{DD2}		10	12.5	μA

INPUT CHARACTERISTICS OF L_DET

Voltage Input Low		V_{IL}			1.33	V
Voltage Input High		V_{IH}	1.5			V
Propagation Delay to DET	$C_{out} = 15\text{ pF}$, $GND_DET = 0\text{ V}$, $L_DET = 1.31\text{ V}$ to 1.52 V	t_{pLH} , t_{pHL}		45		ns
Low to High Propagation Delay to MIC	$C_{out} = 15\text{ pF}$, $GND_DET = 0\text{ V}$, $L_DET = 1.31\text{ V}$ to 1.52 V , $R_{PU} = 2.2\text{ k}\Omega$, MIC bias = 2.3 V	t_{pLH}		230		ns
High to Low Propagation Delay to MIC	$C_{out} = 15\text{ pF}$, $GND_DET = 0\text{ V}$, $L_DET = 1.31\text{ V}$ to 1.52 V , $R_{PU} = 2.2\text{ k}\Omega$, MIC bias = 2.3 V	t_{pHL}		30		ns
Low Voltage Input Bias Current	$V_{L_DET} = 0\text{ V}$	I_{IL}		1.8		μA
High Voltage Input Leakage	$V_{L_DET} = 1.8\text{ V}$	I_{IH}		2.4		nA
Input Capacitance	$f = 1\text{ MHz}$	C_{IN}		3		pF

INPUT CHARACTERISTICS OF GND_DET

Voltage Input Low		V_{IL}			0.63	V
Voltage Input High		V_{IH}	1.17			V
Low to High Propagation Delay to DET	$C_{out} = 15\text{ pF}$, $R_L = 1\text{ M}\Omega$, $L_detect = 0\text{ V}$, $GND_detect = 1.8$ to 0 V	t_{pLH}		30		ns
High to Low Propagation Delay to DET	$C_{out} = 15\text{ pF}$, $R_L = 1\text{ M}\Omega$, $L_detect = 0\text{ V}$, $GND_detect = 0$ to 1.8 V	t_{pHL}		16		ns
Low Voltage Input Bias Current	$V_{GND_detect} = 0\text{ V}$	I_{IL}		1.8		μA
High Voltage Input Leakage	$V_{GND_detect} = 1.8\text{ V}$	I_{IH}		2.7		nA
Input Capacitance	$f = 1\text{ MHz}$	C_{IN}		3		pF

5. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

NCS2302

Table 5. ELECTRICAL CHARACTERISTICS Typical values are referenced to $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$, $V_{DD2} = 2.1\text{ V}$, unless otherwise noted. Min/max values apply from $T_A = -40^\circ\text{C}$ to 85°C , unless otherwise noted. (Notes 5, 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
-----------	-----------------	--------	-----	-----	-----	-------

OUTPUT CHARACTERISTICS OF DET

Voltage Output Low	$I_{OH} = 0.1\text{ mA}$	V_{OL}			0.1	V
Voltage Output High	$I_{OH} = -0.1\text{ mA}$	V_{OH}	1.6			V
Rise Time	$C_{OUT} = 15\text{ pF}$, $R_L = 1\text{ M}\Omega$	t_{rise}		50		ns
Fall Time	$C_{OUT} = 15\text{ pF}$, $R_L = 1\text{ M}\Omega$	t_{fall}		28		ns

INPUT CHARACTERISTICS OF S/E_REF AND S/E_DET

Propagation Delay to S/E	$C_{out} = 15\text{ pF}$, $V_{CM} = \text{mid-supply}$, 100 mV overdrive	t_{pLH} , t_{pHL}		50		ns
Input Leakage	$V_{CM} = 0.9\text{ V}$	I_{IL}		150		pA
Input Capacitance	S/E_DET, $f = 1\text{ MHz}$	C_{IN}		3		pF
	S/E_REF, $f = 1\text{ MHz}$			11		

OUTPUT CHARACTERISTICS OF S/E

Voltage Output Low	$I_{OH} = 0.1\text{ mA}$	V_{OL}			0.1	V
Voltage Output High	$I_{OH} = -0.1\text{ mA}$	V_{OH}	1.9			V
Rise Time	$C_{OUT} = 15\text{ pF}$, $R_L = 1\text{ M}\Omega$	t_{rise}		30		ns
Fall Time	$C_{OUT} = 15\text{ pF}$, $R_L = 1\text{ M}\Omega$	t_{fall}		18		ns

CHARACTERISTICS OF MIC

Drain-Source On Resistance of NMOS	$I_{MIC} = 1\text{ mA}$	$R_{DS(ON)}$		0.45	1.2	Ω
------------------------------------	-------------------------	--------------	--	------	-----	----------

- Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- Performance guaranteed over the indicated operating temperature range by design and/or characterization.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

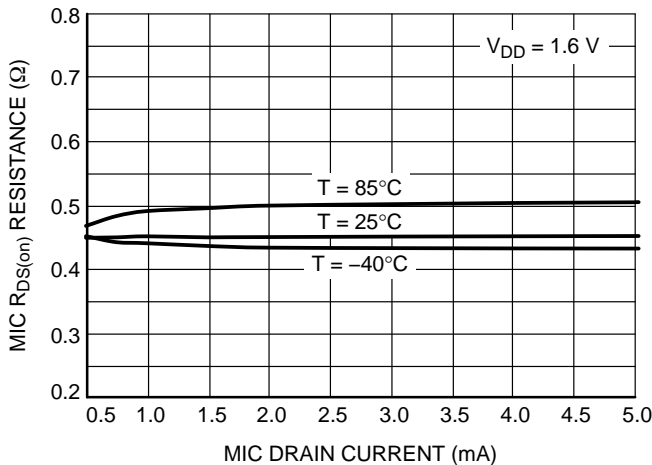


Figure 3. MIC On Resistance vs. Drain Current at $V_{DD} = 1.6\text{ V}$

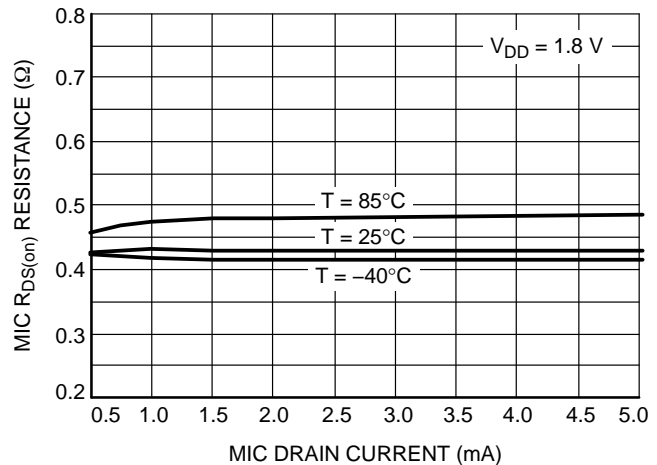


Figure 4. MIC On Resistance vs. Drain Current at $V_{DD} = 1.8\text{ V}$

TYPICAL CHARACTERISTICS

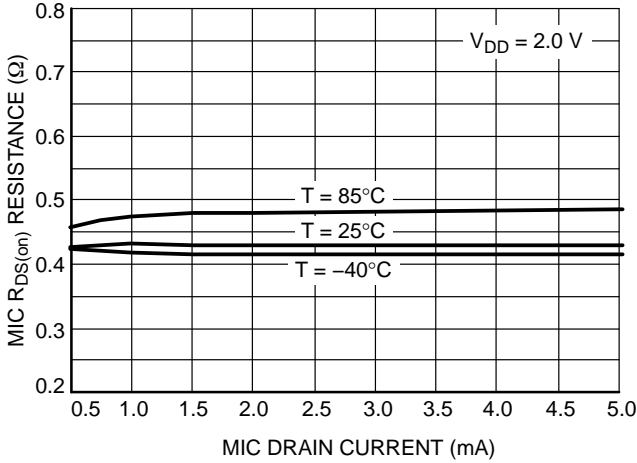


Figure 5. MIC On Resistance vs. Drain Current at $V_{DD} = 2.0$ V

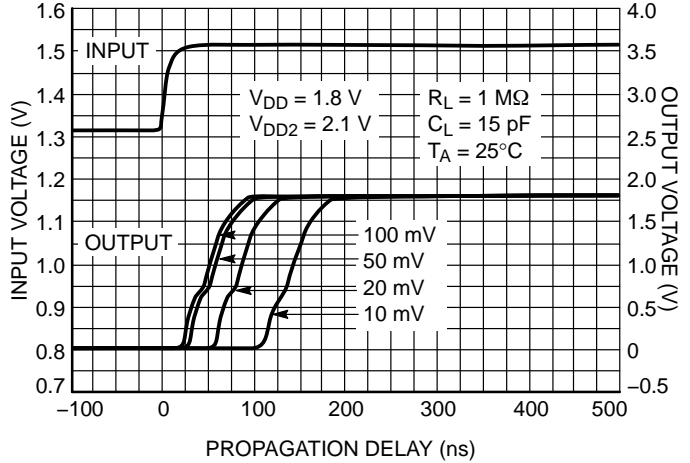


Figure 6. Low to High Propagation to DET with Changing Input Overdrive of L_DET

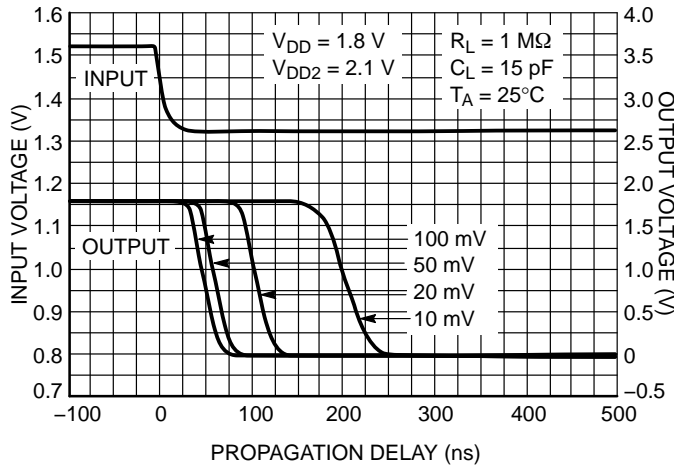


Figure 7. High to Low Propagation to DET with Changing Input Overdrive of L_DET

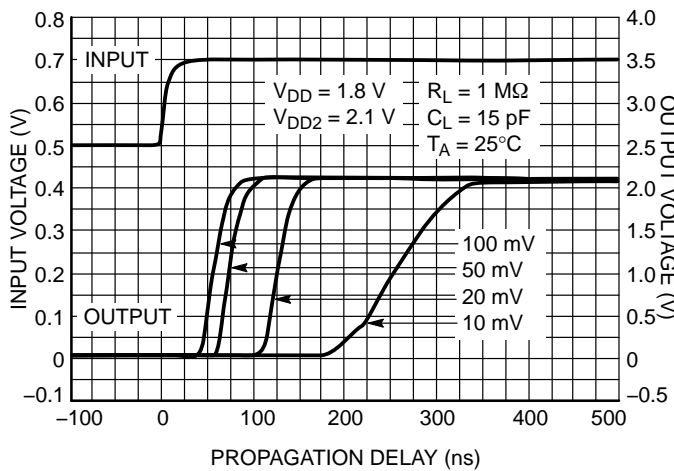


Figure 8. Low to High Propagation to SE with Changing Input Overdrive of SE_DET

TYPICAL CHARACTERISTICS

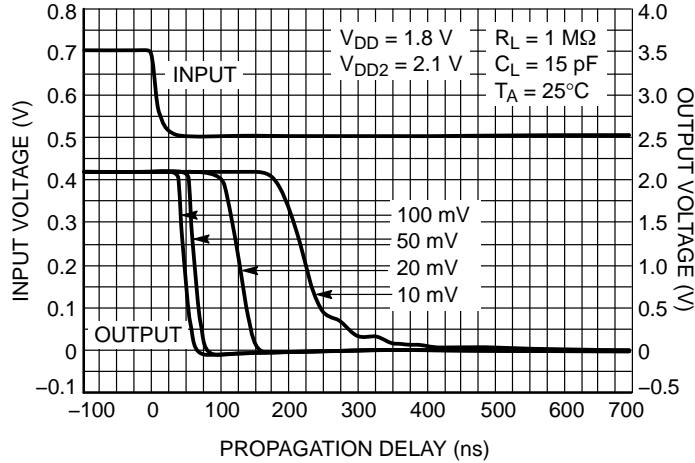


Figure 9. High to Low Propagation to SE with Changing Input Overdrive of SE_DET

APPLICATIONS INFORMATION

Supply Voltages

The NCS2302 works with a wide range of supply voltages. The main headset detection circuitry power supply can range from $V_{DD} = 1.6\text{ V}$ to 2.5 V . The send/end button press detection circuit can be powered from $V_{DD2} = 1.6$ to 2.8 V . V_{DD} should be powered up before V_{DD2} . The send/end detection comparator will not be functional unless V_{DD} and V_{DD2} are both applied. V_{DD2} can be connected to V_{DD} or to a separate supply voltage, such as the MIC bias voltage. Decoupling capacitors of $0.1\ \mu\text{F}$ should be placed as close as possible to each power supply pin. Since the NCS2302 has built in latch-up immunity up to 800 mA , series resistors are not recommended on V_{DD} or V_{DD2} .

Audio Jack Detection

The NCS2302 is designed to simplify the detection of a stereo audio connector with a microphone contact. When the headset is not connected, the internal pull-up resistors on L_DET and GND_DET pull those pins high. When the headset is connected to the switched audio jack, the headset ground and left audio channel trigger L_DET and GND_DET to logic low.

The NCS2302 can work with either the CTIA or OMTP standard. In order to support both standards simultaneously, a cross point switch and additional circuitry is necessary to detect and swap the ground and microphone pins.

Send/End Button Press Detection

A second integrated comparator allows the send/end signal to be compared with a reference voltage to detect whether the send/end button has been pressed.

MIC Pin Biasing

The typical application schematic in Figure 1 shows the recommended $2.2\text{ k}\Omega$ pull-up resistor to the MIC bias voltage. The MIC bias voltage can exceed V_{DD} and can go as high as 2.95 V . When the headset is not detected, the internal NMOS transistor is enabled to mute the MIC signal. In the typical application scenario with a $2.2\text{ k}\Omega$ pull-up to a 2.1 V MIC bias voltage, the MIC pin is pulled to 1 mV when the headset is not present. The internal NMOS transistor is optimized to sink up to 2 mA of current, allowing some flexibility in the selection of the pull-up resistor and MIC bias voltage.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

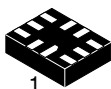
ON Semiconductor®



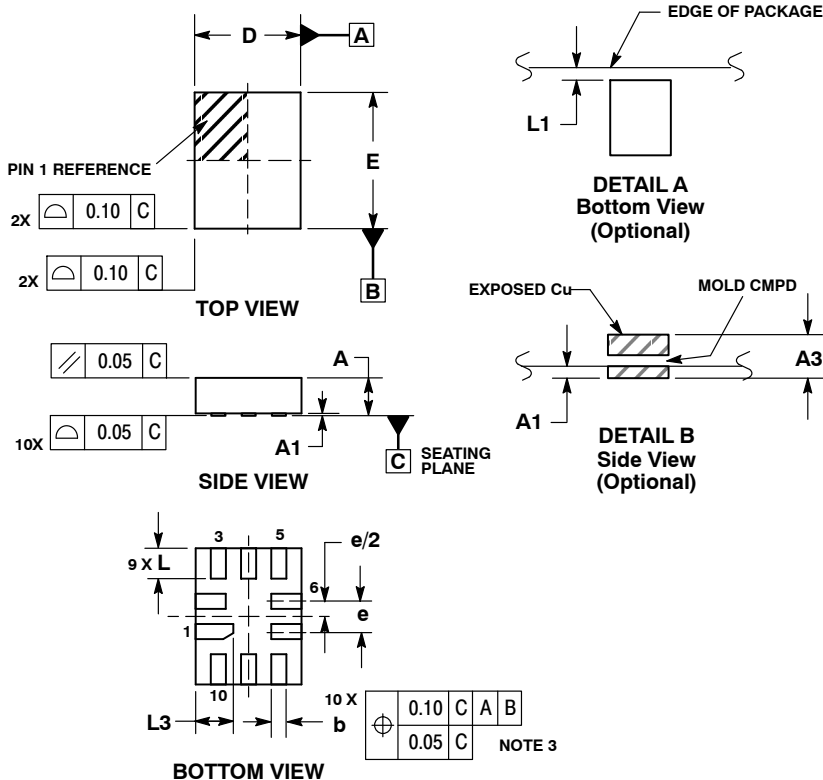
UQFN10 1.4x1.8, 0.4P

CASE 488AT-01
ISSUE A

DATE 01 AUG 2007

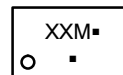


SCALE 5:1



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 - CONTROLLING DIMENSION: MILLIMETERS
 - DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 - COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

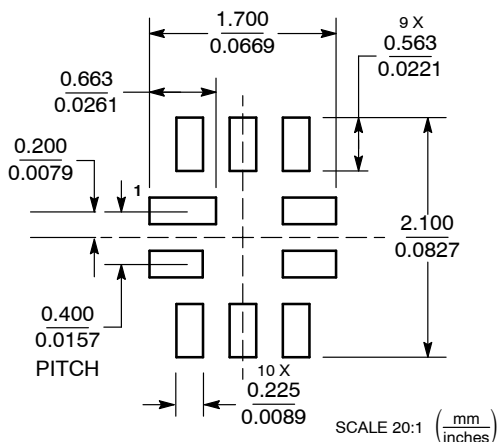
GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
 - M = Date Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

MOUNTING FOOTPRINT



DOCUMENT NUMBER:	98AON22493D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	10 PIN UQFN, 1.4 X 1.8, 0.4P	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

