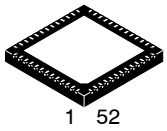
4 + 1 Phase Output Controller with SVID Interface for Computer CPU Applications

NCP81523, NCP81523R



QFN52 6x6, 0.4P
CASE 485BE

The NCP81523 is a dual rail, four plus one phase buck solution optimized for Intel's IMVP9.1 CPUs. The multi−phase rail control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing. This provides an ultra−fast initial response to dynamic load events and reduced system cost. The NCP81523 has an ultra−low offset current monitor amplifier with programmable offset compensation for high accuracy current monitoring.

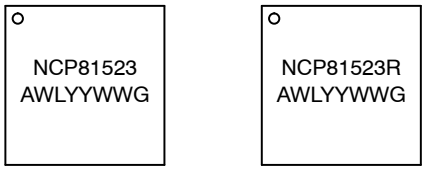
Features

- Vin Range 4.5 V to 21 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Digital Soft Start Ramp
- Adjustable Vboot
- High Impedance Differential Output Voltage Amplifier
- Dual VID Table Support to be Compatible with IMVP9.1
- Support High Current Extensions
- Dynamic Reference Injection
- Programmable Output Voltage Slew Rates
- Dynamic VID Feed−Forward
- Differential Current Sense Amplifiers for Each Phase
- Programmable Adaptive Voltage Positioning (AVP)
- Adjustable Switching Frequency Range
- Digitally Stabilized Switching Frequency
- UltraSonic Operation
- Supports Acoustic Noise Mitigation Function
- Support for VCCIN_AUX IMON Input
- PSYS Input Monitor (SVID address 0D)
- Meets Intel's IMVP9.1 Specifications
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- This is a Pb−Free Device

Typical Applications

- Desktop, Notebook and Ultra−book Computers

MARKING DIAGRAM



A	= Assembly Site Code
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81523MNTXG	QFN52 (Pb−Free)	2500 / Tape & Reel
NCP81523RMNTXG	QFN52 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

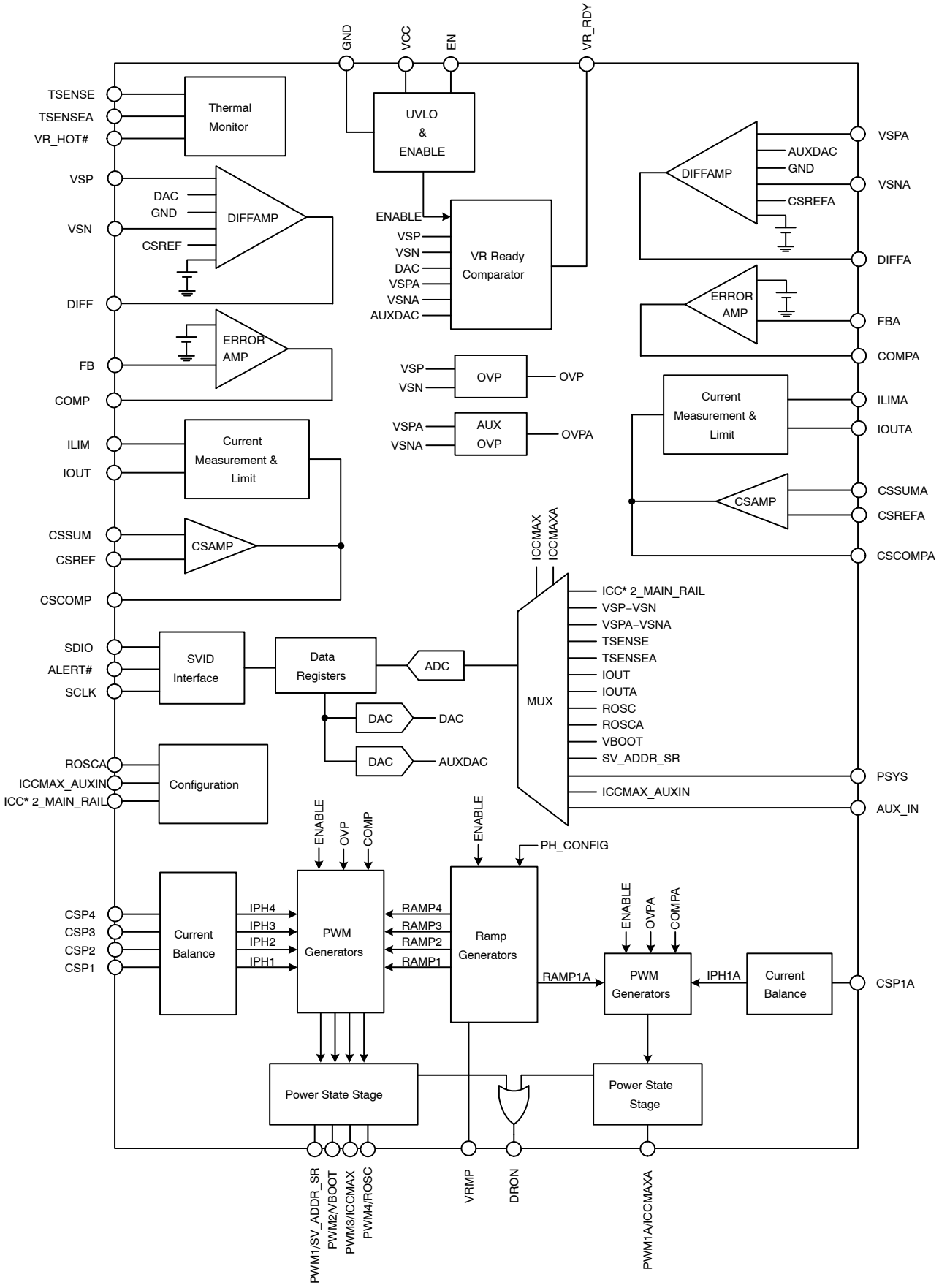


Figure 1. Internal Block Diagram

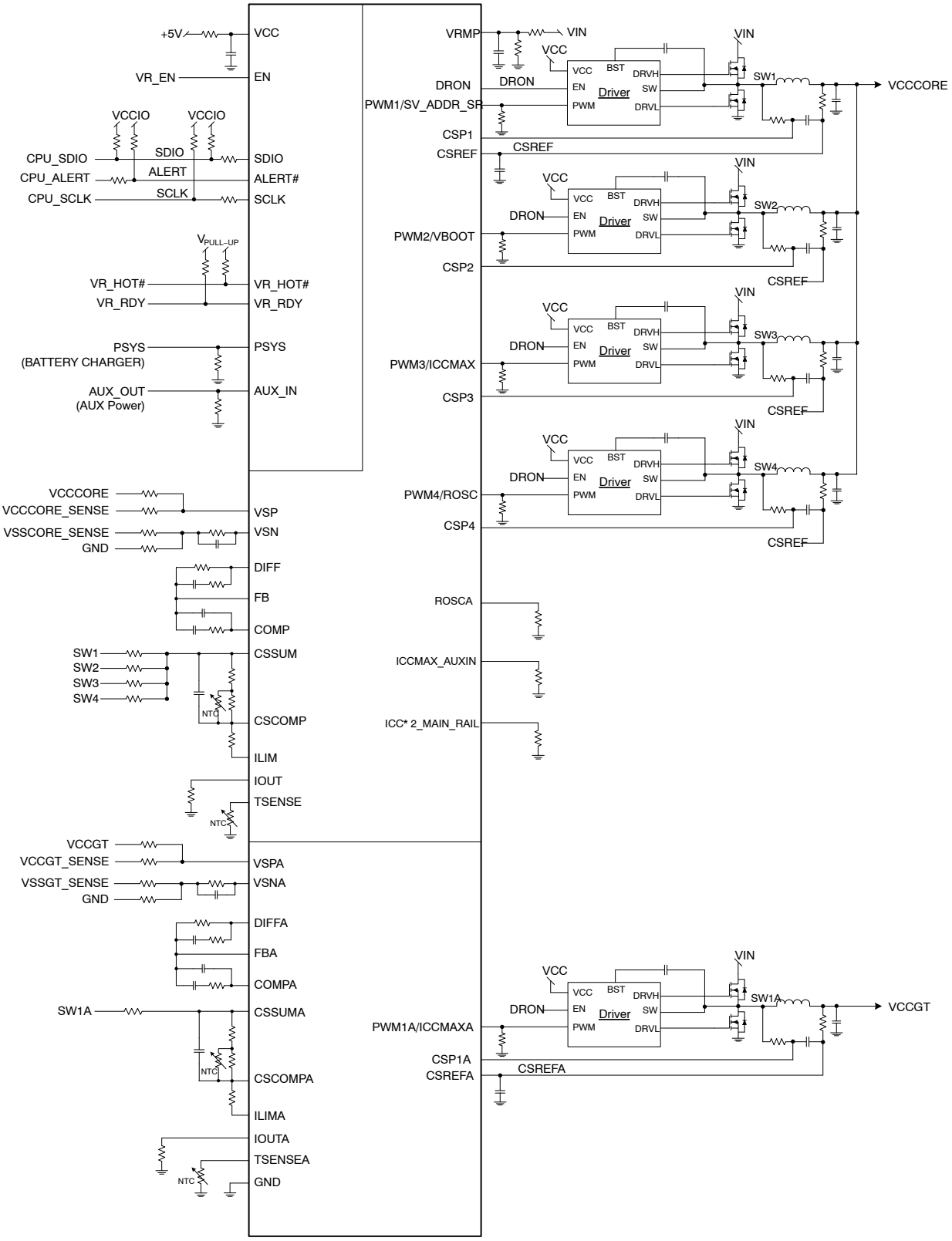


Figure 2. Typical Application Circuit

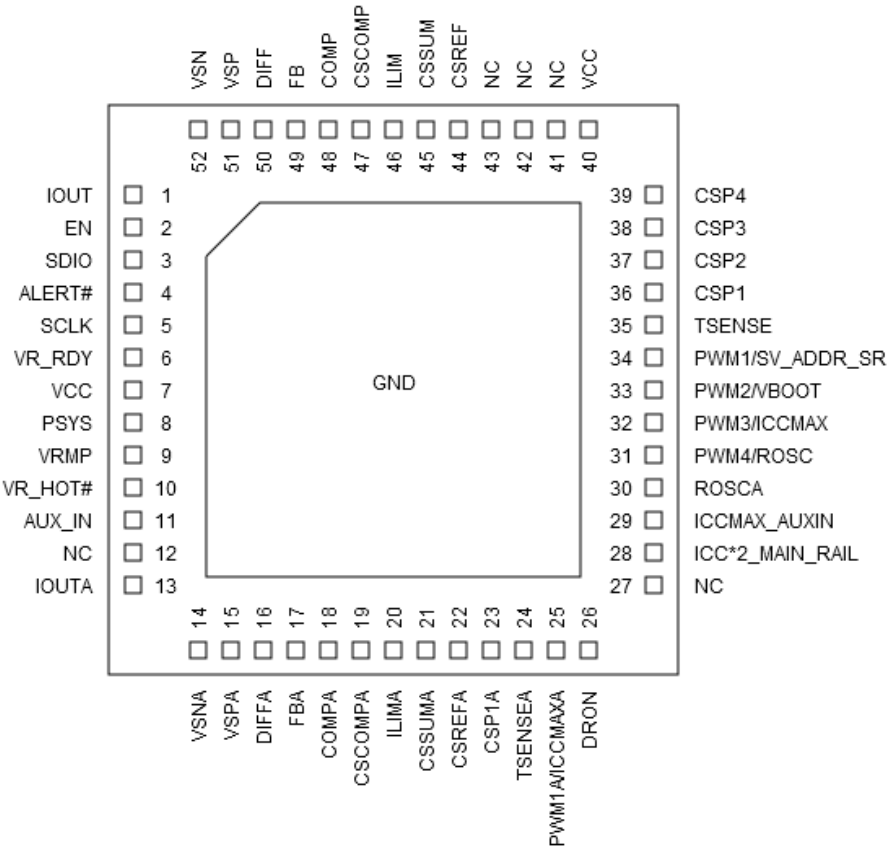


Figure 3. Pinout Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	IOUT	Total output current monitor for regulator 1.
2	EN	Enable. High enables both rails
3	SDIO	Serial VID data interface
4	ALERT#	Serial VID ALERT#
5	SCLK	Serial VID clock
6	VR_RDY	VR_RDY indicates both rails are ready to accept SVID commands
7	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
8	PSYS	System power signal input. A resistor to ground scales this signal.
9	VRMP	Feed−forward input of Vin for the ramp−slope compensation. The current fed into this pin is used to control the ramp of the PWM slopes.
10	VR_HOT#	OD output. Indicates high VR temperature, per channel OCP condition, or OCPL threshold crossed.
11	AUX_IN	AUX IMON Input on 0x0Dh SVID domain. A resistor to ground scales this signal.
12	NC	No Connect
13	IOUTA	Total output current monitor for regulator 2.
14	VSNA	Differential output voltage sense negative for regulator 2.
15	VSPA	Differential output voltage sense positive for regulator 2.
16	DIFFA	Output for regulator 2's differential remote sense amplifier.
17	FBA	Error amplifier voltage feedback for regulator 2.
18	COMPA	Output of the error amplifier and the inverting inputs of the PWM comparators of output for regulator 2.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
19	CSCOMPA	Output of total−current−sense amplifier for regulator 2.
20	ILIMA	Over−current threshold setting − programmed with a resistor to CSCOMPA output for regulator 2.
21	CSSUMA	Inverting input of total−current−sense amplifier of output for regulator 2.
22	CSREFA	Total−current−sense amplifier reference voltage input output for regulator 2.
23	CSP1A	Non−inverting input to current−balance amplifier for Phase 1 output for regulator 2.
24	TSENSEA	Temperature sense input for regulator 2.
25	PWM1A / ICCMAXA	PWM1 output for regulator 2. During startup, ICCMAXA for two−phase regulator is programmed with a pull−down resistor.
26	DRON	External FET driver enable for discrete driver or ONSemi DrMOS.
27	NC	No Connect
28	ICC*2_MAIN_RAIL	Pulldown on this pin programs ICCMAX on main rail from 255 to 511A.
29	ICCMAX_AUXIN	Pulldown resistor on this pin programs ICCMAX for the AUX_IN monitoring rail.
30	ROSCA	Pulldown on this pin programs RoscA % dependent on main rail value and ICCMAX range for main rail.
31	PWM4 / ROSC	PWM4 output for regulator 1 / Pulldown on this pin programs Rosc value for main rail.
32	PWM3 / ICCMAX	PWM3 output for regulator 1 / Pulldown on this pin programs ICCMAX for regulator 1 during startup.
33	PWM2 / VBOOT	PWM2 output for regulator 1 / Pin−program for regulator 1 and regulator 2 Vboot.
34	PWM1 / SV_ADDR_SR	NCP81523: PWM1 output for regulator 1 / Pulldown on this pin configures SVID address and slew rate. NCP81523R: PWM1 output for regulator 1 / Pulldown on this pin configures SVID address, slew rate and VR_Hot control for fast V mode.
35	TSENSE	Temperature sense input for regulator 1.
36	CSP1	Differential current sense positive for Phase 1 of regulator 1.
37	CSP2	Differential current sense positive for Phase 2 of regulator 1.
38	CSP3	Differential current sense positive for Phase 3 of regulator 1.
39	CSP4	Differential current sense positive for Phase 4 of regulator 1.
40	VCC	Recommended to connect this pin to VCC through a 2K resistor
41	NC	No Connect
42	NC	No Connect
43	NC	No Connect
44	CSREF	Total−current−sense amplifier reference voltage input for regulator 1.
45	CSSUM	Inverting input of total−current−sense amplifier for regulator 1.
46	ILIM	Over−current threshold setting − programmed with a resistor to CSCOMP for regulator 1.
47	CSCOMP	Output of total−current−sense amplifier for regulator 1.
48	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators for regulator 1.
49	FB	Error amplifier voltage feedback for regulator 1.
50	DIFF	Output of the regulator 1 differential remote sense amplifier.
51	VSP	Differential output voltage sense positive for regulator 1.
52	VSN	Differential output voltage sense negative for regulator 1.
−	FLAG	GND

1. “Regulator 1” is referred to as “Main” rail throughout the datasheet. “Main” is the primary rail with the highest phase count.
2. “Regulator 2” is referred to as “A” rail throughout the datasheet.

Table 1. MAXIMUM RATINGS (Note 3)

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP	VCC + 0.3 V	−0.3 V	2 mA	2 mA
COMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWMX	VCC + 0.3 V	−0.3 V		1 mA
VSN	GND + 0.3 V	GND − 0.3 V	1 mA	2 mA
VSNA	GND + 0.3 V	GND − 0.3 V	1 mA	2 mA
DIFF	VCC + 0.3 V	−0.3 V	2 mA	2 mA
DIFFA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VR_RDY	VCC + 0.3 V	−0.3 V	2 mA	
VCC	6.0 V	−0.3 V		
VRMP	VCC + 0.3 V	−0.3 V		
SCLK, SDIO	3.6 V	−0.3 V		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. All signals referenced to GND unless noted otherwise

Table 2. ESD Capability

Description	Symbol	Typ	Unit
ESD Capability, Human Body Model (Note 4)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 4)	ESD_{CDM}	750	V

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   Latch−up Current Maximum Rating: ≤ 200 mA per JEDEC standard: JESD78.

Table 3. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Max	Unit
VCC Voltage Range	VCC	4.75	5.25	V
Operating Junction Temperature Range (Note 5)	TJ	−10	125	°C
Operating Ambient Temperature Range	TA	−10	100	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. JEDEC JESD 51−7 with 0 LFM.

Table 4. THERMAL CHARACTERISTICS

Description	Symbol	Typ	Unit
Thermal Characteristic QFN Package	R_{JA}	65	°C/W
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Soldering Temperature		260	°C
Junction−to−Ambient, Thermal Resistance (Note 6)	θ_{JA}	30	°C/W
Junction−to−Case (Top), Thermal Resistance (Note 6)	$\theta_{JC(TOP)}$	18	°C/W
Junction−to−Board Heat Spreader, Thermal Resistance (Note 6)	θ_{JB}	1.0	°C/W
Junction−to−Case (Top), Measurement Reference (Note 6)	Ψ_{J-CT}	1.1	°C/W
Moisture Sensitivity Level QFN Package	MSL	1	

6. JEDEC JESD 51−7 with 0 LFM

Table 5. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Voltage Range		4.75		5.25	V
Quiescent Current	PS0		25		mA
	PS1		23		mA
	PS2		19		mA
	PS3		17		mA
	PS4			79	μA
Quiescent Current	Enable Low			64	μA
UVLO Threshold	VCC Rising			4.5	V
	VCC Falling	4.1			V
	VCC UVLO Hysteresis		100		mV
VRMP					
VIN Supply Range	VRMP range prior to external voltage divider resistor network with 1/12 ratio	4.5		21	V
UVLO Threshold	VRMP Rising			0.355	V
	VRMP Falling	0.250			V
UVLO Hysteresis			100		mV
ENABLE INPUT					
Upper Threshold	Activation Level	0.8			V
Lower Threshold	Deactivation Level			0.3	V
PHASE DETECTION					
CSP Pin Threshold Voltage		VCC−0.4			V
Phase Detect Timer			1.5		ms
IMVP9.1 DAC (PROTOCOL 0Eh)					
System Voltage Accuracy	0.25 V < DAC < 0.495 V (at 25°C only)	−10		10	mV
	0.5 V < DAC < 0.745 V (at 25°C only)	−8		8	mV
	0.75 V < DAC < 1.52 V (at 25°C only)	−0.5		0.5	%
DAC SLEW RATE					
Soft Start Slew Rate			1/4 fast		mV/μs
Slew Rate Slow			1/4 fast		mV/μs
Slew Rate Fast	Resistor Selectable (See Table 7)		>10		mV/μs
DRON					
Output High Voltage	Sourcing 1 mA	3			V
Output Low Voltage	Sinking 1 mA			0.1	V
TSENSE					
TSENSE Bias Current		115.5	120	124.5	μA
Alert#	Assert Threshold		556		mV
	De−Assert Threshold		595		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

N* is the phase configuration number in PS0.

7. Tested at 25°C / 5 V VCC only.
8. Guaranteed by characterization, not production tested.

Table 5. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
TSENSE					
VR_HOT	Assert Threshold		517		mV
	De−Assert Threshold		556		mV
VR_RDY OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = −4 mA		0.1	0.3	V
VR_RDY Rise Time	1 kΩ pull−up to 3.3 V, C_{TOT} = 45 pF		110	150	ns
VR_RDY Fall Time			20	150	ns
SVID (SDIO and SCLK)					
SVID Voltage Low Level (Note 7)	VIL			0.45	V
SVID Voltage High Level (Note 7)	VIH	0.65			V
SVID Pull Down Resistance			4		Ω
SDIO Output Low Voltage	VOL			0.3	V
SVID Clock to Data Delay (Note 8)	TCO			12	ns
SVID Setup Time (Note 8)		7			ns
SVID Hold Time (Note 8)		14			ns
Pad and Pin Capacitance (Note 8)			5		pF
ALERT#					
VOL (Output Low)				0.3	V
OVP AND UVP					
Absolute Over Voltage Threshold	10 mV DAC step During Soft Start − CSREF Rising	3.3	3.44	3.6	V
	5 mV DAC step During Soft Start − CSREF Rising	2.4	2.5	2.6	V
Over Voltage Threshold Above DAC	VSP−VSN−VID Rising	350	400	475	mV
Over Voltage Delay	VSP−VSN Rising to PWM Low		50		ns
Under Voltage Threshold Below DAC−DROOP (VUVM)	VSP−VSN−VID Falling	−440	−400	−360	mV
Under Voltage Delay			5		μs
PWM OUTPUT					
Output High Voltage	Sourcing 500 μA	Vcc−0.2			V
Output Mid Voltage	No Load, Power State 2	1.7	1.8	1.9	V
Output Low Voltage	Sinking 500 μA			0.7	V
DIFFERENTIAL AMPLIFIER					
Input Bias Current	VSP = 1.3 V	200		500	nA
−3 dB Bandwidth	CL = 20 pF, RL = 10 kΩ		22.5		MHz
Closed Loop DC Gain	VSP − VSN = 0.5 V to 1.3 V		1		V/V
ERROR AMPLIFIER					
Input Bias Current	Input = 1.3 V	−400		400	nA

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Table 5. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
DC Gain	CL = 20 pF, RL = 10 kΩ		80		dB
−3 dB Bandwidth	CL = 20 pF, RL = 10 kΩ		20		MHz
Slew Rate	ΔVin = 100mV, G=−10V/V, ΔVout = 1.5 V to 2.5 V, CL = 20 pf, RL = 10 kΩ		5		V/μs
OVER−CURRENT PROTECTION (ILIM)					
ILim Threshold Current (Delayed OCP shutdown)	PS0	8.5	10	11.5	μA
	PS1, PS2, PS3		10/N*		μA
ILim Threshold Current (Immediate OCP shutdown)	PS0	13.5	15	16.5	μA
	PS1, PS2, PS3		15/N*		μA
Shutdown Delay	Immediate		1.3		μs
	Delayed		50		μs
IOUT OUTPUT					
Current Gain	IOUT/ILIM (RLIM = 20 kΩ, RIOUT = 5 kΩ, Vout = 0.8 V, 1.25 V, 1.52 V)	9.5	10	10.5	A/A
PWM GENERATOR					
PWM Minimum Pulse Width			40		ns
0% Duty Cycle	Comp Voltage for PWM Held Low		1.3		V
100% Duty Cycle	Comp Voltage for PWM Held High VIN at 4.5 V		1.75		V
100% Duty Cycle	Comp Voltage for PWM Held High VIN at 21 V		3.4		V
CURRENT SUMMING AMPLIFIER (CSAMP)					
Offset Voltage		−500		500	μV
Input Bias Current	CSSUM = CSREF = 1.0 V	−10		10	μA
Open Loop Gain			80		dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND		10		MHz
CURRENT BALANCE AMPLIFIER					
Differential Mode Input Voltage Range	CSNx = 1.2 V	−100		100	mV
PSYS					
Full Scale Input Voltage			2.5		V
Disable Threshold			V_{CC}−0.4		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

N* is the phase configuration number in PS0.

7. Tested at 25°C / 5 V VCC only.
8. Guaranteed by characterization, not production tested.

Start Up

Following the rise of VCC above the UVLO threshold, externally programmed configuration data is collected, and all PWM outputs are set to Mid−level to prepare the gate drivers of the power stages for activation. When the controller is enabled, DRON is asserted (high) to activate the external gate drivers. A digital counter steps the DAC up from zero to the target boot voltage based on the Soft Start Slew Rate in the spec table. As the DAC ramps, the PWM outputs of each rail will change from Mid−level to high when the first PWM pulse for that rail is produced. When the controller is disabled, the PWM signals return to Mid−level. The VR_RDY signal is asserted when the controller is ready to accept the first SVID command.

TIMING DIAGRAMS

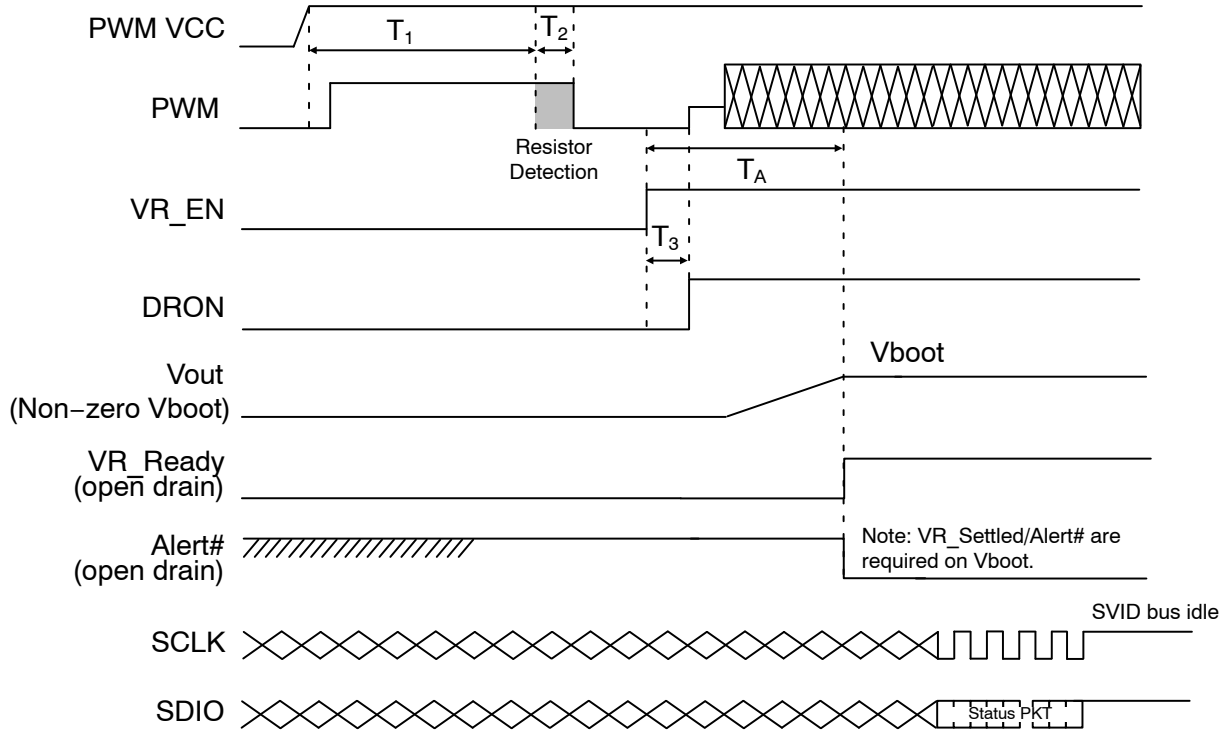

Figure 4. Start−Up Timing Diagram − VBOOT

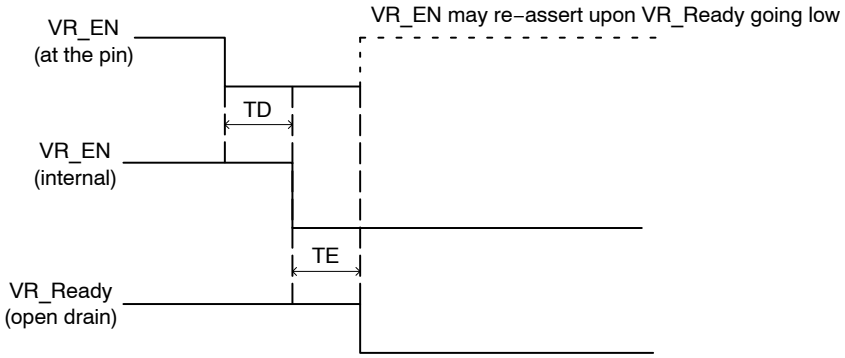

Figure 5. Shut−Down Timing Diagram

Table 6. VR START UP AND ENABLE TIMINGS

Description		Min	Typ	Max	Units
TA	VR_EN to VR_Ready. Controller ready to accept SVID command	−	−	2.5	ms
TD	External de−assertion of VR_EN to the internal recognition of VR_EN de−assertion (glitch filter)	0	−	1	μs
TE	VR_EN internal de−assertion to VR_Ready de−assertion	−	−	500	ns
T1	VCC rise over UVLO to configured resistor detection begin	−	1.5	−	ms
T2	Configured resistor detection time	−	100	−	μs
T3	VR_EN to DRON	−	117	−	μs

DEVICE CONFIGURATION

Phase and Rail Configuration

During start−up, the number of operational phases of the multiphase rail is determined by the internal circuitry monitoring the CSP inputs. If a reduced phase count is required, the appropriate CSP pins should be externally pulled to VCC with a resistor during startup. Also, whether or not the PSYS function is active and responds to an address call on the SVID bus is determined by the internal circuitry monitoring the PSYS input. Tying the PSYS input to VCC will cause the PSYS rail to not respond to any calls to address 0Dh on the SVID bus.

Basic Configuration

The controller has four basic configuration features. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. The following features will be programmed:

- SVID Address
- Slew Rate
- V_{BOOT}
- Output Voltage Step

NCP81523R Fast V Mode

VR_HOT assertion for Fast V mode on/off selection as shown in Table 10. Fast V mode is disabled on the NCP81523.

Switching Frequency

Switching frequencies between 180 kHz and 1.17 MHz are programmed on power up with pulldown resistors on Rosc and RoscA pin. Switching frequency options are shown in Table 14.

ICCMAX

The SVID interface provides the platform ICCMAX values at register 21h. Resistors to ground on the PWM3/ICCMAX, PWM1A/ICCMAXA and ICCMAX_AUXIN pins program these registers on power up. 10 μA is sourced from this pin to generate a voltage on the program resistor. The value of the register is set by the equation below. The resistor value should be no less than 10 kΩ.

$$ICCMAX_{21h} = \frac{R \cdot 10\ \mu A \cdot 255}{2.5\ V}$$

ICCMAX Additional Capability

IMVP9.1 adds an option to extend the current range of the main rail by scaling the lsb size of register $ICCMAX_{21h}$ by $2^{ICCMAX\_ADD_{50h}[1:0]}$ amps (See Table 7). On the NCP81523, these register bits can be configured to 2 A per bit by enabling ICC*2_MAIN_RAIL mode. See Table 13 for details on how to enable this mode.

Table 7. ICCMAX CAPABILITY SCALING

$ICCMAX\_ADD_{50h}[4:0]$		ICC Scaling	Power Scaling
Power [4:2]	Current [1:0]		
010	00	1 A / bit	4 W /bit
011	01	2 A / bit	8 W / bit

When ICC*2_MAIN_RAIL mode is enabled, the bits $ICCMAX\_ADD_{50h}$[1:0] are set to 01b to indicate a scaling of 2 A per bit. This scaling applies to both the $ICCMAX_{21h}$ and the $IOUT\_H_{15h}$ SVID registers. The bits $ICCMAX\_ADD_{50h}$[4:2] are also set to 011b to indicate that the POUT_H18h register value is scaled to 8 W per bit. See SVID register $ICCMAX\_ADD_{50h}$ description in Table 17 for more details. Table 8 shows the rail configurations when ICC*2_MAIN_RAIL mode is enabled and disabled.

Table 8. RAIL SETTINGS FOR ICC*2_MAIN_RAIL MODE

		ICC*2_MAIN_RAIL	
		Disabled	Enabled
Main Rail	$ICCMAX_{21h}$ LSB Size	1A	2A
	$IOUT_{15h}$ LSB Size	1A	2A
	$POUT_{18h}$ LSB Size	4 W	8 W
	$HIGHPOWER\_ICCMAX\_ADD_{50h}$[1:0]	00	01
	$HIGHPOWER\_ICCMAX\_ADD_{50h}$[4:2]	010	011
	Loadline Weighting	43.75%	87.50%
A Rail	$ICCMAX_{21h}$ LSB Size	1A	
	$IOUT_{15h}$ LSB Size	1A	
	$POUT_{18h}$ LSB Size	4 W	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}$[1:0]	00	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}$[4:2]	010	
	Loadline Weighting	93.75%	
VCCIN_AUX	$ICCMAX_{21h}$ LSB Size	1A	
	$IOUT_{15h}$ LSB Size	1A	
	$POUT_{18h}$ LSB Size	4 W	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}$[1:0]	00	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}$[4:2]	010	

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

CCM/DCM Operation

In PS0, all rails operate in Continuous Conduction Mode (CCM) which uses the dual−edge control methodology. However, if PS0 is configured as one−phase instead of multi−phase, the control methodology changes to RPM operation. RPM has great transient performance in one−phase CCM operation. The RPM frequency average DC value is targeted to be similar to the PS0 Dual Edge frequency. However, the switching frequency of RPM depends on input voltage, output voltage, load current, inductor value, and output capacitor value. In PS1, all rails operate in one−phase CCM RPM. In PS2 and PS3, all rails operate in either CCM or Discontinuous Conduction Mode (DCM). It depends on load current in order to prevent loss of efficiency from negative inductor current.

Table 9. NCP81523 SVID ADDRESS AND SLEW RATE

Resistor (kΩ)	SR (mV/us)	Main Rail SVID Address	A Rail SVID Address
10	10	00	01
14	30	00	01
18.7	48	00	01
24.3	10	01	00
30.9	30	01	00
38.3	48	01	00
47.5	10	00	02
59	30	00	02
71.5	48	00	02
86.6	10	01	02
105	30	01	02
127	48	01	02

Table 10. NCP81523R SVID ADDRESS, SLEW RATE AND FAST V MODE

Resistor (kΩ)	SR (mV/us)	Main Rail SVID Address	A Rail SVID Address	VR_HOT Assertion Fast V Mode
10	10	0	1	ON
14	30	0	1	ON
18.7	48	0	1	ON
24.3	10	0	1	OFF
30.9	30	0	1	OFF
38.3	48	0	1	OFF
47.5	10	0	2	ON
59	30	0	2	ON
71.5	48	0	2	ON
86.6	10	0	2	OFF
105	30	0	2	OFF
127	48	0	2	OFF

Table 11. V_{BOOT} AND OUTPUT VOLTAGE STEP

Resistor (kΩ)	V_{BOOT}(V) Main rail	V_{BOOT}(V) A rail	Output Voltage Step
10	0V	0V	Both rail 5mV/step
14	0V	1.05V	
18.7	1.05V	0V	
24.3	1.05V	1.05V	
30.9	0V	0V	Both rail 10mV/step
38.3	0V	1.8V	
47.5	1.8V	0V	
59	1.8V	1.8V	
71.5	0V	0V	Main rail 5mV/step. A rail 10mV/step.
86.6	0V	1.8V	
105	1.05V	0V	
127	1.05V	1.8V	
154	0V	0V	Main rail 10mV/step. A rail 5mV/step.
187	1.8V	0V	
221	0V	1.05V	
280	1.8V	1.05V	

Table 12. POWER STATES

SVID Power State	Typical Operating Mode
PS0	Multiphase rail dual edge
PS1	One−phase CCM RPM
PS2	One−phase DCM RPM
PS3	One−phase DCM RPM
PS4	Standby

PSYS

The PSYS pin is an analog input to the VR controller. PSYS is a system input power monitor that facilitates the monitoring of the total platform system power. The system power is sensed at the platform charging device, the VR controller facilitates reporting back current and through the SVID interface at address 0Dh.

AUX_IN

The AUX_IMON current monitor input is a means of measuring the VCCIN_AUX platform VR output current using the IMVP9.1 ADC. This input is used to digitize the VCCIN_AUX output current information, which is sent to the IMVP9.1 PWM controller as an analog current mode signal proportional to the VCCIN_AUX output current. The signal is converted to a voltage at the IMVP9.1 controller input pin by a termination resistor, located at the controller. A resistor with high input impedance should be selected to avoid loading effects on the signal. The AUX Current reading is scaled by ICCMAX_AUXIN and can be read back on Register 0x15 of Rail 0x0D of the controller SVID bus.

Programming Pin

This is a multifunction select pin used to set the operation of multiple features and the combination of these features enabled/disabled. Items programmed on this pin are ICC*2_MAIN_RAIL which allows the user to select if the ICCMAX and IOUT reporting for the main rail is a 1 A or 2 A LSB step size. When off, the resolution is 1 A per LSB. When on, the resolution is set to 2 A per LSB which allows reporting of over 255 A on the main rail only.

The other options include dithering and acoustic noise solution.

Table 13. PIN OF ICC*2_MAIN_RAIL CONFIGURATION

Resistor (kΩ)	ICC*2 Main Rail	Acoustic Noise Solution	Dithering
10	OFF	OFF	OFF
18.7	OFF	OFF	ON
30.9	OFF	ON	OFF
47.5	OFF	ON	ON
71.5	ON	OFF	OFF
105	ON	OFF	ON
154	ON	ON	OFF
221	ON	ON	ON

Table 14. SWITCHING FREQUENCY

R_{OSC}/R_{OSCA} Control by Pin Resistor (kΩ)	Switching Frequency (kHz)
	1 Phase ~ 4 Phase
10	180
14	225
18.7	270
24.3	315
30.9	360
38.3	405
47.5	450
59	495
71.5	540
86.6	630
105	720
127	810
154	900
187	990
221	1080
280	1170

Input Voltage Feed−Forward (VRMP Pin)

Ramp generator circuits are provided for the dual−edge modulator. The ramp generators implement input voltage feed−forward control by varying the ramp slopes proportional to the VRMP pin voltage. The VRMP pin also has a UVLO function, which is active only after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled. For multi−phase operation, the dual−edge PWM ramp amplitude is changed according to the following:

$$VRMP_{PP} = 0.1 \cdot V_{VRMP}$$

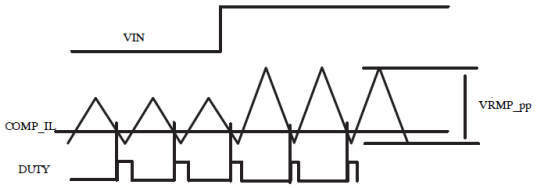

Figure 6. Ramp Feed Forward

An external voltage divider is required on this VRMP pin. In order to scale the voltage seen on the VRMP pin, the voltage divider on the pin needs to be setup to maintain a ratio of 1/12. Typical resistor values may include 1 MΩ Rup / 90.9 kΩ Rdown or 1.1 MΩ Rup / 100 kΩ Rdown. UVLO on VRMP is inactive in PS4 power state and PS3 when a VID to 0 V is received.

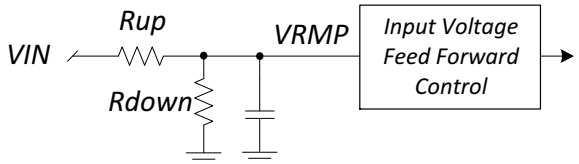

Figure 7. Ramp Feed Forward Circuit

Differential Current Feedback Amplifiers

Each phase of the rail has a low offset, differential amplifier to sense the current of that phase in order to balance current. The CSREF and CSPx pins are high impedance inputs, but it is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset due to leakage current.

It is also recommended that the voltage sense element be no less than 0.5 mΩ for best current balance.

The external filter RCSN and CCSN time constant should match the inductor L/DCR time constant, but fine tuning of this time constant is generally not required. Phase current signals are summed with the COMP or ramp signals at their respective PWM comparator inputs in order to balance phase currents via a current mode control approach.

$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \cdot DCR}$$

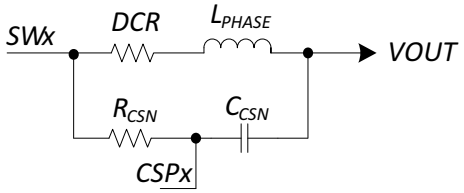

Figure 8. Per Phase Current Sense Network

Total Current Sense Amplifier

The multiphase rail uses a patented approach to sum the phase currents into a single, temperature compensated, total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The Rref(n) resistors average the voltages at the output terminals of the inductors to create a low impedance reference voltage at CSREF. The Rph resistors sum currents from the switch nodes to the virtual CSREF potential created at the CSSUM pin by the amplifier. The total current signal is the difference between the CSCOMP and CSREF voltages.

The amplifier filters, and amplifies, the voltage across the inductors in order to extract only the voltage across the inductor series resistances (DCR). An NTC thermistor (Rth) in the feedback network placed near the Phase 1 inductor senses the inductor temperature, and compensates both the DC gain and the filter time constant for the change in DCR with temperature. The Phase 1 inductor is chosen for the thermistor location so that the temperature of the inductor providing current in the PS1 power mode.

The DC gain equation for the DC total current signal is:

$$V_{CSCOMP} - V_{CSREF} = \frac{R_{CS2} + \frac{R_{CS1} \cdot Rth}{R_{CS1} + Rth}}{Rph} \cdot DCR \cdot I_{OUT}$$

Set the DC gain by adjusting the value of the Rph resistors in order to make the ratio of total current signal to output current equal the desired loadline. The values of Rcs1 and Rcs2 are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.

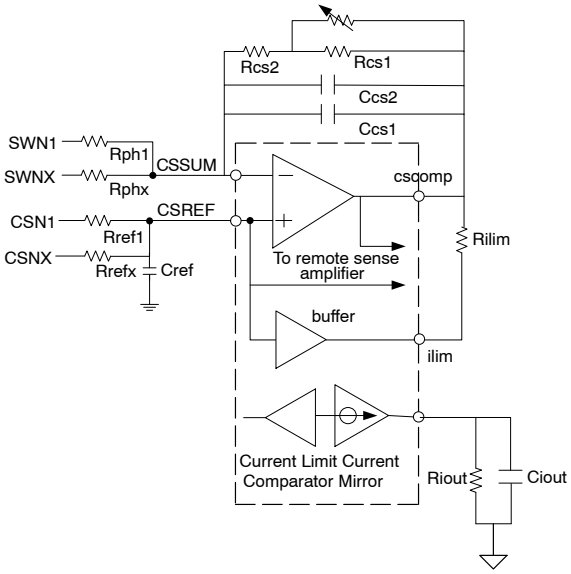

Figure 9. Total Current Sense Amplifier

The pole frequency of the CSCOMP filter should be set equal to the zero of the output inductor. This causes the total current signal to contain only the component of inductor voltage caused by the DCR voltage, and therefore to be proportional to inductor current. Connecting Ccs2 in parallel with Ccs1 allows fine tuning of the pole frequency using commonly available capacitor values. It is best to perform fine tuning during transient testing.

$$F_Z = \frac{DCR_{25°C}}{2\pi \cdot L_{PHASE}}$$

$$Fp = \frac{1}{2\pi \cdot \left(R_{CS2} + \frac{R_{CS1} \cdot Rth}{R_{CS1} + Rth}\right) \cdot \left(C_{CS1} + C_{CS2}\right)}$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier.

The value of the CREF capacitor (in nF) on the CSREF pin should be:

$$Cref = \frac{0.02 \cdot Rph}{Rref}$$

High Performance Voltage Error Amplifier

The Remote Sense Amplifier output feeds a Type III compensation network formed by the Error Amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote Sense Amplifier output.

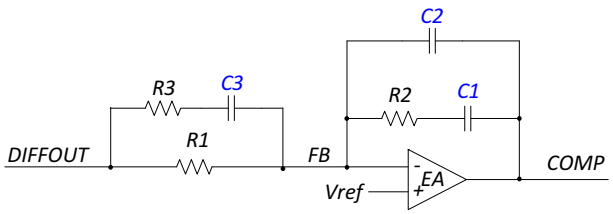

Figure 10. Error Amplifier

Loadline Programming (V_{DROOP})

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

A load line is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. The load line is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.

$$V_{DROOP} = \frac{R_{CS2} + \frac{R_{CS1} \cdot Rth}{R_{CS1} + Rth}}{Rph} \cdot DCR \cdot I_{OUT}$$

For the main rail, loadline programming is dependent on its programmed ICCMAX value.

$$Loadline = DCR \times \frac{RCS}{Rph} \times Weighting$$

For ICC*2_MAIN_RAIL configuration enabled, , weighting = 87.50%.
For ICC*2_MAIN_RAIL configuration disabled, weighting = 43.75%.
For the A rail, loadline weighting = 93.75%.

Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense regulator output voltage. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage.

$$V_{DIFFOUT} = \left(V_{VSP} - V_{VSN}\right) + \left(1.3\ V - V_{DAC}\right) + \left(V_{DROOP} - V_{CSREF}\right)$$

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins. The multiphase rails generates a replica of the CSREF pin voltage at the ILIM pin, and compares ILIM pin current to ICL0 and ICLM0 (ICL1 and ICLM1 in PS1, PS2 and PS3). The controller latches off if ILIM pin current exceeds ICL0 (ICL1 for PS1, PS2, and PS3) for t_{OCP_DELAY}, and latches off immediately if ILIM pin current exceeds ICLM0 (ICLM1 for PS1, PS2 and PS3). Set the value of the current limit resistor RLIMIT according to the desired current limit Iout LIMIT.

$$R_{LIMIT} = \frac{R_{CS2} + \frac{R_{CS1} \cdot Rth}{R_{CS1} + Rth}}{Rph} \cdot DCR \cdot I_{OUT_{LIM}}}{10\ \mu}$$

Programming IOUT

The IOUT pin sources a current proportional to the ILIM current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2.5 V signal on IOUT.

$$R_{IOUT} = \frac{2.5\ V \cdot R_{LIM}}{10 \cdot \frac{R_{CS2} + \frac{R_{CS1} \cdot Rth}{R_{CS1} + Rth}}{Rph} \cdot DCR \cdot ICCMAX}$$

Programming DAC Feed−Forward Filter

The multiphase rail outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the DROOP function to current flowing into the charging output capacitors. In the following equations, C_{OUT} is the total output capacitance of the system.

$$R_{FF} = Cout \cdot LL \cdot 453.6 \cdot 10^{6}$$

$$C_{FF} = \frac{LL \cdot Cout}{R_{FF}}$$

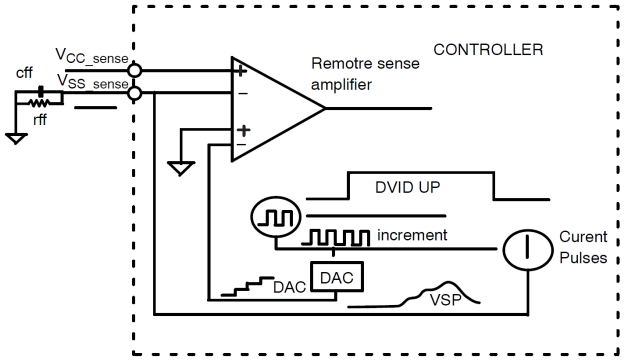

Figure 11. DAC Feed Forward

TSENSE Network

A temperature sense input is provided for each rail. A precision current is sourced from the output of the TSENSE/A pins to generate a voltage on the temperature sense networks. The voltages on the temperature sense

inputs are sampled by the internal A/D converter. A 100k NTC similar to the Murata NCP15WF104E03RC should be used. Rcomp1 in the following Figure is optional, and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.

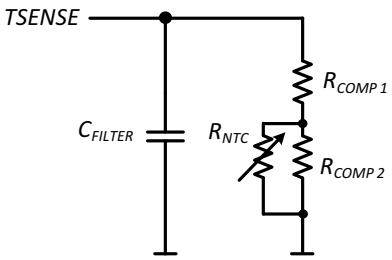

Figure 12. TSENSE Network

PWM Comparators

The noninverting input of each comparator (one for each phase) is connected to the summation of the error amplifier output (COMP) and each phase current (IL×DCR×Phase Balance Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output. During steady state PS0 operation, the main rail PWM pulses are centered on the valley of the triangle ramp waveforms and both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the error amp signal increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

Table 15. PHASE CONFIGURATION

Phase Configuration	Programming Pin in CSPx	Unused Pin
4 + 1	All CSP pins are connected normally	No unused Pin
3 + 1	CSP1 to CSP3, and CSP1A pins connected normally. CSP4 connected to VCC through a 2k resistor.	Use PWM4 for programming ROSC only.
2 + 1	CSP1, CSP2 and CSP1A pins connected normally. CSP3 connected to VCC through a 2k resistor.	Float CSP4. Use PWM4 for programming ROSC only. Use PWM3 for programming ICCMAX only.
2 + 0	CSP1, CSP2, pins connected normally. CSP3 and CSP1A connected to VCC through a 2k resistor.	Float PWM1A and CSP4 Use PWM4 for programming ROSC only. Use PWM3 for programming ICCMAX only.

FAULT PROTECTION

Over Current Protection (OCP)

A programmable total phase current limit is provided that is decreased when not operating in PS0 mode. This limit is programmed with a resistor between the CSCOMP and ILIM pins. The current from the ILIM pin to this resistor is compared to the ILIM Threshold Currents (ICL0, ICLM0, ICL1, and ICLM1). When the A rail is operating in PS0, if the ILIM pin current exceeds ICL0, an internal latch−off timer starts.

If the fault is not removed, the controller shuts down when the timer expires. If the current into the pin exceeds ICLM0, the controller shuts down immediately. When operating in PS1, PS2, or PS3, the ILIM pin current limits are ICL1 and ICLM1. To recover from an OCP fault, the EN pin or VCC voltage must be cycled low.

Input Under−voltage Lockouts (UVLO)

The VR monitors the 5 V VCC supply as well as the VRMP pin voltage. Hysteresis is incorporated within these monitors.

Output Under Voltage Monitor

The multiphase rail output voltage is monitored for under voltage at the output of the differential amplifier. If the multiphase−phase rail output falls more than VUVM2 below the DAC−DROOP voltage, the UVM comparator will trip – sending the VR_RDY signal low.

Output Over Voltage Protection

The multiphase phase output voltage is monitored for OVP at the VSP pin. During normal operation, if an output voltage exceeds the DAC voltage by VOVP, the VR_RDY flag goes low, and the DAC voltage of the overvoltage rail will be slowly ramped down to 0 V to avoid producing a negative output voltage. At the same time, the PWM outputs of the overvoltage rail are sent low. The PWM output will pulse to mid−level during the DAC ramp down period if the output decreases below the DAC + OVP threshold as DAC decreases. When the DAC gets to zero, the PWMs will be held low, and the VR will stay in this mode until the VCC voltage or EN is toggled.

Absolute OVP

During start up, the OVP threshold is set to the absolute over voltage threshold. This allows the controller to start up without false triggering OVP.

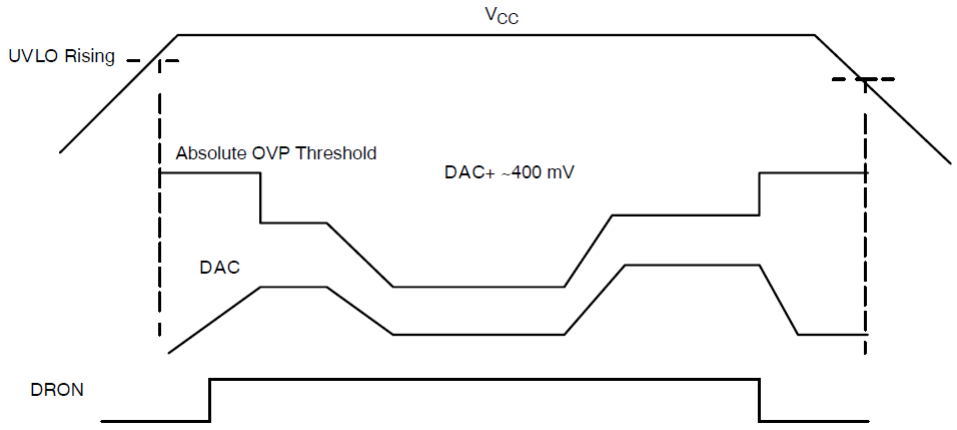

Figure 13. OVP Threshold Behavior

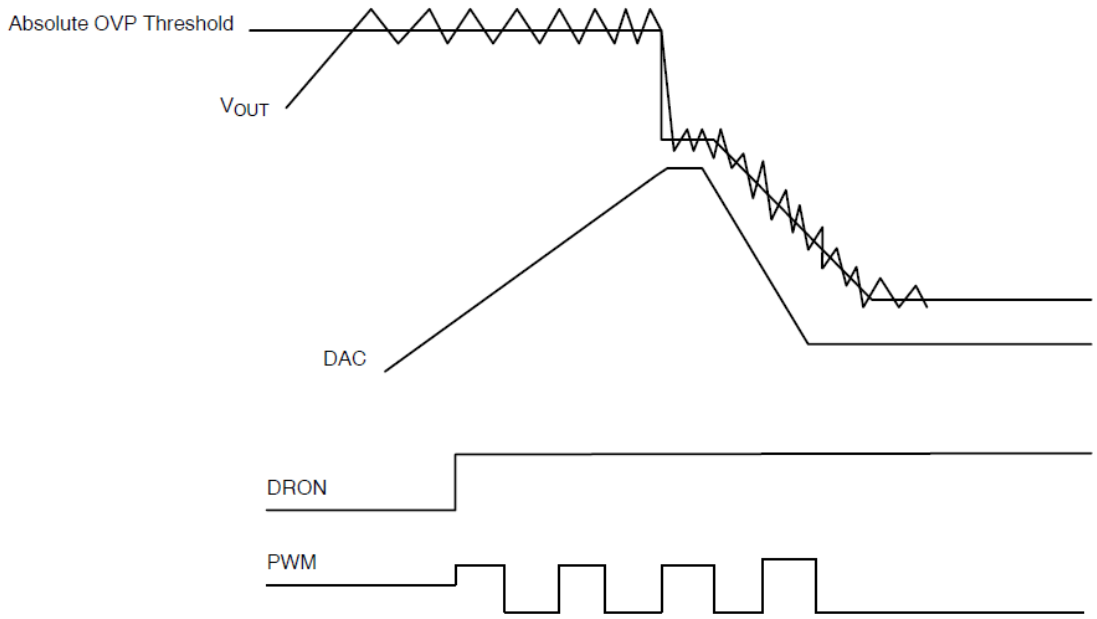

Figure 14. OVP Behavior at Start−up

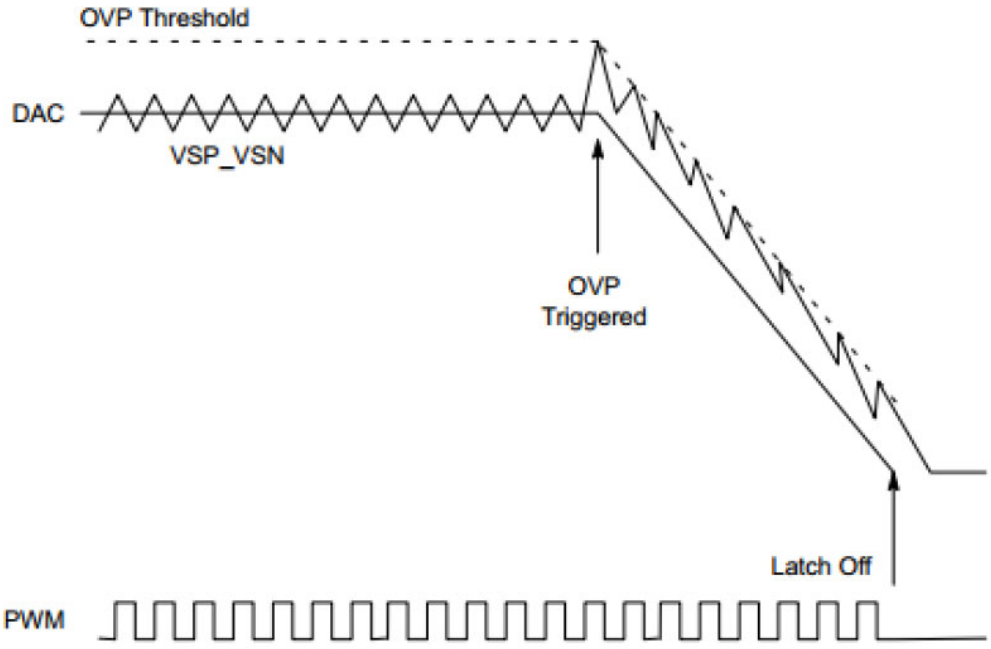

Figure 15. OVP During Normal Operation Mode

Serial VID Interface (SVID)

The Serial VID Interface (SVID Interface) is a 3 wire digital interface used to transfer power management information between the CPU (Master) and the VR controller (Slave). The 3 wires are clock (SCLK), data (SDIO) and ALERT#. The SCLK is unidirectional and generated by the master. The SDIO is bi−directional, used for transferring data from the microprocessor to the VR controller and from the VR controller to the CPU. The ALERT# is an open drain output from the VR controller to signal to the master that the Status Register should be read.

Refer to the relevant Intel document for SVID routing and pull−up topologies. The SVID bus will operate at a max frequency of 43 MHz.

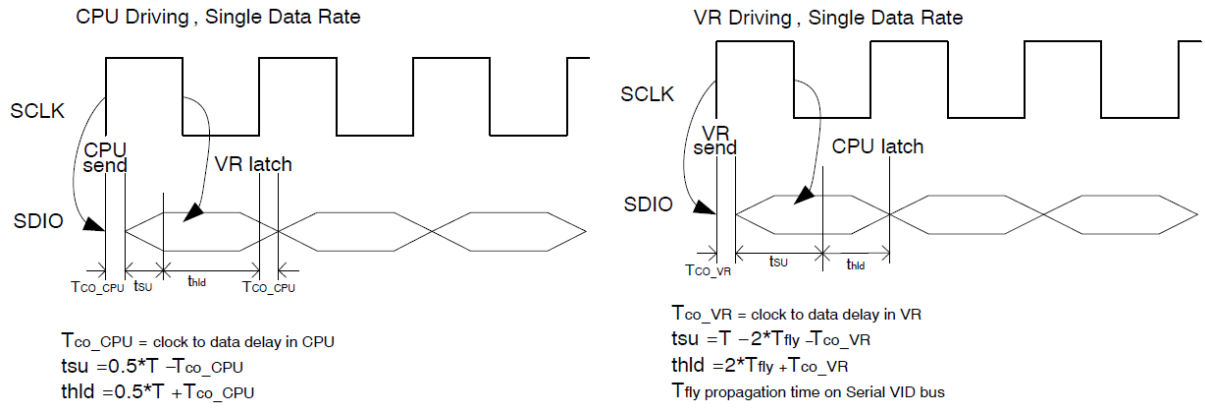

Figure 16. SVID Timing Diagram

Table 16. SLEW RATE

Option	SVID Command Code	Feature Description	Register Address (Indicating the Slew Rate of VID Code Change)
SetVID_Fast	01h	10 mV/μs, 30 mV/μs, or 48 mV/μs VID code change slew rate	24h
SetVID_Slow	02h	= 1/4 of SetVID_Fast VID code change slew rate	25h
SetVID_Decay	03h	No control, VID code down	N/A

Table 17. SVID REGISTER MAP

Index	Register Name	Description	Access	Default 00h	PSYS 0Dh
00h	VENDOR_ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to onsemi is 1Ah.	R	1Ah	1Ah
01h	PROD_ID	Uniquely identifies the VR product. The VR vendor assigns this number. NCP81523 NCP81523R	R	 54h 74h	 54h 74h
02h	PROD_REV	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R	00h	00h
05h	PROTOCOL_ID	Identifies the SVID Protocol the controller supports	R	0Eh	0Eh
06h	CAPABILITY	Informs the Master of the controller's Capabilities "1" = supported, "0" = not supported Bit[7]: Output Current reported as a fraction of ICCMAX. Default = "1" Bit[6]: ADC Measurement of Temp Supported. Default = "1" Bit[5]: ADC Measurement of Pin Supported. Default = "0" Bit[4]: ADC Measurement of Vin Supported. Default = "1" Bit[3]: ADC Measurement of Iin Supported. Default = "0" Bit[2]: ADC Measurement of Pout Supported. Default = "1" Bit[1]: ADC Measurement of Vout Supported. Default = "1" Bit[0]: ADC Measurement of Iout Supported. Default = "1"	R	D7h	N/A
10h	STATUS1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR. Bit[7]: Read status Bit[6:4]: Reserved Bit[3]: VID 30mV above target Bit[2]: ICCMAX status Bit[1]: Temp status Bit[0]: VR settled status	R	00h	N/A

Table 17. SVID REGISTER MAP

Index	Register Name	Description	Access	Default 00h	PSYS 0Dh
11h	STATUS2	Data register showing optional status_2 data. Bit[7:3]: Reserved Bit[2]: Reserved Bit[1]: Data frame fault Bit[0]: Parity fault	R	00h	N/A
12h	TEMPERATURE	Data register showing temperature zones the system is operating in.	R	00h	N/A
14h	LASTREAD	Contains last read value read by GET command.	R	00h	N/A
15h	IOUT_H	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max.	R	01h	01h
16h	VOUT_H	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 15.625 mV.	R	01h	N/A
17h	VR_TEMP	8 bit binary word ADC of voltage. Binary format in deg C, IE 100°C = 64h. A value of 00h indicates this function is not supported. To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resister in parallel. NTC uses 100 kΩ under 25°C and B25/50 approximates 4250. Use 13.5 kΩ for parallel resistor and 0.3 kΩ for series resistor.	R	01h	N/A
18h	POUT_H	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported.	R	01h	N/A
1Ah	VIN_H	8 bit binary word ADC of voltage. Input voltage is (1Ah−2)/7, unit is Volt. Full scale voltage is approximate 36 V	R	01h	N/A
1Bh	PIN_H	Required for Input Power Domain Address 0Dh.	R	N/A	00h
1Ch	STATUS2_LASTREAD	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h	N/A
1Fh	I_C2CL	Cycle−to−cycle current limit level.	R/W	00h	N/A
21h	ICC_MAX	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.	R	00h	00h
22h	TEMP_MAX	Data register containing the max temperature the platform supports and the level (No Suggestions) asserts. This value defaults to 100°C and programmable over the SVID Interface	R	64h	N/A
24h	SR_FAST	Slew Rate for SetVID_fast commands. Binary format in mV/μs.	R	By setting	N/A
25h	SR_SLOW	Slew Rate for SetVID_slow commands. It is 16, 8, 4 or 2 times slower than the SR_fast rate. Binary format in mV/μs. FAST/4 is default for IMVP9.1.	R	1/4 Fast	N/A
26h	VBOOT	The VBOOT is resistor programmed at startup. The controller will ramp to VBOOT and hold at VBOOT until it receives a new SVID SetVID command to move to a different voltage.	R	By setting	N/A
2Ah	SLOW_SR_SEL_HC	Fast_SR/2 (Default), Fast_SR/4, Fast_SR/8, Fast_SR/16	R/W	02h	N/A
2Bh	PS4_EXIT_LAT	Reflects the latency of exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the output voltage beginning to ramp.	R	7Bh	N/A
2Ch	PS3_EXIT_LAT	Reflects the latency of exiting PS3 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID/ SetPS command until the controller is capable of supplying max current of the command PS state.	R	55h	N/A
2Dh	EN_SVID_RDY_T	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands.	R	CAh	N/A

Table 17. SVID REGISTER MAP

Index	Register Name	Description	Access	Default 00h	PSYS 0Dh
30h	VID_MAX	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP9.1 VID format.	R/W	FFh	N/A
31h	VID_SETTING	Data register containing currently programmed VID voltage. VID data format.	R	00h	N/A
32h	PWR_STATE	Register containing the current programmed power state.	R	00h	N/A
33h	OFFSET	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0 = positive margin, 1 = negative margin. Remaining 7 BITS are #. VID steps for margin 2 s complement 00h = no margin 01h = +1 VID step 02h = +2 VID steps FFh = −1 VID step FEh = −2 VID steps	R/W	00h	N/A
34h	MULTI_VR_CFG	Bit mapped data register that configures multiple VRs behavior on the same bus and can be programmed to reset behavior of VR_Ready under 0.0 V VID command.	R/W	00h	00h
35h	MAIN_ADDR_PTR	Write address pointer for main address space.	R/W	35h	N/A
49h	PSYS_DBC_CLR	Sets the duration of the Deassert Debounce applied to the PSYS critical comparator. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R/W	N/A	00h
4Ah	PSYS_CR_LVL_H	Sets the threshold level of the PSYS critical comparator, while PSYS is higher than this threshold the VR_HOT signal is asserted. Must be scaled to the same voltage level as PSYS ADC. Delay from PSYS exceeding threshold to VR_HOT# assertion is dependent on register 0x4F debounce time.	R/W	N/A	00h
4Bh	PSYS_W2_LVL_H	Sets the threshold level of the PSYS warning 2 comparator. Must be scaled to the same voltage level as PSYS ADC	R/W	N/A	00h
4Ch	PSYS_W1_LVL_H	Sets the threshold level of the PSYS warning 1 comparator. Must be scaled to the same voltage level as PSYS ADC	R/W	N/A	00h
4Dh	PSYS_WARN2_CNT	This counter accumulates the duration of time that the PSYS input is above the warning 2 level set by register 0x4B. This register is only cleared on each read or when the threshold level in 0x4B is changed. This register does not roll over when it reaches 0xFF. Data is held while in PS4. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R	N/A	00h
4Eh	PSYS_WARN1_CNT	This counter accumulates the duration of time that the PSYS input is above the warning 1 level set by register 0x4C. This register is only cleared on each read or when the threshold level in 0x4C is changed. This register does not roll over when it reaches 0xFF. Data is held while in PS4. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R	N/A	00h
4Fh	PSYS_DBC_SET	Sets the duration of the Assert Debounce applied to the PSYS critical comparator. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R/W	N/A	00h
50h	ICCMAX_ADD	ICCMAX additional capability Bit[7:2]: Optional if not supported reads 0’s Bit[1:0]: “00” = 255A, “01” = 511A, where “00” indicates 1A/bit scaling and “01” indicates 2A/bit scaling	R	By setting	N/A
5Ch	C2CL_EVENT_CNT	Cycle−to−cycle current limit triggered event counter.	R	00h	N/A

Table 18. IVMP9.1 VID COMMAND

VID Code (Hex)	Setting Voltage (V) (5 mV/step)	Setting Voltage (V) (10 mV/step)
00h	0	0
01h	0.250	0.200
02h	0.255	0.210
03h	0.260	0.220
04h	0.265	0.230
05h	0.270	0.240
...	...	...
A1h	1.050	1.800
...	...	...
FBh	1.500	2.700
FCh	1.505	2.710
FDh	1.510	2.720
FEh	1.515	2.730
FFh	1.520	2.740

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