NCP3901

Dual Input, Single Output Power Source Multiplexer

The NCP3901 integrated circuit is a dual input, single output power source multiplexer. It is optimized for multiplexing 2 different charging inputs to feed a single input battery charger. To address all types of applications, the device is able to support autonomous and slave modes of operation. Reverse USB on−the−go is fully supported.

Features

- 3 A DC Minimum Current through Power Paths
- Reverse 5 V OTG Support through VINA Path
- Maximum 20 V Over Voltage Threshold
- 28 V Absolute Maximum Voltage on VINA
- Compliance with IEC61000−4−5 at 100 V for VINA
- Indication of Presence of Second Input
- Autonomous Priority Selection and Switch Over Lock
- Small Footprint: 3.1 x 1.65 mm WLCSP28 0.4 mm Pitch
- 30 ms Minimum Break−before−make Time
- This is a Pb−Free Device

Typical Applications

- Handheld Devices
- Tablets
- Smart Phone
- PDAs

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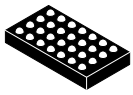


WLCSP28
FCC SUFFIX
CASE 567KR

MARKING DIAGRAM

3901= NCP3901
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 11 of this data sheet.

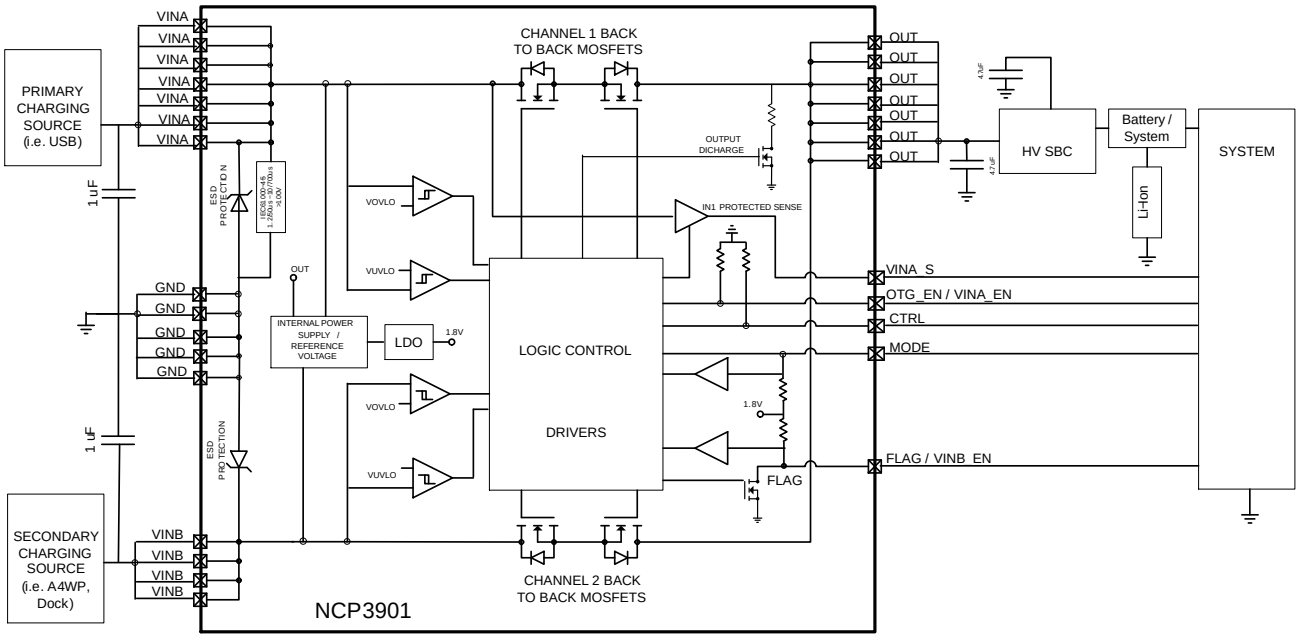


Figure 1. Typical Application Circuit

Table 1. PIN FUNCTIONAL DESCRIPTION

Pin	Name	Type	Description
A1	VINA	POWER	Channel 1 power input path. These pins must be decoupled with a 1 μF input capacitor.
A2			
A3			
A4			
A5			
A6			
A7			
C4	OUT	POWER	Output power path. Connected to battery charger. These pins must be decoupled with a 4.7 μF input capacitor.
B5			
B6			
B7			
C5			
C6			
C7			
B1	GND	GROUND	Ground. Must be connected to a ground plane.
B2			
B3			
C2			
C3			
D4	VINB	POWER	Channel 2 power input path. These pins must be decoupled with a 1 μF input capacitor.
D5			
D6			
D7			
C1	MODE	DIGITAL INPUT	Digital Input Pin. Used to determine autonomous−or slave mode.
D1	CRTL	DIGITAL INPUT	Digital Input Pin. Used to determine autonomous−locked or autonomous−not locked mode.
B4	VINA_S	ANALOG OUTPUT	Image of VINA input when VINA is within the operating range.
D2	VINA_EN/OTG_EN	DIGITAL INPUT	Used to select USB On−The−Go mode on channel 1
D3	VINB_EN/FLAG	DIGITAL INPUT / OPEN DRAIN OUTPUT	VINB valid indicator. This pin is used to indicate VINB is valid. Can also be used as an input to enable both VINA and VINB channels.

Pin Out

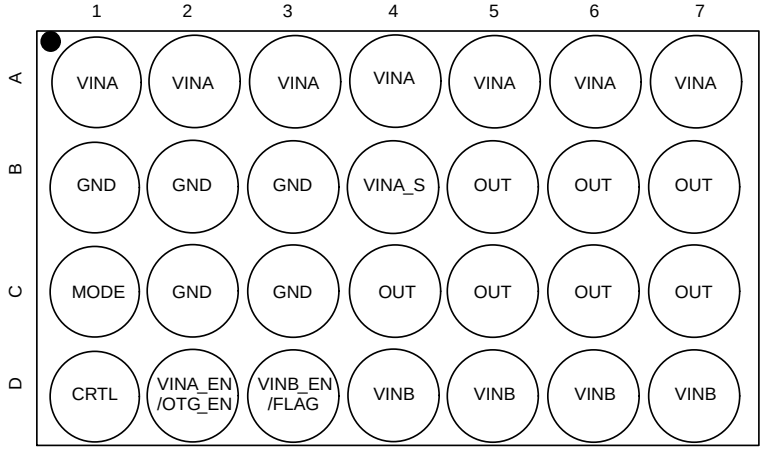


Figure 2. Package TOP VIEW

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VINA, (Note 1)	V_{INA}	−0.3 to +29	V
VINA, (Note 2)		100	V
VINB, VINA_S (Note 1)	V_{INB}	−0.3 to +21	V
OUT (Note 1)	V_{OUT}	−0.3 to +18	V
CTRL, MODE, VINA_EN/OTG_EN, VINB_EN/FLAG (Note 1)	V_{CTRL}	−0.3 to +6	V
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature (Note 3)	T_J	−40 to +TSD	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	
Human Body Model (HBM) ESD Rating (JEDEC standard: JESD22−A114)	ESD HBM	2500	V
Charged Device Model (CDM) ESD Rating (JEDEC standard: JESD22−A114)	ESD CDM	2000	V
Latch up Current (JEDEC standard: JESD78 class II):	ILU	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. With Respect to GND. According to JEDEC standard JESD22−A108.
2. With Respect to GND. According to standard IEC61000−4−5 1.2/50 μs.
3. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

Table 3. OPERATING CONDITION

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INA}	Operational Power Supply on VINA		0		28	V
V_{INB}	Operational Power Supply on VINB		0		20	V
V_{CTRL},V_{MODE}, V_{INA_EN/OTG_EN}, $V_{INB\_EN/FLAG}$	Operational Supply		0		5.5	V
I_{OUT}	Operational Output Current		0		3	A
V_{OUT}	Operational Supply on OUT	OTG mode, VINA = VINB = 0 V	0		5.5	V
		Charging mode	0		17.3	V
C_{IN}	Input Capacitor			1		μF
C_{OUT}	Output Capacitor			4.7		μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	(Notes 3 and 5)		60		°C/W
T_J	Junction Temperature Range		−40	25	+125	°C

5. The $R_{\theta JA}$ is dependent on the PCB heat dissipation. Board used to drive this data was a 2s2p JEDEC PCB standard.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between V_{UVLO} to V_{OVLO} (Unless otherwise noted) Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CORE						
V_{UVLO}	Under Voltage Lockout applied to VINA, VINB or OUT	Rising	−	−	3.0	V
		Falling	2.45	−	−	V
V_{OVLO}	Over Voltage Lockout Referred to VINA or VINB	Rising		17		V
		Falling		16.4		V
I_{OFF}	Stand by current	Measured on VOUT, VINA and VINB < UVLO, OTG mode off		20		μA
I_{ON}	Quiescent Current	VINB > UVLO			100	
		VINA and VINB > UVLO (including FLAG pull down)			200	
V_{INTPUP}	Internal pull up	Measured on FLAG pin or MODE pin	1.6	1.8	2	V
V_{CTRLH}	CTRL High− input voltage		2.2		5.5	V

6. Guaranteed by design and characterization.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between V_{UVLO} to V_{OVLO} (Unless otherwise noted) Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CORE						
V_{IH}	MODE, VINA_EN/OTG_EN, VINB_EN/FLAG, CTRL High−level input voltage		1.2		5.5	V
V_{IL}	MODE, VINA_EN/OTG_EN, CRTL, VINB_EN/FLAG, CTRL Low−level input voltage		0		0.4	V
V_{FLGL}	VINB_EN/FLAG Low−level output voltage		0		0.4	V
R_{FLGPUP}	VINB_EN/FLAG pull up resistance			50		kΩ
$R_{MODEPUP}$	MODE pin pull up resistance			100		kΩ
R_{PULDN}	VINA_EN/OTG_EN, CRTL pins pull down resistance			500		kΩ
R_{DIS}	Output Discharge Resistance	During Break before make transition, measured on OUT pin		500		Ω
POWER						
R_{DSONA}	On resistance input VINA	V_{INA} > 4 V		50	80	mΩ
R_{DSONB}	On resistance input VINB	V_{INB} > 4 V		50	80	mΩ
T_{RIN}	Soft Start on both channel	From 10% to 90% of VINA or VINB, CLOAD = 4.7 μF, RLOAD = 500 Ω.			800	μs
T_{ROUT}	Soft Start on both channel	VOUT = 5V. From 10% to 90% of VINA or VINB, CLOAD = 4.7 μF, RLOAD = 500 Ω.			800	μs
I_{RHMX}	Inrush current	Supply on VINA = 5 V or 10 V or VINB = 5 V or 10 V or VOUT = 5 V CLOAD = 4.7 μF, RLOAD = 500 Ω. (Note 6)			800	mA
		Total charge on C_{OUT} during T_{ON} time (Note 6)			50	μC
		Supply on VINA or VINB or VOUT CLOAD = 4.7 μF, RLOAD = 500 Ω. (Note 6)			1	A
T_{ON}	Turn−on time	Slave Mode, from V_{INA_EN} = 1 to V_{OUT} = 90% of V_{INA} or V_{INB_EN} = 1 to V_{OUT} = 90% of V_{INB}.			800	μs
V_{OUTMAX}	VOUT maximum voltage	VINA from 0 V to 28 V in 3 V/μs and COUT = 4.7 μF			17.3	V
		VINB from 0 V to 20 V in 3 V/μs and COUT = 4.7 μF				
		100 V surge holdoff to support IEC 61000−4−5 on VINA. (Note 6)				
CONTROL and TIMING						
T_{DEBINA}	Debounce time for V_{INA} valid	From V_{UVLO} < V_{INA} < V_{OVLO} to V_{INA} enable (excluding soft start)		15		ms
T_{DEBINB}	Debounce time for V_{INB} valid	From V_{UVLO} < V_{INB} < V_{OVLO} to V_{INB} enable (excluding soft start)		1		ms
T_{CRTL}	CRTL pin deglitcher			100		μs
T_{OTG1}	OTG wait time	Autonomous Mode, VINB valid, From VINA_EN/ OTG_EN = 1 to VINA valid (excluding soft start)		10		ms
T_{OTG2}		Autonomous Mode, VINB not valid, From VINA_EN/ OTG_EN = 1 to VINA valid (excluding soft start)		1		ms
T_{BBM}	Break before make time	Autonomous Mode, From VINA valid to VINB valid or from VINB valid to VINA valid		30		ms
INPUT SENSE PIN						
V_{INSDRP}	Voltage Drop VINA – VINA_S	20 mA sink on V_{INA_S}			200	mV
$V_{INSNSMX}$	Max Voltage on VINA_S voltage sense	(Note 6)			20	V
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown	Temperature Rising		150		°C
		Temperature Falling		135		

6. Guaranteed by design and characterization.

Functional Description

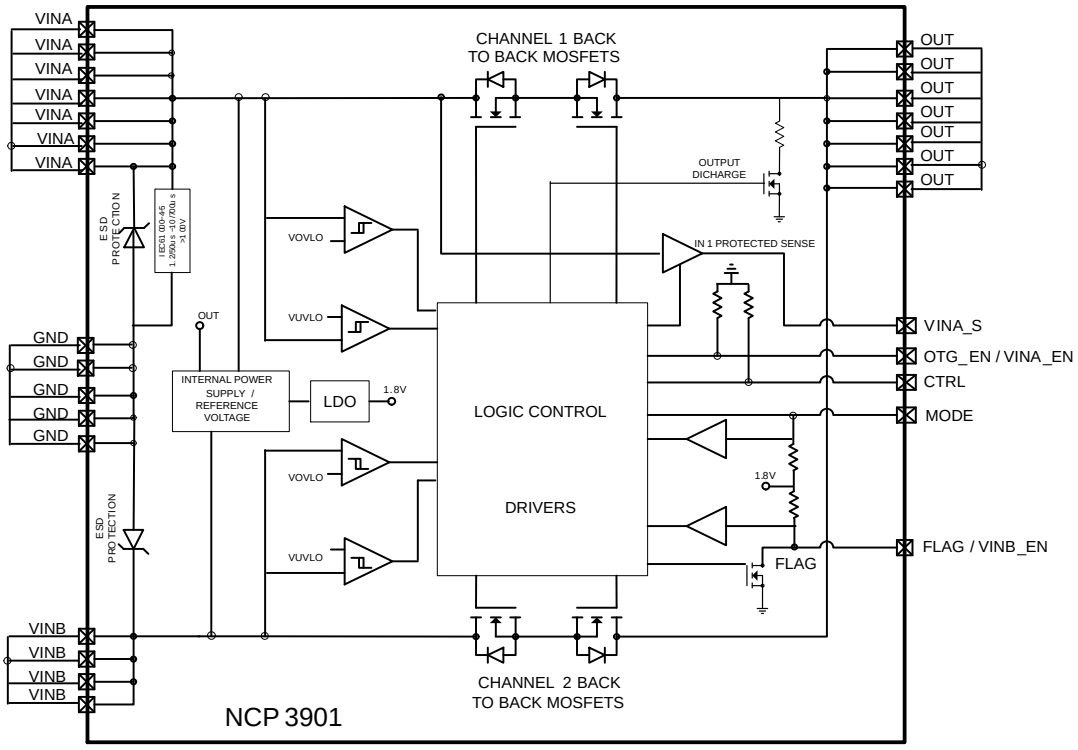


Figure 3. Block Diagram

Overview

The NCP3901 is a 2 to 1 flexible power source selector with arbitration logic. A primary power path (VINA) and secondary power path (VINB) are switched to a single pin (OUT) that provides power to a system (battery charger input).The two inputs (VINA and VINB) are Over Voltage protected. The Over Voltage Threshold is set in such a way that, considering pass MOSFET turn off time, the absolute highest voltage at the OUT pin with a 3 V/µs rising input voltage will be 20 V.

In addition, VINA is connected to an active clamp that protects all downstream circuitry up to a high voltage surge of 100 Vas defined by the IEC61000−4−5 1.2/50 µs and 10/700 µs standard. The IC is protected against reverse voltage applied to the OUT pin on both inputs by use of back to back power MOSFETs.

When a valid voltage is applied to the OUT pin, a digital input VINA_EN/OTG_EN pin will allow this voltage to pass through the power channel 1 from OUT to VINA.

The IC contains a VINB_EN/FLAG input that informs the controlling logic if the secondary channel is conducting or not.The VINB_EN/FLAG pin can also be used as an input signal in order to enable both inputs at the same time.

The IC features a VINA_S protected and current limited output as soon as the VINA voltage is valid (operating range).

Depending on the MODE pin level, the IC will operate in “Autonomous” or “Slave” mode.

- If MODE pin is high the part operates in Slave Mode
- If MODE pin is low the part operates in Autonomous Mode

In Autonomous mode, the CTRL pin will prevent, if pulled high, the part from switching from one input to the other one. MODE digital pin, if pulled high, can also be used to do this.

Finally, a thermal protection will stop the IC when exceeding the TSD threshold. The IC function will be enabled automatically when the part cools down.

Mode Selection

Mode selection to support multiple applications is based on the CTRL and MODE pins, as depicted in the table below. If no external components are connected to the CRTL and MODE pins, the device is configured in slave mode.

MODE Pin	CTRL Pin	PMUX behavior
Low	Low	Autonomous mode – Not Locked
Low	High	Autonomous mode – Locked
High	Low	Slave mode
High	High	

Mode 1 – Slave Mode

In slave mode, the NCP3901 is directly control by the host. The OTG and FLAG pins are respectively assigned to VINA_EN and VINB_EN, directly controlling input channel A and input channel B.

VINA_EN	VINB_EN	Selected Path
Low	Low	None
Low (default)	High (default)	VINB Conducting
High	Low	VINA Conducting
High	High	VINB and VINA Conducting

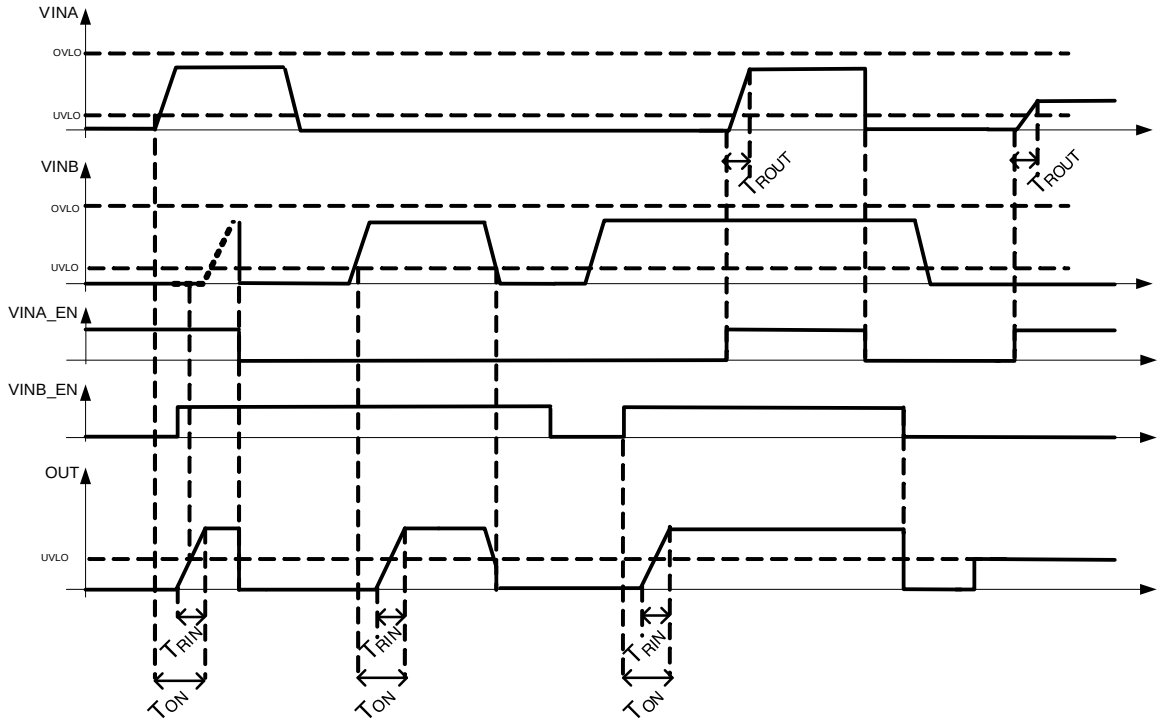


Figure 4. Signal Timing in Slave Mode

Mode 2 – Autonomous Mode

Autonomous Mode − Not Locked

In autonomous not locked mode, the device uses its own logic to determine which input path is conducting and provides information to the system and priority is given to the VINA channel. If a VINA supply is detected valid while VINB is conducting, the PMUX will automatically switch the conducting input from VINB to VINA. During this transition, a break−before−make operation is performed within 30 ms in order to avoid cross conduction between VINA and VINB and to ensure proper operation. A 500 Ω pulldown resistor on OUT is enabled for the entire duration of the break−before−make time. As the PMUX is able to turn on channel VINA or VINB, a FLAG pin indicates to the system the active path. When the VINB path is active, FLAG pin is high. As a consequence, if a valid voltage is present on the OUT pin and if FLAG is low, VINA is active.

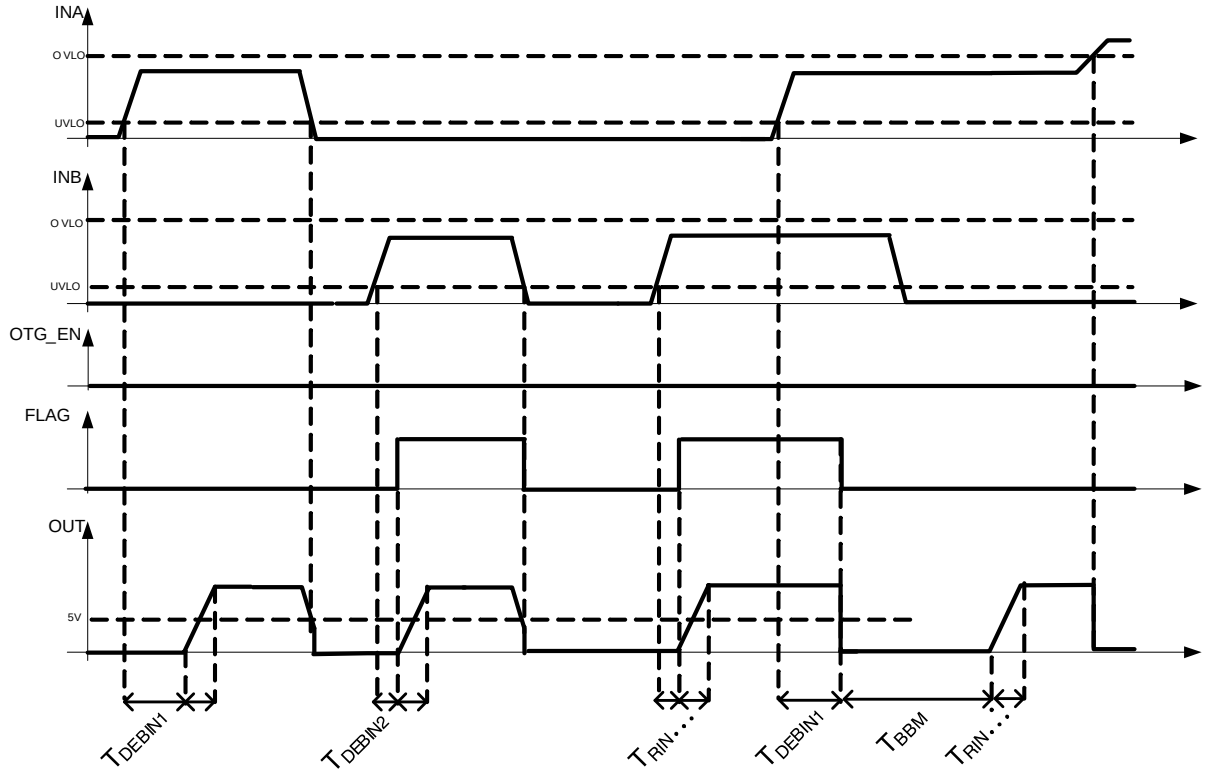


Figure 5. Signal Timing in Autonomous Mode – Charging Example

Autonomous Mode − Locked

Autonomous locked mode is set when the CTRL pin is high. In this mode, the first valid input is active till this input becomes not valid. This feature can be used to lock the VINB channel in case of a weak battery for example.

OTG Mode

5 V is applied on the output of the device during OTG mode. This 5 V will pass through the VINA path when the OTG_EN pin is driven high. When enabling the OTG mode, the VINA output is powered from VOUT and is soft−started for 1 ms.

For VINB to supply the OTG accessory (connected on VINA) though OUT, both channels must be activated. This can be done by asserting the FLAG pin low. Usually used as an output, the FLAG pin is also sensed by the PMUX in autonomous mode. When VINB is valid, the FLAG pin open drain is open. Thus asserting the FLAG pin low will turn on the VINA path with VINB already active.

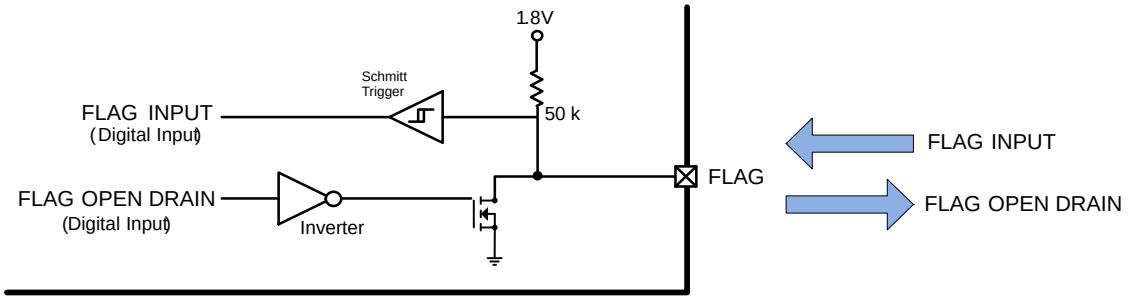


Figure 6. FLAG Functional Diagram

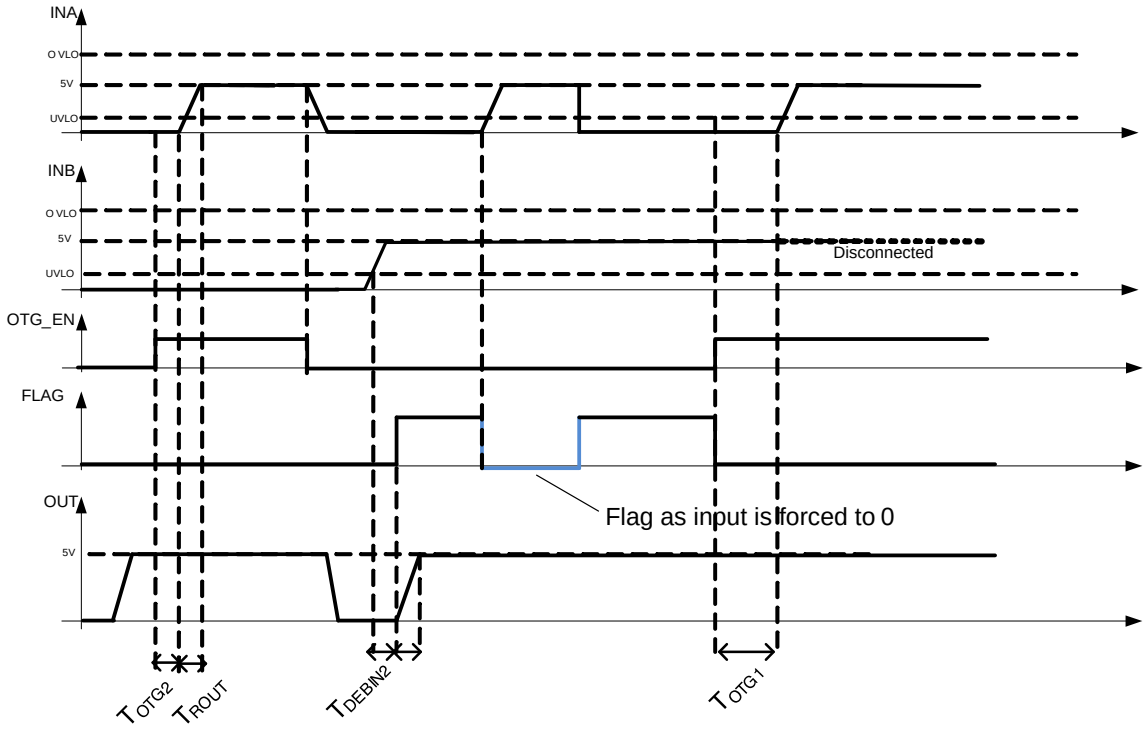


Figure 7. Signal Timing in Autonomous Mode – USB On The Go Example

Autonomous Mode Functional Diagram

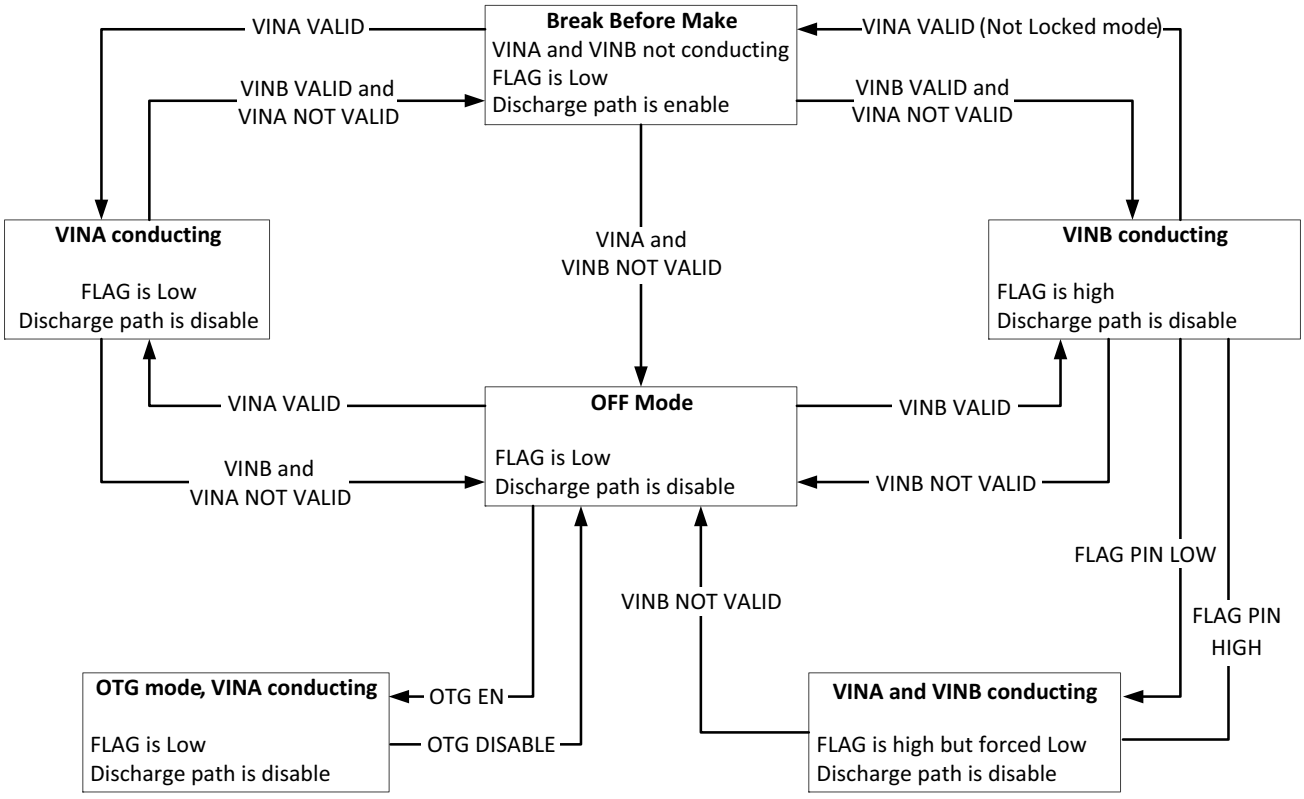


Figure 8. Functional Diagram

VINA Sense Output

The IC features a protected VINA Sense to the processor. This output is 0V when the VINA voltage level is lower than V_{UVLO} and higher than V_{OVLO} and equal to VINA when the VINA voltage is within the operation range.

Input Voltage Protection

The device can withstand a maximum of 28 V DC on VINA and 20 V DC on VINB. Embedded OVP thresholds will disable both VINA and VINB when the voltage applied to VINA or VINB will exceed the OVLO thresholds. The response time of the overvoltage lock out is fast enough to prevent a voltage of maximum of 20 V at VOUT.

In compliance with IEC 61000−4−5, both 1.2/50 μs and 10/700 μs surge waveforms up to 100 V, the PMUX clamp input voltage surges on VINA to 28 V and hold off the voltage. During these surges, the voltage at VOUT will not exceed 20 V.

TYPICAL CHARACTERISTICS

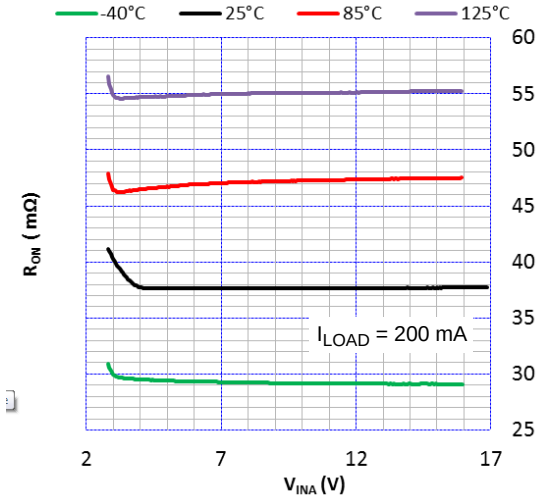


Figure 9. VINA ON Resistance vs. VINA

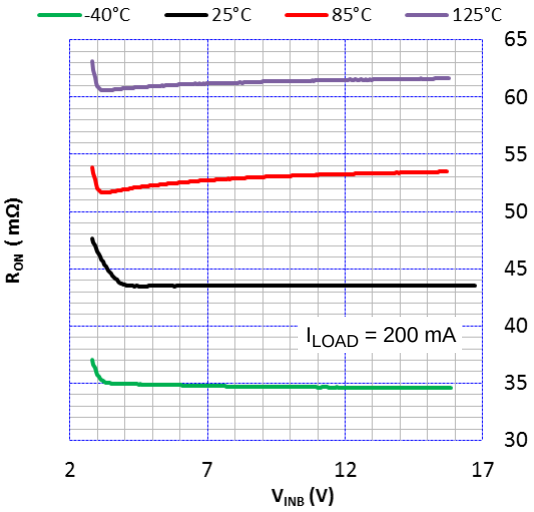


Figure 10. VINB ON Resistance vs. VINB

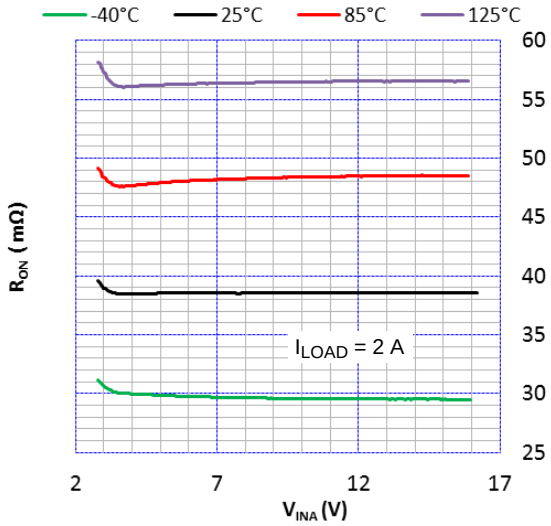


Figure 11. VINA ON Resistance vs. VINA

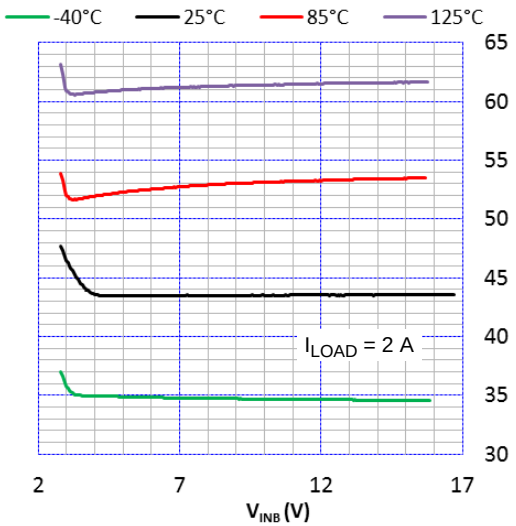


Figure 12. VINB ON Resistance versus VINB

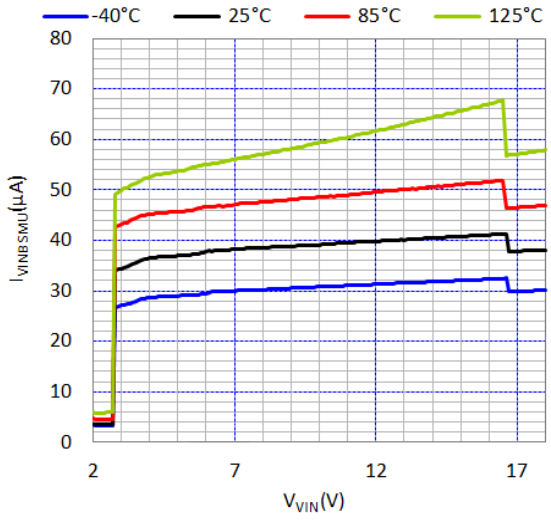


Figure 13. VINA ION vs VINA

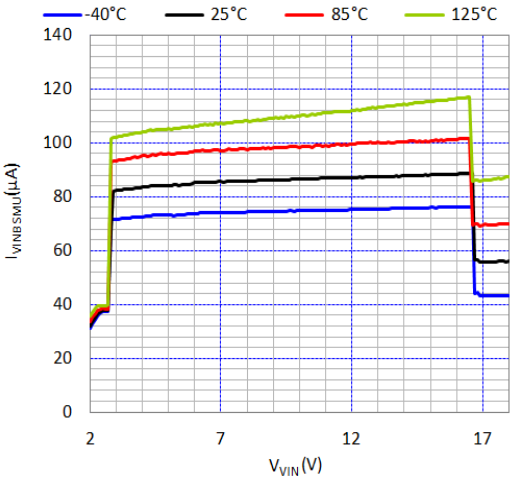


Figure 14. VINB ION vs VINB (including FLAG pull−up)

APPLICATION INFORMATION

Typical Application

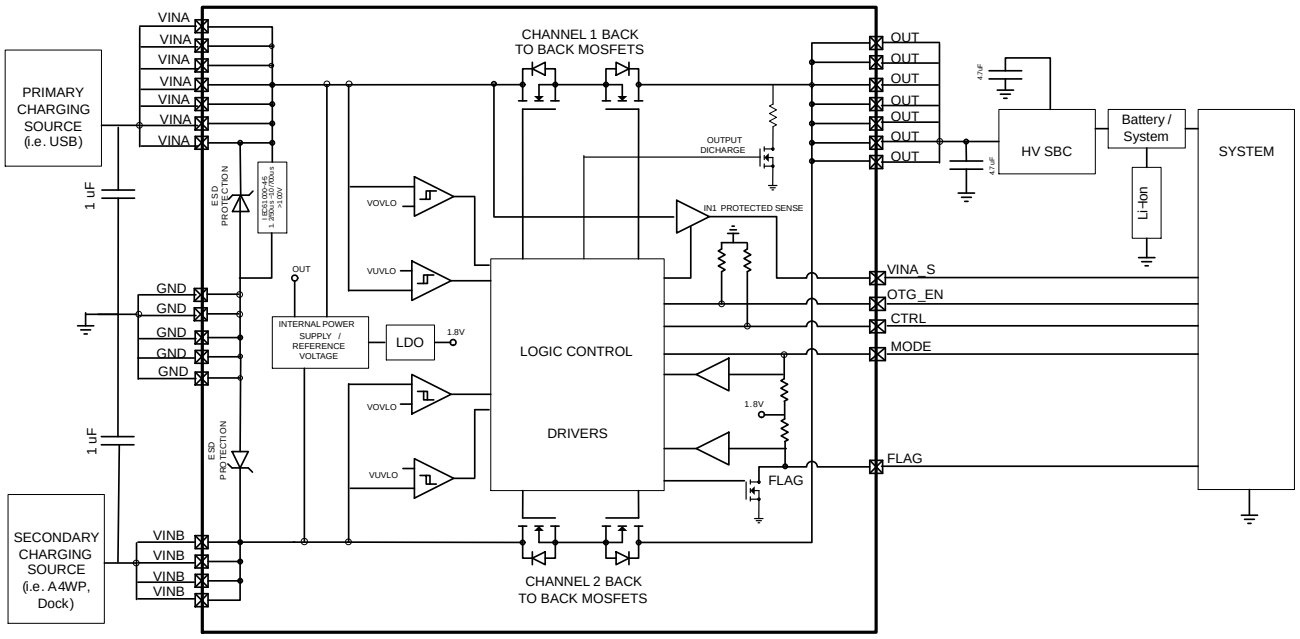


Figure 15. Autonomous Mode

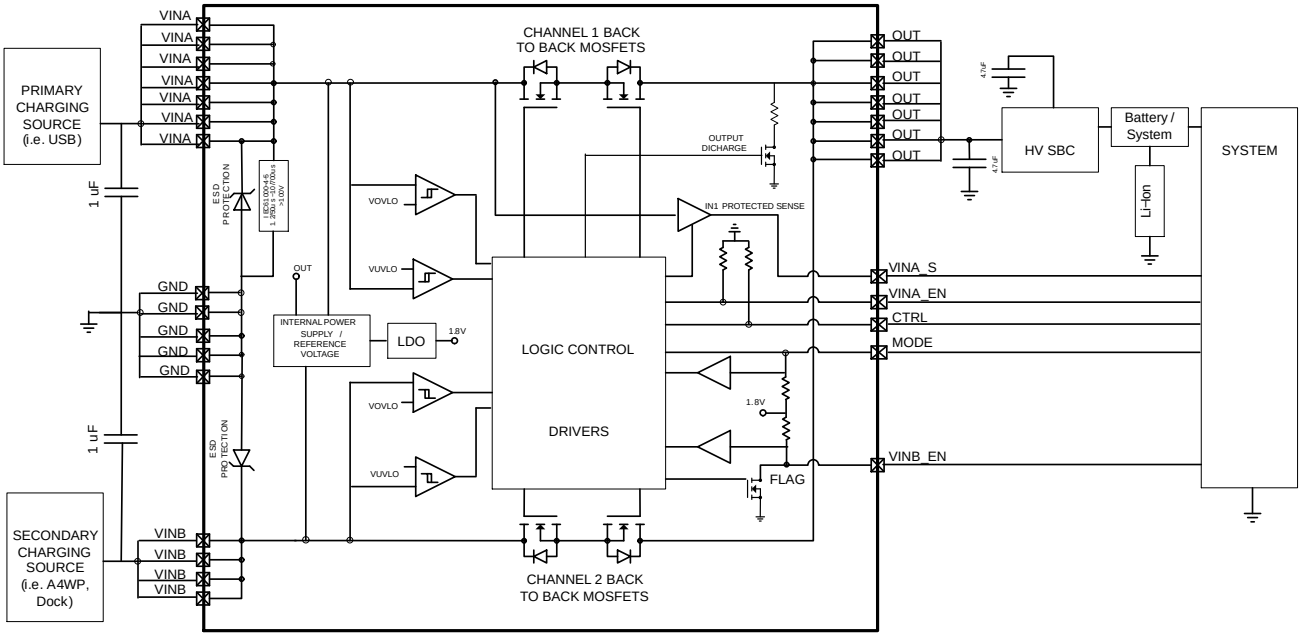


Figure 16. Salve Mode

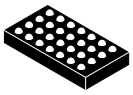
ORDERING INFORMATION

Part Number	Marking Diagram	Shipping†
NCP3901FCCT1G	3901	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

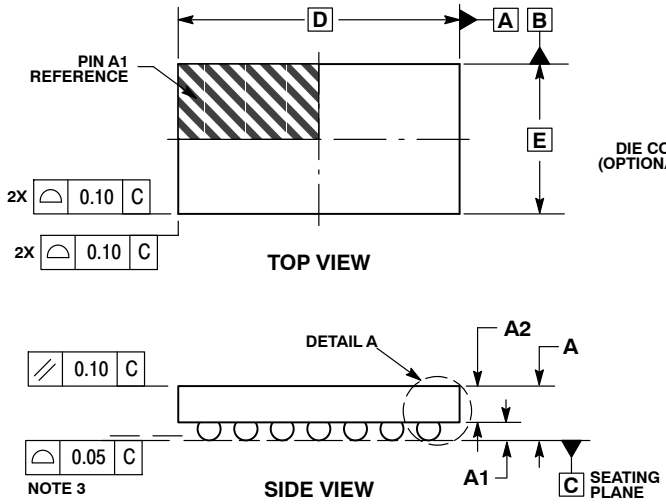
ON Semiconductor®



SCALE 4:1

WLCSP28, 3.1x1.65, 0.4P
CASE 567KR
ISSUE O

DATE 23 SEP 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

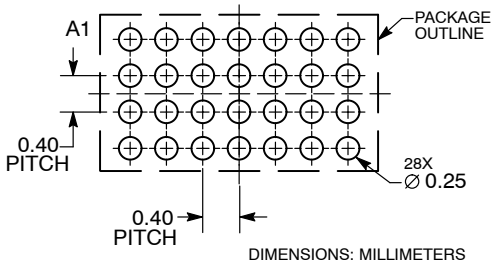
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.33	0.39
A3	0.02	0.04
b	0.24	0.28
D	3.10 BSC	
E	1.65 BSC	
e	0.40 BSC	

GENERIC MARKING DIAGRAM*

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON91880F**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**WLCSP28, 3.1X1.65, 0.4P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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