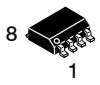
Power Factor Controller for Compact and Robust, Continuous Conduction Mode Pre-Converters

NCP1654



SO−8
D SUFFIX
CASE 751

The NCP1654 is a controller for Continuous Conduction Mode (CCM) Power Factor Correction step−up pre−converters. It controls the power switch conduction time (PWM) in a fixed frequency mode and in dependence on the instantaneous coil current.

Housed in a SO8 package, the circuit minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NCP1654 a driver for robust and compact PFC stages like an effective input power runaway clamping circuitry.

Features

- IEC61000−3−2 Compliant
- Average Current Continuous Conduction Mode
- Fast Transient Response
- Very Few External Components
- Very Low Startup Currents (< 75 μA)
- Very Low Shutdown Currents (< 400 μA)
- Low Operating Consumption
- ±1.5 A Totem Pole Gate Drive
- Accurate Fully Integrated 65/133/200 kHz Oscillator
- Latching PWM for cycle−by−cycle Duty−Cycle Control
- Internally Trimmed Internal Reference
- Undervoltage Lockout with Hysteresis
- Soft−Start for Smoothly Startup Operation
- Shutdown Function
- Pin to Pin Compatible with Industry Standard
- This is a Pb−Free Device

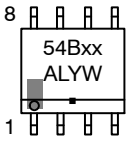
Safety Features

- Inrush Currents Detection
- Overvoltage Protection
- Undervoltage Detection for Open Loop Detection or Shutdown
- Brown−Out Detection
- Soft−Start
- Accurate Overcurrent Limitation
- Overpower Limitation

Typical Applications

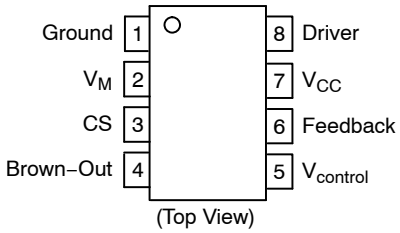
- Flat TVs, PC Desktops
- AC Adapters
- White Goods, other Off−line SMPS

MARKING DIAGRAM



xx	= 65, 133 or 200
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1654BD65R2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCP1654BD133R2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCP1654BD200R2G	SO−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
DRV	8	Output Drive Capability − Source Output Drive Capability − Sink	−1.5 +1.5	A
V_{CC}	7	Power Supply Voltage, V_{CC} pin, continuous voltage	−0.3, +20	V
	7	Transient Power Supply Voltage, duration < 10 ms, IV_{CC} < 10 mA	+25	V
Vin	2, 3, 4, 5, 6	Input Voltage	−0.3, +10	V
$P_D(SO)$ $R_{\theta JA}(SO)$		Power Dissipation and Thermal Characteristics D suffix, Plastic Package, Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction−to−Air	 450 178	 mW °C/W
T_J		Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}		Maximum Junction Temperature	150	°C
T_{Smax}		Storage Temperature Range	−65 to +150	°C
T_{Lmax}		Lead Temperature (Soldering, 10 s)	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) 2000 V per JEDEC standard JESD22, Method A114E
   Machine Model (MM) 200 V (except pin#7 which complies 150 V) per JEDEC standard JESD22, Method A115A.
2. This device contains Latch−up Protection and exceeds ±100 mA per JEDEC Standard JESD78.

TYPICAL ELECTRICAL CHARACTERISTICS TABLE (V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 3)

Symbol	Rating	Min	Typ	Max	Unit
GATE DRIVE SECTION					
R_{OH}	Source Resistance @ I_{source} = 100 mA	−	9.0	20	Ω
R_{OL}	Sink Resistance @ I_{sink} = −100 mA	−	6.6	18	Ω
T_r	Gate Drive Voltage Rise Time from 1.5 V to 13.5 V (C_L = 2.2 nF)	−	60	−	ns
T_f	Gate Drive Voltage Fall Time from 13.5 V to 1.5 V (C_L = 2.2 nF)	−	40	−	ns
REGULATION BLOCK					
V_{REF}	Voltage Reference	2.425	2.5	2.575	V
I_{EA}	Error Amplifier Current Capability	−	±28	−	μA
G_{EA}	Error Amplifier Gain	100	200	300	μS
$I_B$pin6	Pin 6 Bias Current @ V_{FB} = V_{REF}	−500	−	500	nA
$V_{control}$ $V_{control(max)}$ $V_{control(min)}$ $\Delta V_{control}$	Pin5 Voltage Maximum Control Voltage @ V_{FB} = 2 V Minimum Control Voltage @ V_{FB} = 3 V $\Delta V_{control}$ = $V_{control(max)}$ − $V_{control(min)}$	 − − 2.7	 3.6 0.6 3.0	 − − 3.3	V
$V_{OUT}L$ / V_{REF}	Ratio (V_{OUT} Low Detect Thresold / V_{REF})	94	95	96	%
$H_{OUT}L$ / V_{REF}	Ratio (V_{OUT} Low Detect Hysteresis / V_{REF})	−	0.5	−	%
I_{BOOST}	Pin 5 Source Current when (V_{OUT} Low Detect) is activated	190	228	260	μA
CURRENT SENSE BLOCK					
V_S	Current Sense Pin Offset Voltage, (I_{CS} = 100 μA)	−	10	−	mV
$I_{S(OCP)}$	Overcurrent Protection Threshold	185	200	215	μA
POWER LIMITATION BLOCK					
I_{CS} x V_{BO}	Overpower Limitation Threshold	−	200	−	μVA
$I_{CS(OPL1)}$ $I_{CS(OPL2)}$	Overpower Current Threshold (V_{BO} = 0.9 V, V_M = 3 V) Overpower Current Threshold (V_{BO} = 2.67 V, V_M = 3 V)	186 62	222 75	308 110	μA
PWM BLOCK					
Dcycle	Duty Cycle Range	−	0−97	−	%

TYPICAL ELECTRICAL CHARACTERISTICS TABLE (V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 3)

Symbol	Rating	Min	Typ	Max	Unit
OSCILLATOR / RAMP GENERATOR BLOCK					
fsw	Switching Frequency				kHz
	65 kHz	58	65	72	
	133 kHz	120	133	146	
	200 kHz	180	200	220	
BROWN−OUT DETECTION BLOCK					
V_{BOH}	Brown−Out Voltage Threshold (rising)	1.22	1.30	1.38	V
V_{BOL}	Brown−Out Voltage Threshold (falling)	0.65	0.7	0.75	V
I_{IB}	Pin 4 Input Bias Current @ V_{BO} = 1 V	−500	−	500	nA
CURRENT MODULATION BLOCK					
I_{M1}	Multiplier Output Current ($V_{control} = V_{control(max)}$, V_{BO} = 0.9 V, I_{CS} = 25 μA)	−	1.9	−	μA
I_{M2}	Multiplier Output Current ($V_{control} = V_{control(max)}$, V_{BO} = 0.9 V, I_{CS} = 75 μA)				
	(@ 0 ∼ 125°C)	1.5	4.7	8.8	
	(@ −40 ∼ 125°C)	1.5	4.7	9.8	
I_{M3}	Multiplier Output Current ($V_{control} = V_{control(min)}$ + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 25 μA	−	28.1	−	
I_{M4}	Multiplier Output Current ($V_{control} = V_{control(min)}$ + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 75 μA	−	84.4	−	
OVERVOLTAGE PROTECTION					
V_{OVP} / V_{REF}	Ratio (Overvoltage Threshold / V_{REF})	103	105	107	%
T_{OVP}	Propagation Delay (V_{FB} − 107% V_{REF}) to Drive Low	−	500	−	ns
UNDERVOLTAGE PROTECTION / SHUTDOWN					
$V_{UVP(on)}/V_{REF}$	UVP Activate Threshold Ratio (T_J = 0°C to +105°C)	4	8	12	%
$V_{UVP(off)}/V_{REF}$	UVP Deactivate Threshold Ratio (T_J = 0°C to +105°C)	6	12	18	%
$V_{UVP(H)}$	UVP Lockout Hysteresis	−	4	−	%
T_{UVP}	Propagation Delay (V_{FB} < 8% V_{REF}) to Drive Low	−	500	−	ns
THERMAL SHUTDOWN					
T_{SD}	Thermal Shutdown Threshold	150	−	−	°C
H_{SD}	Thermal Shutdown Hysteresis	−	30	−	°C
V_{CC} UNDERVOLTAGE LOCKOUT SECTION					
$V_{CC(on)}$	Start−Up Threshold (Undervoltage Lockout Threshold, V_{CC} rising)	9.6	10.5	11.4	V
$V_{CC(off)}$	Disable Voltage after Turn−On (Undervoltage Lockout Threshold, V_{CC} falling)	8.25	9.0	9.75	V
$V_{CC(H)}$	Undervoltage Lockout Hysteresis	1.0	1.5	−	V
DEVICE CONSUMPTION					
	Power Supply Current:				
I_{STUP}	Start−Up (@ V_{CC} = 9.4 V)	−	−	75	μA
I_{CC1}	Operating (@ V_{CC} = 15 V, no load, no switching)	−	3.7	5.0	mA
I_{CC2}	Operating (@ V_{CC} = 15 V, no load, switching)	−	4.7	6.0	mA
I_{STDN}	Shutdown Mode (@ V_{CC} = 15 V and V_{FB} = 0 V)	−	300	400	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

NOTE: $$I_M = \frac{I_{cs} \times V_{BO}}{4 \times \left(V_{control} - V_{control(min)}\right)}$$

DETAILED PIN DESCRIPTIONS

Pin	Sym-bol	Name	Function
1	GND	Ground	–
2	V_{in}	Multiplier Voltage	This pin provides a voltage V_M for the PFC duty cycle modulation. The input impedance of the PFC circuits is proportional to the resistor R_M externally connected to this pin. The device operates in average current mode if an external capacitor C_M is connected to the pin. Otherwise, it operates in peak current mode.
3	CS	Current Sense Input	This pin sources a current I_{CS} which is proportional to the inductor current I_L. The sense current I_{CS} is for overcurrent protection (OCP), overpower limitation (OPL) and PFC duty cycle modulation. When I_{CS} goes above 200 μA, OCP is activated and the Drive Output is disabled.
4	V_{BO}	Brown−Out / In	Connect a resistor network among the rectified input voltage, BO pin, and ground. And connect a capacitor between BO pin and ground. BO pin detects a voltage signal proportional to the average input voltage. When V_{BO} goes below V_{BOL}, the circuit that detects too low input voltage conditions (brown−out), turns off the output driver and keeps it in low state until V_{BO} exceeds V_{BOH}. This signal which is proportional to the RMS input voltage V_{ac} is also for overpower limitation (OPL) and PFC duty cycle modulation.
5	$V_{control}$	Control Voltage / Soft−Start	The voltage of this pin $V_{control}$ directly controls the input impedance. This pin is connected to external type−2 compensation components to limit the $V_{control}$ bandwidth typically below 20 Hz to achieve near unity power factor. The device provides no output when $V_{control} < V_{control(min)}$. When it starts operation, the power increases slowly (soft−start).
6	V_{FB}	Feed−Back / Shutdown	This pin receives a feedback signal V_{FB} that is proportional to the PFC circuits output voltage. This information is used for both the output regulation, the overvoltage protection (OVP), and output undervoltage protection (UVP) to protect the system from damage at feedback abnormal situation. When V_{FB} goes above 105% V_{REF}, OVP is activated and the Drive Output is disabled. When V_{FB} goes below 8% V_{REF}, the device enters a low−consumption shutdown mode.
7	V_{CC}	Supply Voltage	This pin is the positive supply of the IC. The circuit typically starts to operate when V_{CC} exceeds 10.5 V and turns off when V_{CC} goes below 9 V. After start−up, the operating range is 9 V up to 20 V.
8	DRV	Drive Output	The high current capability of the totem pole gate drive (±1.5 A) makes it suitable to effectively drive high gate charge power MOSFET.

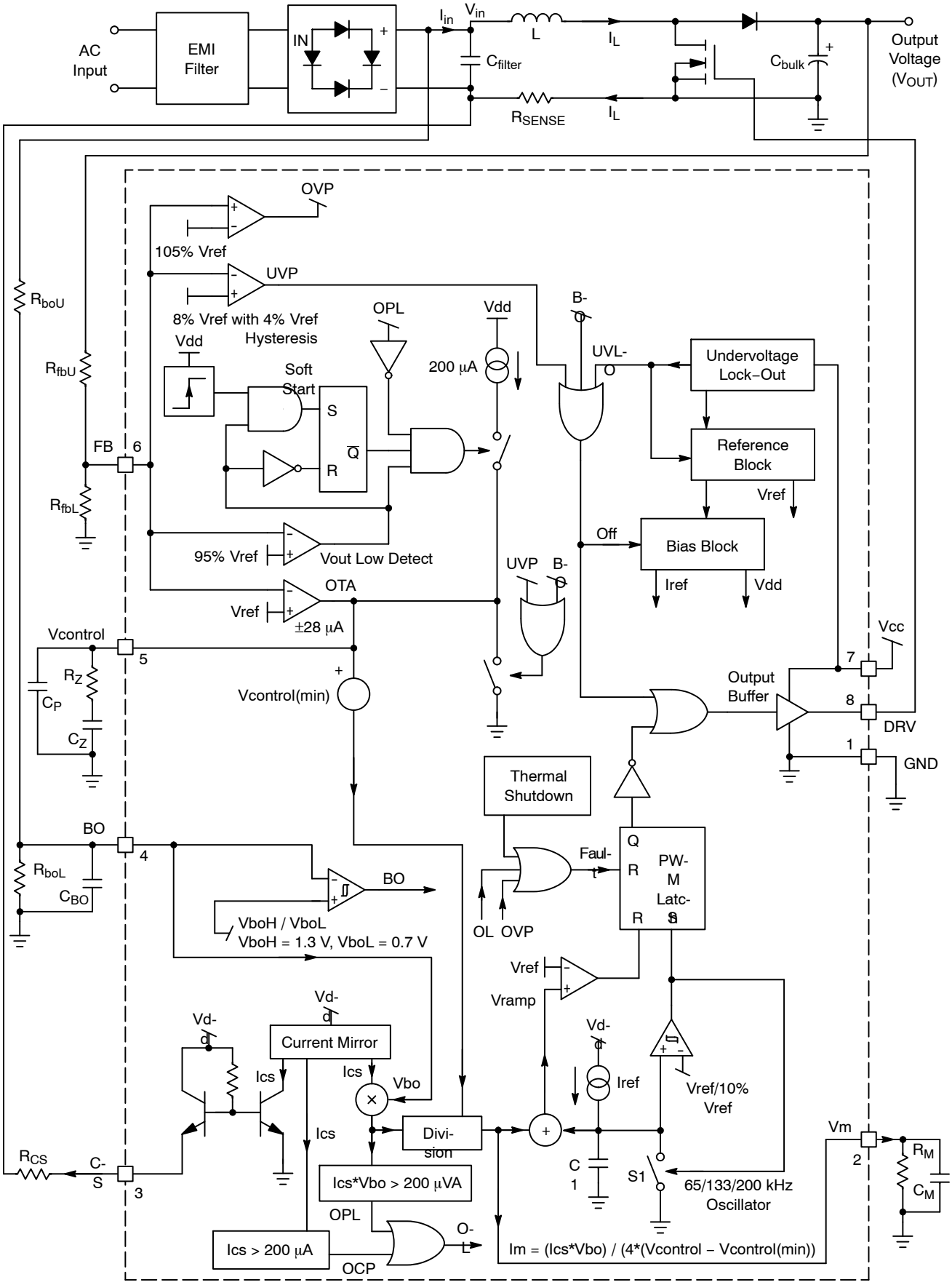


Figure 1. Functional Block Diagram

TYPICAL CHARACTERISTICS

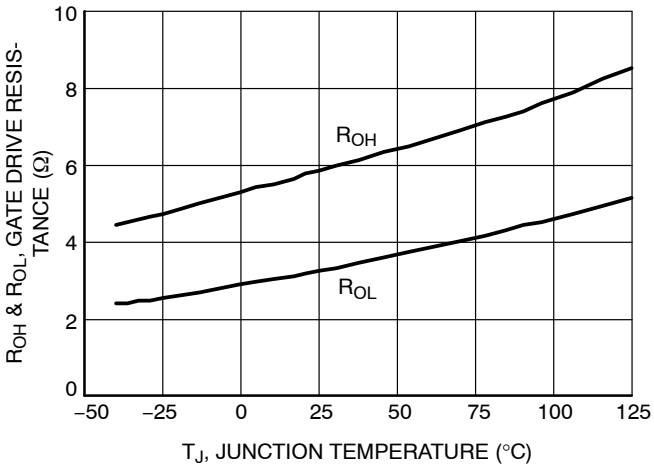


Figure 2. Gate Drive Resistance vs. Temperature

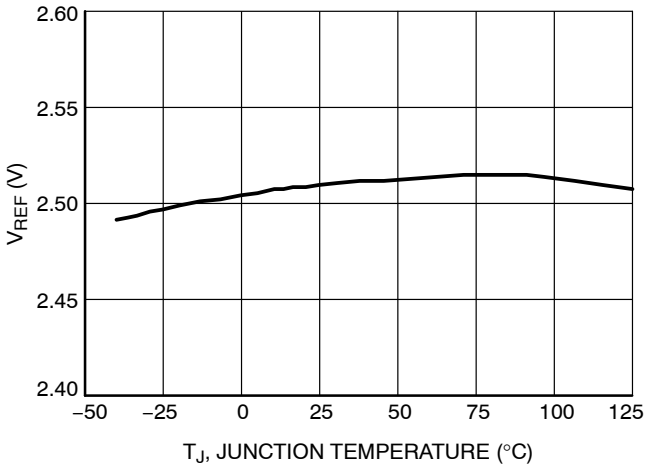


Figure 3. Reference Voltage vs. Temperature

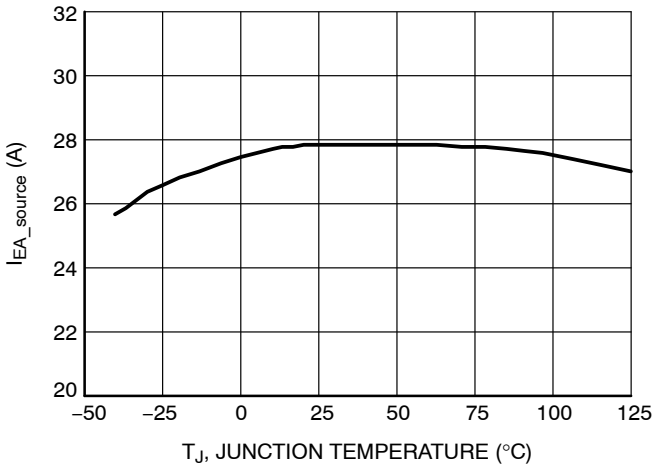


Figure 4. Source Current Capability of the Error Amplifier vs. Temperature

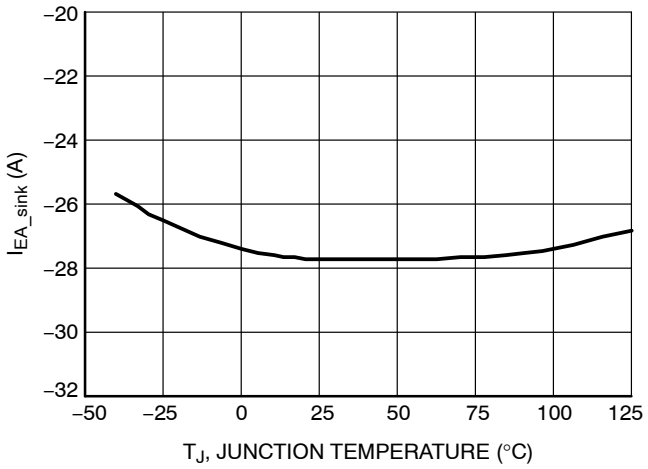


Figure 5. Sink Current Capability of the Error Amplifier vs. Temperature

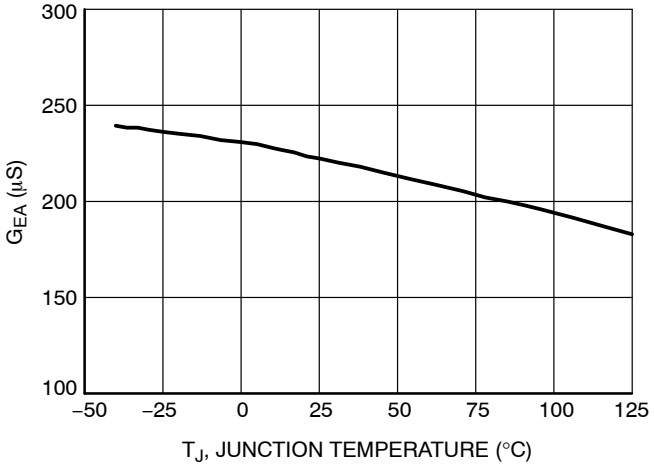


Figure 6. Error Amplifier Gain vs. Temperature

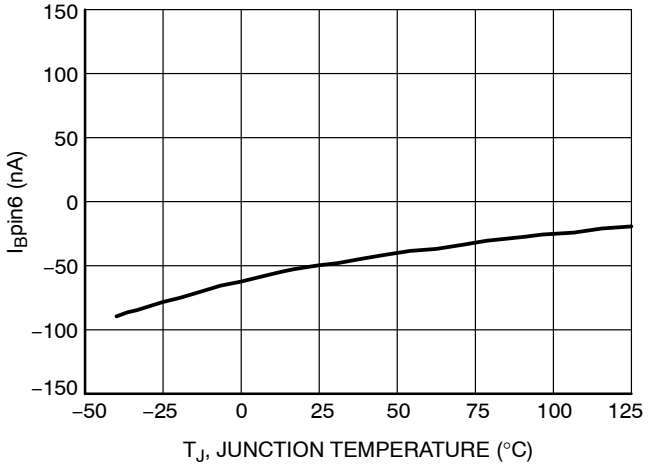


Figure 7. Feedback Pin Current vs. Temperature (@V_{fb} = V_{REF})

TYPICAL CHARACTERISTICS

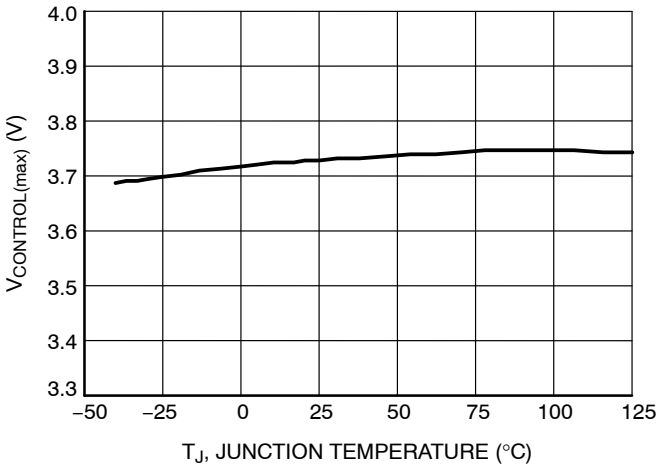


Figure 8. $V_{control}$ Maximum Voltage vs. Temperature

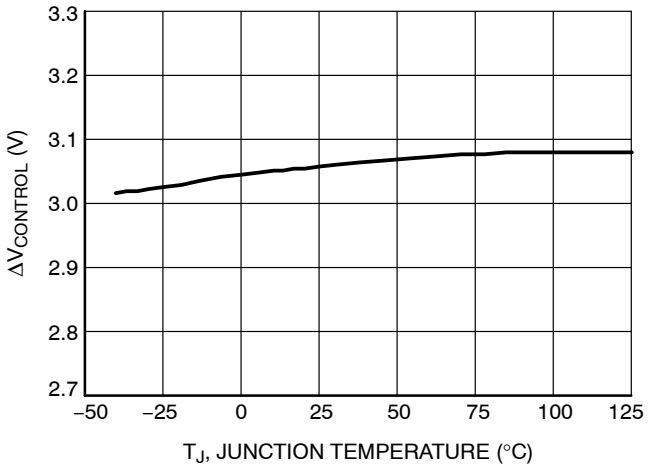


Figure 9. $V_{control}$ Maximum Swing ($\Delta V_{CONTROL}$) vs. Temperature

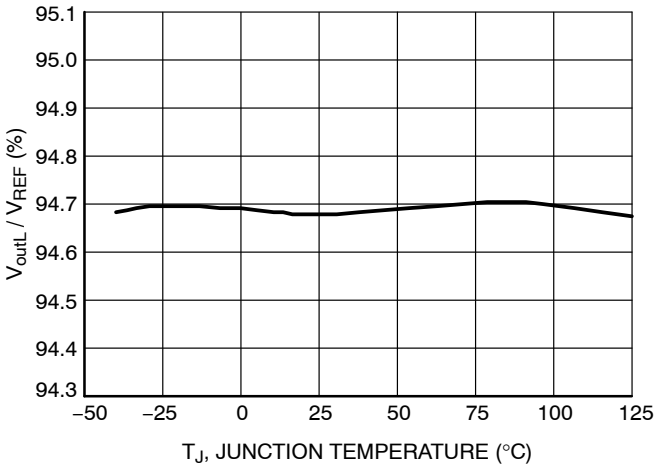


Figure 10. Ratio (V_{OUT} Low Detect Threshold / V_{REF}) vs. Temperature

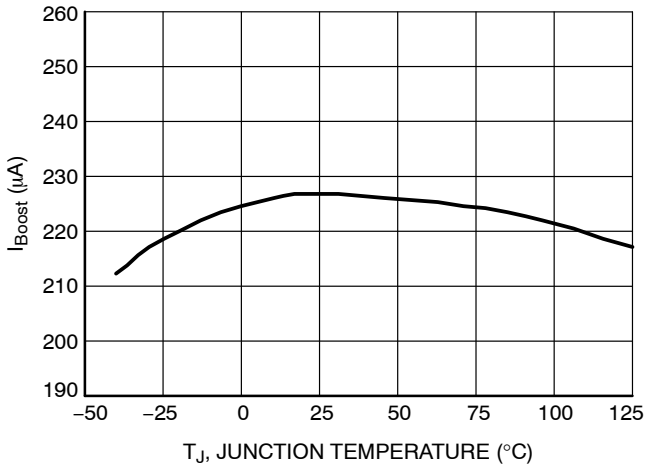


Figure 11. Pin 5 Source Current when (V_{OUT} Low Detect) is Activated vs. Temperature

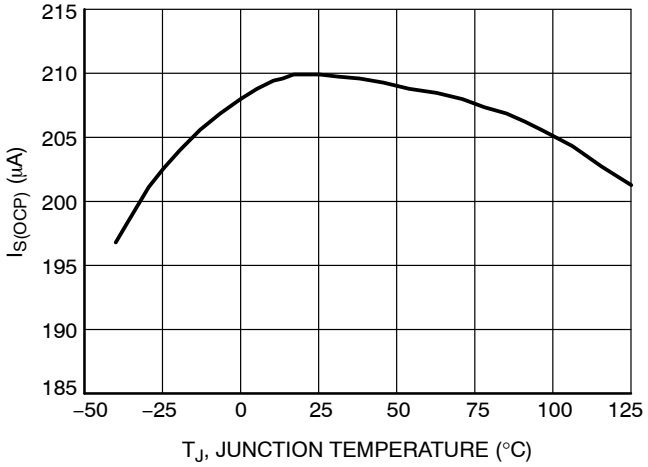


Figure 12. Over−Current Protection Threshold vs. Temperature

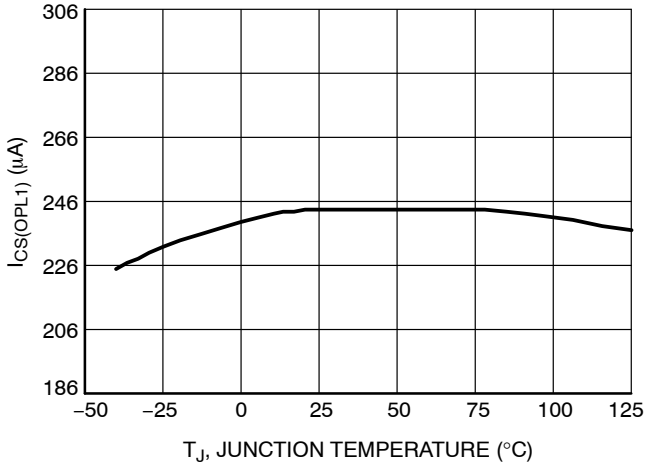


Figure 13. Over−Power Current Threshold (@V_{BO} = 0.9 V & V_m = 3 V) vs. Temperature

TYPICAL CHARACTERISTICS

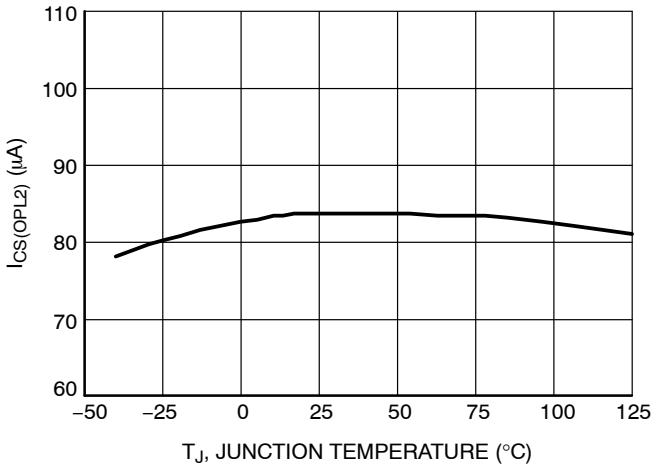


Figure 14. Over−Power Current Threshold (@V_{BO} = 2.67 V & V_m = 3 V) vs. Temperature

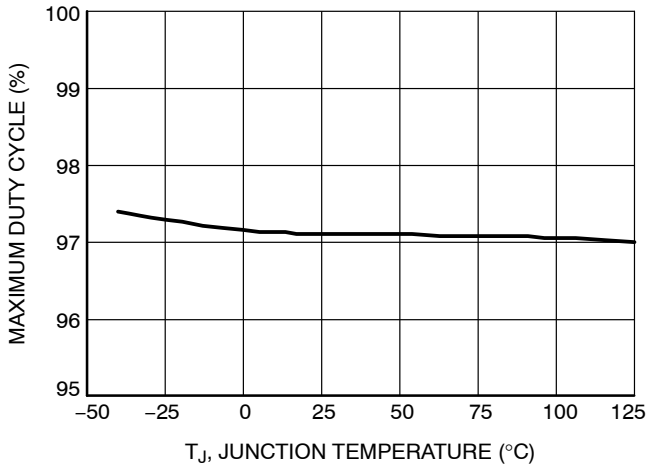


Figure 15. Maximum Duty Cycle vs. Temperature

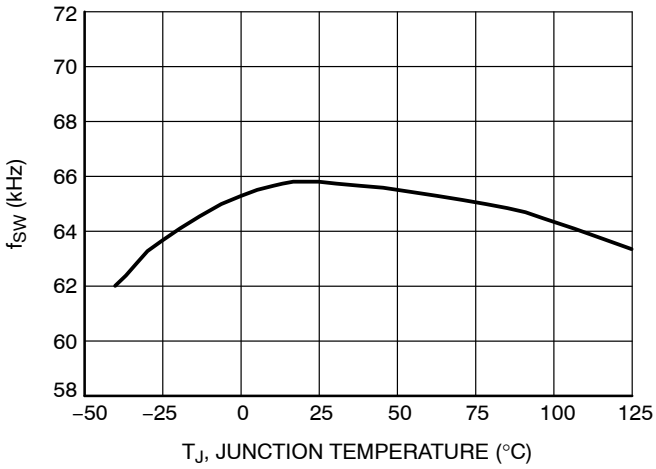


Figure 16. Switching Frequency vs. Temperature (65 kHz Version)

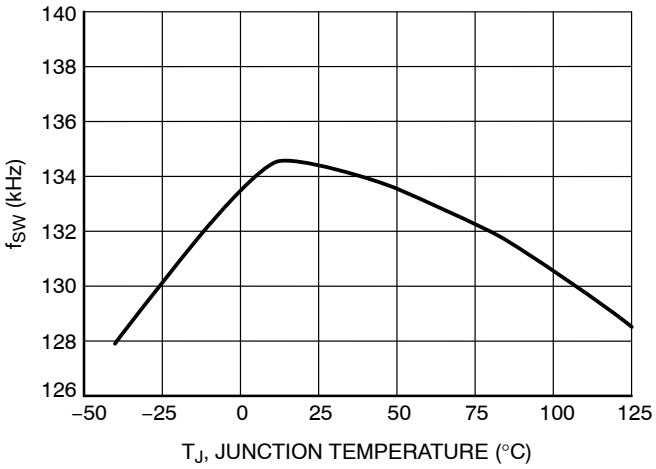


Figure 17. Switching Frequency vs. Temperature (133 kHz Version)

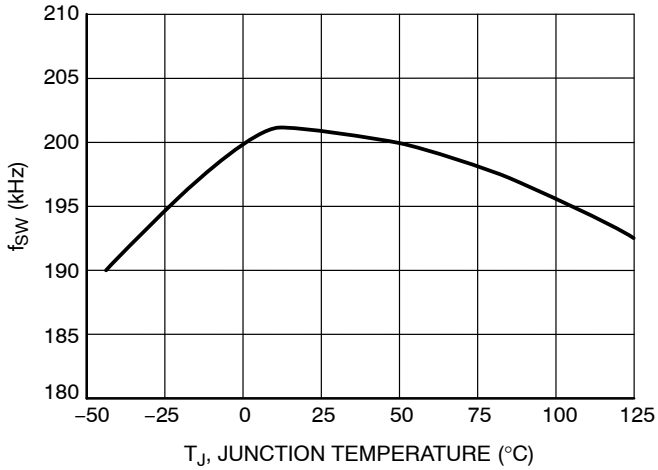


Figure 18. Switching Frequency vs. Temperature (200 kHz Version)

TYPICAL CHARACTERISTICS

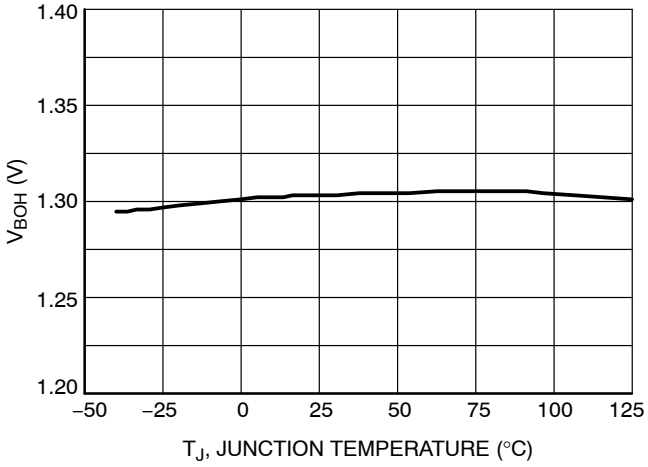


Figure 19. Brown−Out Voltage Threshold (Rising) vs. Temperature

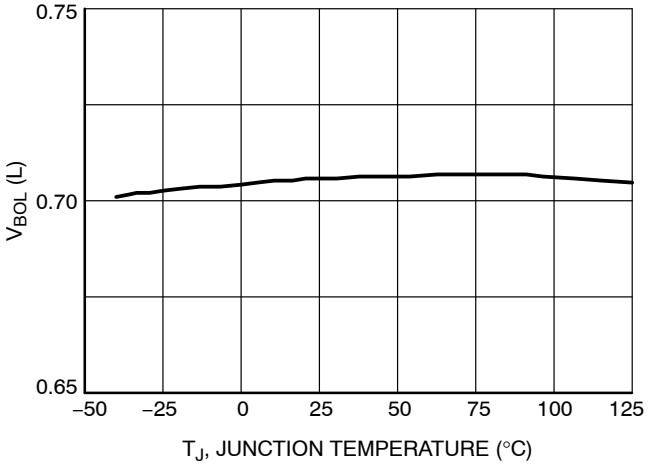


Figure 20. Brown−Out Voltage Threshold (Falling) vs. Temperature

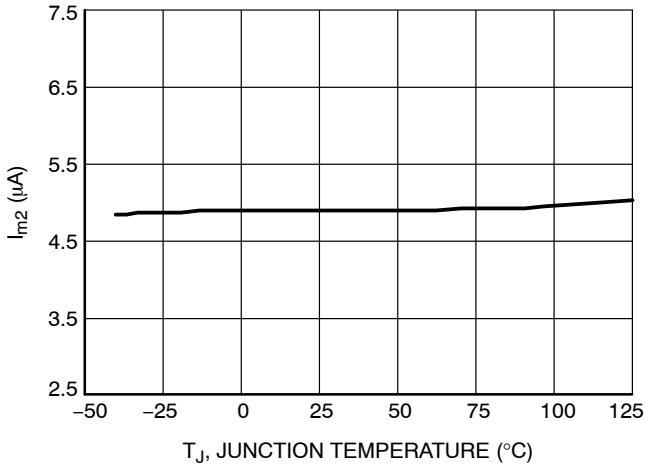


Figure 21. Multiplier Output Current ($V_{control}$ = $V_{CONTROL(max)}$, V_{bo} = 0.9 V, I_{CS} = 75 μA) vs. Temperature

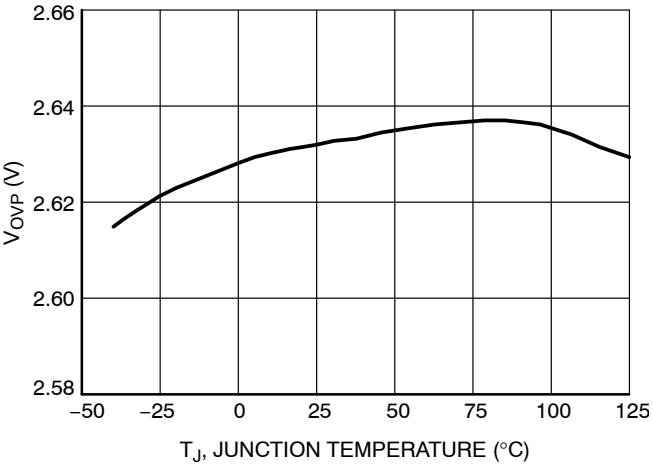


Figure 22. Over Voltage Threshold vs. Temperature

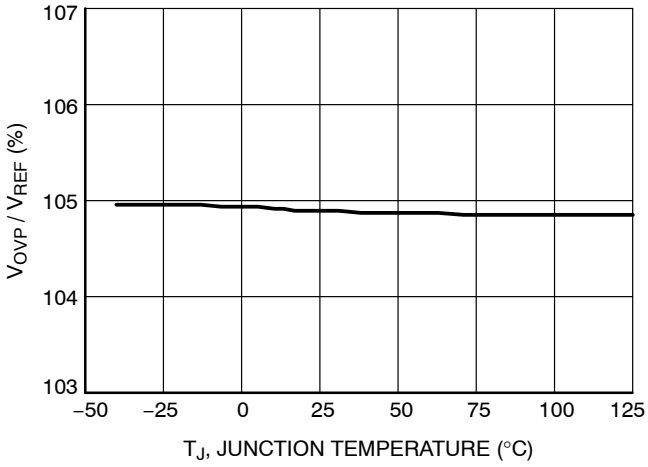


Figure 23. Ratio (Over Voltage Threshold / V_{REF}) vs. Temperature

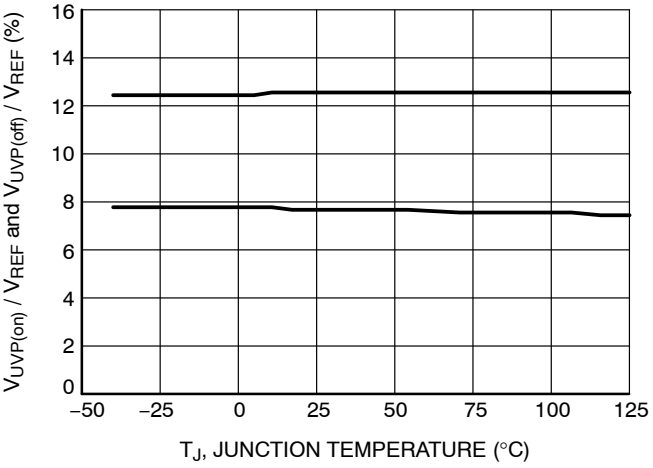


Figure 24. UVP Activate and Deactivate Threshold Ratio vs. Temperature

TYPICAL CHARACTERISTICS

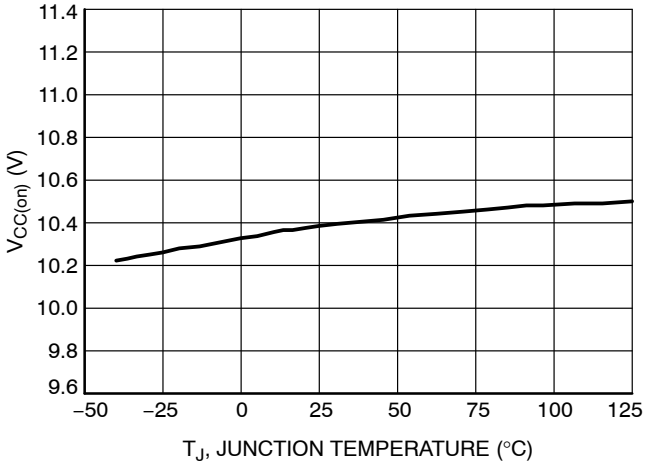


Figure 25. V_{CC} Start−Up Threshold (V_{CC} Rising) vs. Temperature

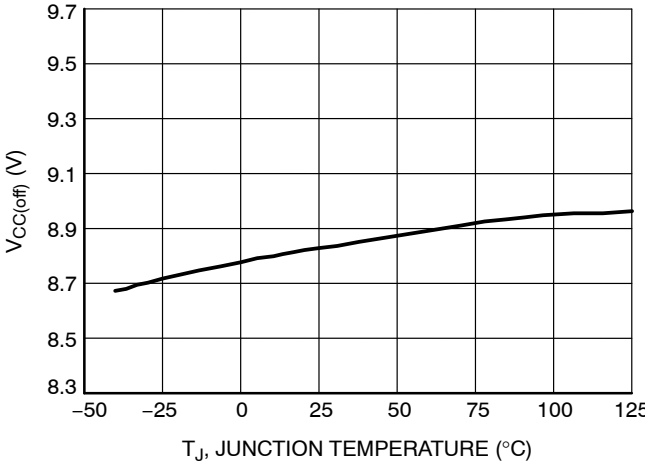


Figure 26. V_{CC} Disable Voltage after Turn−On (V_{CC} Falling) vs. Temperature

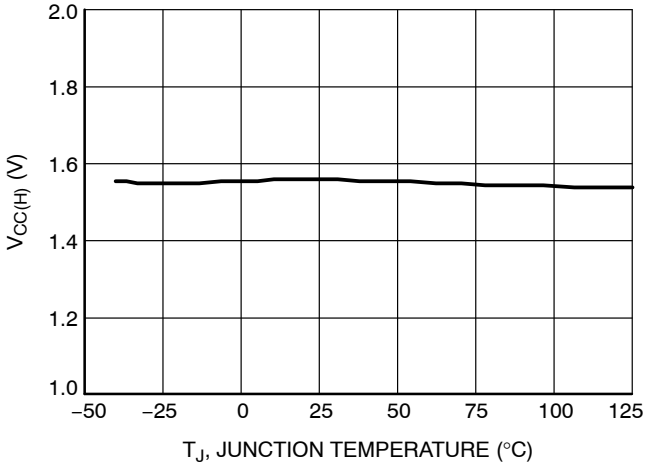


Figure 27. V_{CC} UVLO Hysteresis vs. Temperature

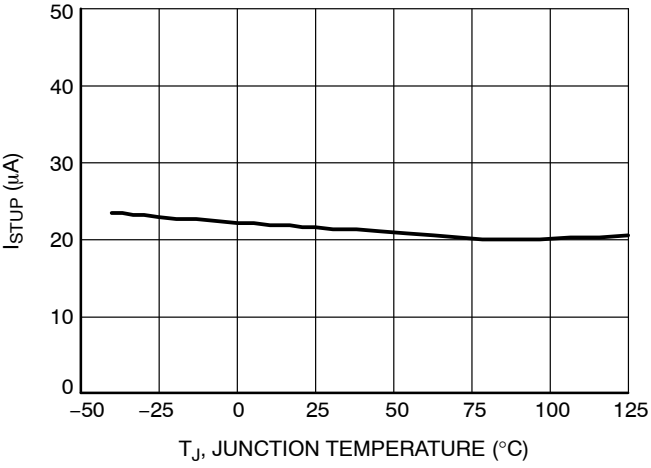


Figure 28. Supply Current in Startup Mode vs. Temperature

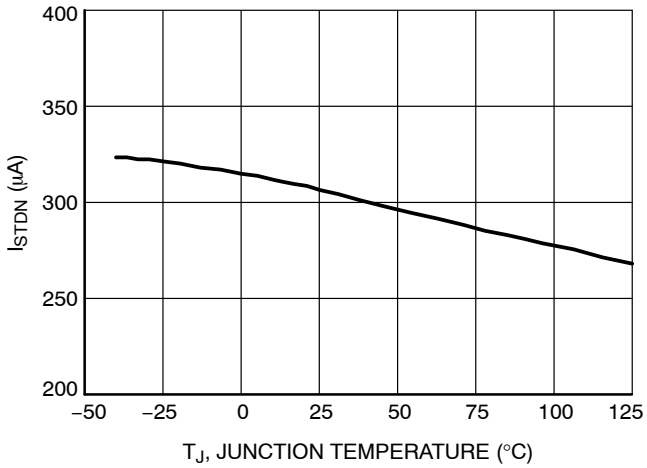


Figure 29. Supply Current in Shutdown Mode vs. Temperature

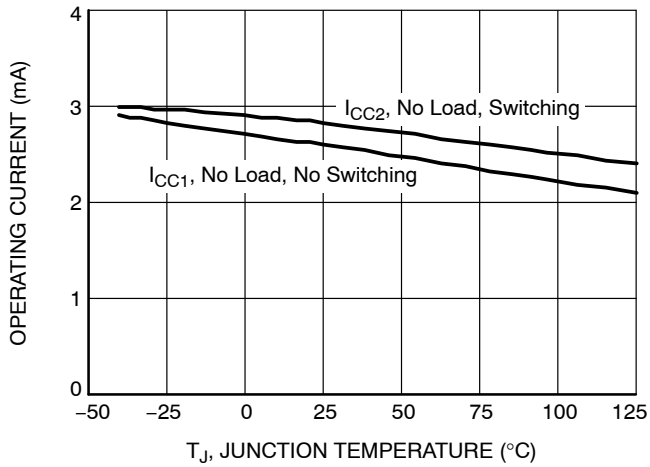


Figure 30. Operating Supply Current vs. Temperature

Detailed Operating Description

Introduction

The NCP1654 is a PFC driver designed to operate in fixed frequency, continuous conduction mode. The fixed frequency operation eases the compliance with EMI standard and the limitation of the possible radiated noise that may pollute surrounding systems. In addition, continuous conduction operation reduces the application di/dt and their resulting interference. More generally, the NCP1654 is an ideal candidate in systems where cost−effectiveness, reliability and high power factor are the key parameters. It incorporates all the necessary features to build a compact and rugged PFC stage:

- **Compactness and Flexibility:** housed in a SO8 package, the NCP1654 requires a minimum of external components. In particular, the circuit scheme simplifies the PFC stage design and eliminates the need for any input voltage sensing. In addition, the circuit offers some functions like the Brown−Out or the true power limiting that enable the optimizations of the PFC design,
- **Low Consumption and Shutdown Capability:** the NCP1654 is optimized to exhibit consumption as small as possible in all operation modes. The consumed current is particularly reduced during the start−up phase and in shutdown mode so that the PFC stage power losses are extremely minimized when the circuit is disabled. This feature helps meet the more stringent stand−by low power specifications. Just ground the Feed−back pin to force the NCP1654 in shutdown mode,
- **Safety Protections:** the NCP1654 permanently monitors the output voltage, the coil current and the die temperature to protect the system from possible over−stresses. Integrated protections (Overvoltage protection, coil current limitation, thermal shutdown...) make the PFC stage extremely robust and reliable:
  - *Maximum Current Limit:* the circuit permanently senses the coil current and immediately turns off the power switch if it is higher than the set current limit. The NCP1654 also prevents any turn on of the power switch as long as the coil current is not below its maximum permissible level. This feature protects the MOSFET from possible excessive stress that could result from the switching of a current higher than the one the power switch is dimensioned for. In particular, this scheme effectively protects the PFC stage during the start−up phase when large in−rush currents charge the output capacitor.
  - *Undervoltage Protection for Open Loop Protection or Shut−down:* the circuit detects when the feed−back voltage goes below than about 8% of the regulation level. In this case, the circuit turns off and its consumption drops to a very low value. This feature protects the PFC stage from starting operation in case of low AC line conditions or in case of a failure in the feed−back network (i.e. bad connection).
  - *Fast Transient Response:* given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over or under−shoots because of abrupt load or input voltage variations (e.g. at start up). If the output voltage is too far from the regulation level:

    Overvoltage Protection: NCP1654 turns off the power switch as soon as V_{out} exceeds the OVP threshold (105% of the regulation level). Hence a cost & size effective bulk capacitor of lower voltage rating is suitable for this application,

    Dynamic Response Enhancer: NCP1654 drastically speeds up the regulation loop by its internal 200 μA enhanced current source when the output voltage is below 95% of its regulation level.
  - *Brown−Out Detection:* the circuit detects low AC line conditions and disables the PFC stage in this case. This protection mainly protects the power switch from the excessive stress that could damage it in such conditions,
  - *Over−Power Limitation:* the NCP1654 computes the maximum permissible current in dependence of the average input voltage measured by the brown−out block. It is the second OCP with a threshold that is line dependent. When the circuit detects an excessive power transfer, it resets the driver output immediately,
  - *Thermal Shutdown:* an internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 120°C (30°C hysteresis),
  - *Soft Start:* $V_{control}$ is pulled low brown−out detection activates, or Undervoltage protection activates, and no drive is provided.

    At start up, the “200 μA enhanced current source” is disabled. So there is only 28 μA to charge the compensation components, and makes $V_{control}$ raise gradually. This is to obtain a slow increasing duty cycle and hence reduce the voltage and current stress on the MOSFET. Hence it provides a soft−start feature.
- **Output Stage Totem Pole:** the NCP1654 incorporates a ±1.5A gate driver to efficiently drive TO220 or TO247 power MOSFETs.

PRINCIPLE OF NCP1654 SCHEME

CCM PFC Boost

A CCM PFC boost converter is shown in Figure 31. The input voltage is a rectified 50 ro 60 Hz sinusoidal signal. The MOSFET is switching at a high frequency (typically 65/133/200 kHz in NCP1654) so that the inductor current I_L basically consists of high and low−frequency components.

Filter capacitor C_{filter} is an essential and very small value capacitor in order to eliminate the high−frequency component of the inductor I_L. This filter capacitor cannot be too bulky because it can pollute the power factor by distorting the rectified sinusoidal input voltage.

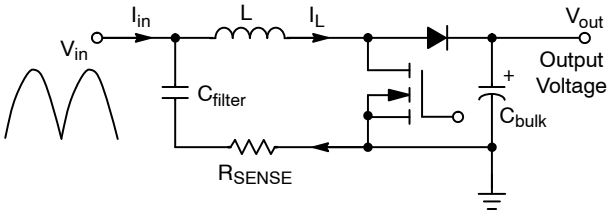


Figure 31. CCM PFC Boost Converter

PFC Methodology

The NCP1654 uses a proprietary PFC methodology particularly designed for CCM operation. The PFC methodology is described in this section.

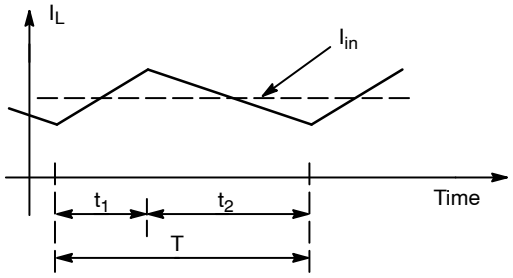


Figure 32. Inductor Current in CCM

As shown in Figure 32, the inductor current I_L in a switching period T includes a charging phase for duration t_1 and a discharging phase for duration t_2. The voltage conversion ratio is obtained in (Equation 1).

$$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2} = \frac{T}{T - t_1}$$

$$V_{in} = \frac{T - t_1}{T} V_{out} \qquad \text{(eq. 1)}$$

where

V_{out} is the output voltage of PFC stage,

V_{in} is the rectified input voltage,

T is the switching period,

t_1 is the MOSFET on time, and

t_2 is the MOSFET off time.

The input filter capacitor C_{filter} and the front−ended EMI filter absorbs the high−frequency component of inductor current I_L. It makes the input current I_{in} a low−frequency signal only of the inductor current.

$$I_{in} = I_{L-50} \qquad \text{(eq. 2)}$$

where

I_{in} is the input AC current.

I_L is the inductor current.

I_{L-50} supposes a 50 Hz operation. The suffix 50 means it is with a 50 Hz bandwidth of the original I_L.

From (Equation 1) and (Equation 2), the input impedance Z_{in} is formulated.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{T - t_1}{T} \frac{V_{out}}{I_{L-50}} \qquad \text{(eq. 3)}$$

where Z_{in} is input impedance.

Power factor is corrected when the input impedance Z_{in} in (Equation 3) is constant or varies slowly in the 50 or 60 Hz bandwidth.

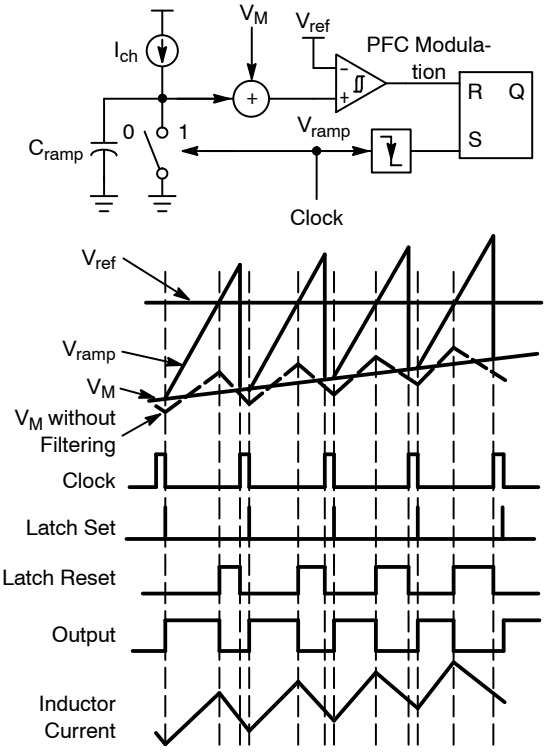


Figure 33. PFC Duty Modulation and Timing Diagram

The PFC modulation and timing diagram is shown in Figure 33. The MOSFET on time t_1 is generated by the intersection of reference voltage V_{REF} and ramp voltage V_{ramp}. A relationship in (Equation 4) is obtained.

$$V_{ramp} = V_m + \frac{I_{ch} t_1}{C_{ramp}} = V_{REF} \qquad \text{(eq. 4)}$$

where

V_{ramp} is the internal ramp voltage, the positive input of the PFC modulation comparator,

V_m is the multiplier voltage appearing on V_m pin,

I_{ch} is the internal charging current,

C_{ramp} is the internal ramp capacitor, and

V_{REF} is the internal reference voltage, the negative input of the PFC modulation comparator.

I_{ch}, C_{ramp}, and V_{REF} also act as the ramp signal of switching frequency. Hence the charging current I_{ch} is specially designed as in (Equation 5). The multiplier voltage V_m is therefore expressed in terms of t_1 in (Equation 6).

$$I_{ch} = \frac{C_{ramp} V_{REF}}{T} \quad \text{(eq. 5)}$$

$$V_m = V_{REF} - \frac{t_1}{C_{ramp}} \frac{C_{ramp} V_{REF}}{T} = V_{REF} \frac{T - t_1}{T} \quad \text{(eq. 6)}$$

From (Equation 3) and (Equation 6), the input impedance Z_{in} is re−formulated in (Equation 7).

$$Z_{in} = \frac{V_m}{V_{REF}} \frac{V_{out}}{I_{L-50}} \quad \text{(eq. 7)}$$

Because V_{REF} and V_{out} are roughly constant versus time, the multiplier voltage V_m is designed to be proportional to the I_{L-50} in order to have a constant Z_{in} for PFC purpose. It is illustrated in Figure 34.

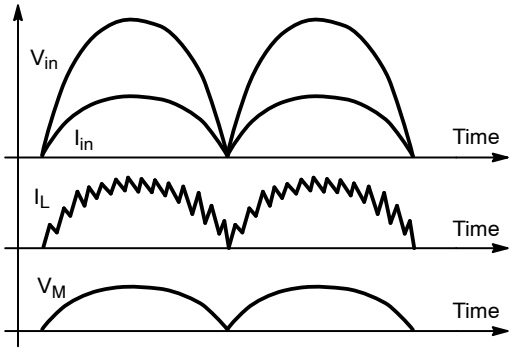


Figure 34. Multiplier Voltage Timing Diagram

It can be seen in the timing diagram in Figure 33 that V_m originally consists of a switching frequency ripple coming from the inductor current I_L. The duty ratio can be inaccurately generated due to this ripple. This modulation is the so−called “peak current mode”. Hence, an external capacitor C_M connected to the multiplier voltage V_m pin is essential to bypass the high−frequency component of V_m. The modulation becomes the so−called “average current mode” with a better accuracy for PFC.

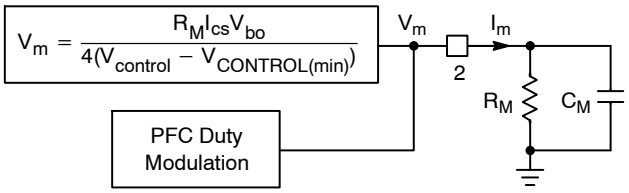


Figure 35. External Connection on the Multiplier Voltage Pin

The multiplier voltage V_m is generated according to (Equation 8).

$$V_m = \frac{R_M I_{cs} V_{bo}}{4(V_{control} - V_{CONTROL(min)})} \quad \text{(eq. 8)}$$

Where,

R_M is the external multiplier resistor connected to V_m pin, which is constant.

V_{bo} is the input voltage signal appearing on the BO pin, which is proportional to the rms input voltage,

I_{cs} is the sense current proportional to the inductor current I_L as described in (Equation 11).

$V_{control}$ is the control voltage signal, the output voltage of Operational Trans−conductance Amplifier (OTA), as described in (Equation 12).

R_M directly limits the maximum input power capability and hence its value affects the NCP1654 to operate in either “follower boost mode” or “constant output voltage mode”.

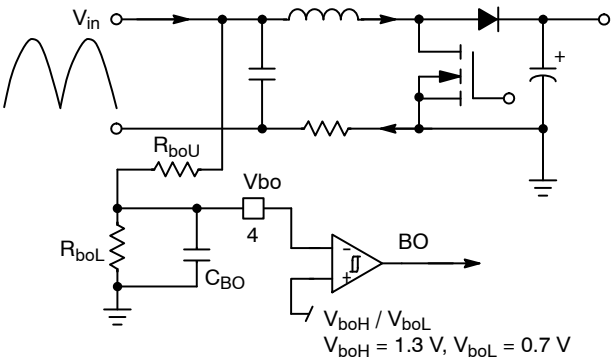


Figure 36. External Connection on the Brown Out Pin

Refer to Figure 36,

$$V_{bo} = K_{BO}(V_{in}) = K_{BO} \cdot \frac{2\sqrt{2}}{\pi} V_{ac} \quad \text{(eq. 9)}$$

$$K_{BO} = \frac{R_{boL}}{R_{boU} + R_{boL}} \quad \text{(eq. 10)}$$

where

V_{bo} is the voltage on BO pin.

K_{BO} is the decay ratio of V_{in} to V_{bo}.

$<V_{in}>$ is the average voltage signal of V_{in}, the voltage appearing on C_{filter}.

V_{ac} is the RMS input voltage.

R_{boL} is low side resistor of the dividing resistors between V_{in} and BO pin.

R_{boU} is upper side resistor of the dividing resistors between V_{in} and BO pin.

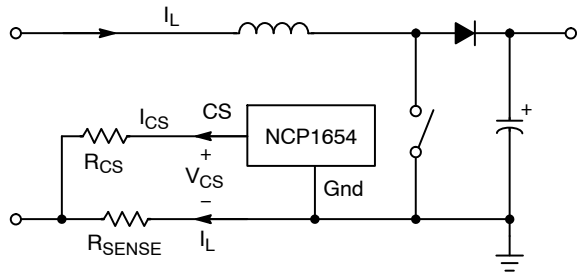


Figure 37. Current Sensing

Refer to Figure 37, sense current I_{cs} is proportional to the inductor current I_L as described in (Equation 11). I_L consists of the high−frequency component (that depends on di/dt or inductor L) and low−frequency component (that is I_{L-50}).

$$I_{cs} = \frac{R_{SENSE}}{R_{CS}} I_L \qquad \text{(eq. 11)}$$

where

R_{SENSE} is the sense resistor to sense I_L.

R_{CS} is the offset resistor between CS pin and R_{SENSE}.

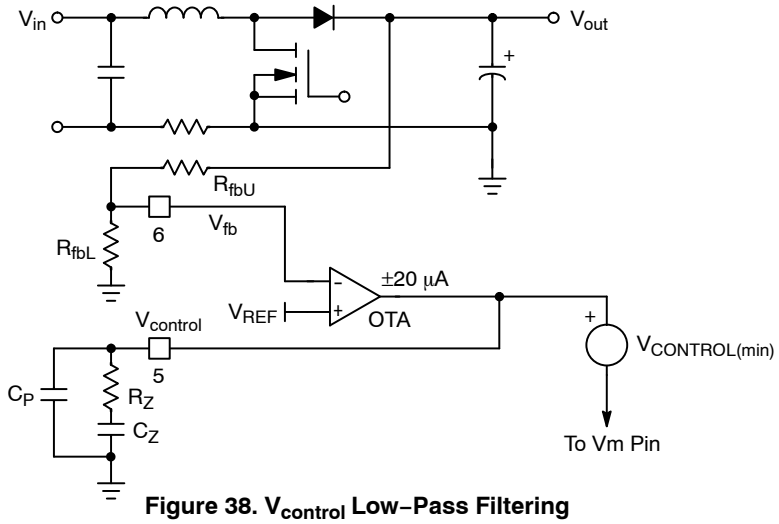


Figure 38. $V_{control}$ Low−Pass Filtering

Refer to Figure 38, the Operational Trans−conductance Amplifier (OTA) senses V_{out} via the feedback resistor dividers, R_{fbU} and R_{fbL}. The OTA constructs a control voltage, $V_{control}$, depending on the output power and hence V_{out}. The operating range of $V_{control}$ is from $V_{CONTROL(min)}$ to $V_{CONTROL(max)}$. The signal used for PFC duty modulation is after decreasing a offset voltage, $V_{CONTROL(min)}$, i.e. $V_{control}-V_{CONTROL(min)}$.

This control current $I_{control}$ is a roughly constant current that comes from the PFC output voltage V_{out} that is a slowly varying signal. The bandwidth of $I_{control}$ can be additionally limited by inserting the external type−2 compensation components (that are R_Z, C_Z, and C_P as shown in Figure 38). It is recommended to limit $f_{control}$, that is the bandwidth of $V_{control}$ (or $I_{control}$), below 20 Hz typically to achieve power factor correction purpose.

The transformer of V_{out} to $V_{control}$ is as described in (Equation 12) if C_Z is >> C_P. G_{EA} is the error amplifier gain.

$$\frac{V_{control}}{V_{out}} = \frac{R_{fbL} \cdot G_{EA} R_Z}{R_{fbL} + R_{fbU}} \cdot \frac{1 + sR_ZC_Z}{sR_ZC_Z(1 + sR_ZC_P)} \qquad \text{(eq. 12)}$$

From (Equation 7) − (Equation 11), the input impedance Z_{in} is re−formulated in (Equation 13).

$$Z_{in} = \frac{\sqrt{2}\, R_M R_{SENSE} V_{out} V_{ac} K_{BO} I_L}{2\pi R_{CS} \cdot (V_{control} - V_{CONTROL(min)}) \cdot V_{REF} I_{L-50}} \qquad \text{(eq. 13)}$$

When I_L is equal to I_{L-50}, (Equation 13) is re−formulated in (Equation 14)

$$Z_{in} = \frac{\sqrt{2}\, R_M R_{SENSE} V_{out} V_{ac} K_{BO}}{2\pi R_{CS} \cdot (V_{control} - V_{CONTROL(min)}) \cdot V_{REF}} \qquad \text{(eq. 14)}$$

The multiplier capacitor C_M is the one to filter the high−frequency component of the multiplier voltage V_m. The high−frequency component is basically coming from the inductor current I_L. On the other hand, the filter capacitor C_{filter} similarly removes the high−frequency component of inductor current I_L. If the capacitors C_M and C_{filter} match with each other in terms of filtering capability, I_L becomes I_{L-50}. Input impedance Z_{in} is roughly constant over the bandwidth of 50 or 60 Hz and power factor is corrected.

Input and output power (P_{in} and P_{out}) are derived in (Equation 15) when the circuit efficiency η is obtained or assumed. The variable V_{ac} stands for the rms input voltage.

$$P_{in} = \frac{V_{ac}^2}{Z_{in}} = \frac{2\pi R_{CS} \cdot (V_{control} - V_{CONTROL(min)}) \cdot V_{REF} \cdot V_{ac}}{\sqrt{2} R_M R_{SENSE} V_{out} K_{BO}} \quad \text{(eq. 15)}$$

$$\propto \frac{(V_{control} - V_{CONTROL(min)}) V_{ac}}{V_{out}}$$

$$P_{out} = \eta P_{in} = \eta \frac{2\pi R_{CS} \cdot (V_{control} - V_{CONTROL(min)}) \cdot V_{REF} \cdot V_{ac}}{\sqrt{2} R_M R_{SENSE} V_{out} K_{BO}} \quad \text{(eq. 16)}$$

$$\propto \frac{(V_{control} - V_{CONTROL(min)}) V_{ac}}{V_{out}}$$

Follower Boost

The "Follower Boost" is an operation mode where the pre−converter output voltage stabilizes at a level that varies linearly versus the ac line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (*refer to MC33260 data sheet for more details at http://www.onsemi.com*).

The NCP1654 operates in follower boost mode when $V_{control}$ is constant, i.e. $V_{control}$ raises to its maximum value $V_{CONTROL(max)}$. Re−formulate (Equation 16) to become (Equation 17) and (Equation 18) by replace $V_{control}$ by $V_{CONTROL(max)}$. If $V_{control}$ is constant based on (Equation 15), for a constant load or power demand the output voltage V_{out} of the converter is proportional to the rms input voltage V_{ac}. It means the output voltage V_{out} becomes lower when the rms input voltage V_{ac} becomes lower. On the other hand, the output voltage V_{out} becomes lower when the load or power demand becomes higher.

$$P_{out} = \eta \frac{2\pi R_{CS} \cdot (V_{CONTROL(max)} - V_{CONTROL(min)}) \cdot V_{REF} \cdot V_{ac}}{\sqrt{2} R_M R_{SENSE} V_{out} K_{BO}} \quad \text{(eq. 17)}$$

$$= \eta \frac{2\pi R_{CS} \cdot \Delta V_{CONTROL} \cdot V_{REF} \cdot V_{ac}}{\sqrt{2} R_M R_{SENSE} V_{out} K_{BO}}$$

$$V_{out} = \eta \frac{2\pi R_{CS} \cdot \Delta V_{CONTROL} \cdot V_{REF}}{\sqrt{2} R_M R_{SENSE} K_{BO}} \cdot \frac{V_{ac}}{P_{out}} \quad \text{(eq. 18)}$$

where

$V_{CONTROL(max)}$ is the maximum control voltage.

$\Delta V_{CONTROL}$ is the gap between $V_{CONTROL(max)}$ and $V_{CONTROL(min)}$.

It is illustrated in Figure 39.

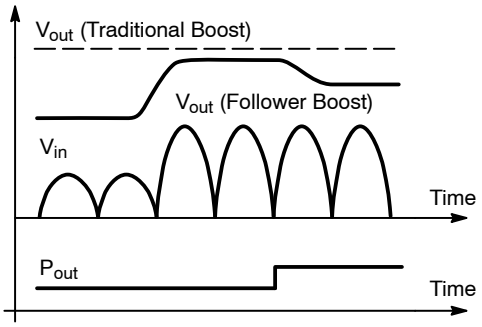


Figure 39. Follower Boost Characteristics

Follower Boost Benefits

The follower boost circuit offers and opportunity to reduce the output voltage V_{out} whenever the rms input voltage V_{ac} is lower or the power demand P_{out} is higher. Because of the step−up characteristics of boost converter, the output voltage V_{out} will always be higher than the input voltage V_{in} even though V_{out} is reduced in follower boost operation. As a result, the on time t_1 is reduced. Reduction of on time makes the loss of the inductor and power MOSFET smaller. Hence, it allows cheaper cost in the inductor and power MOSFET or allows the circuit components to operate at a lower stress condition in most of the time.

Reference Section

The internal reference voltage (V_{REF}) is trimmed to be ±2% accurate over the temperature range (the typical value is 2.5 V). V_{REF} is the reference used for the regulation. V_{REF} also serves to build the thresholds of the fast transient response, Overvoltage (OVP), brown out (BO), and Undervoltage protections (UVP).

Output Feedback

The output voltage V_{out} of the PFC circuits is sensed at V_{fb} pin via the resistor divider (R_{fbL} and R_{fbU}) as shown in Figure 38. V_{out} is regulated as described in (Equation 19).

$$V_{out} = V_{REF} \frac{R_{fbU} + R_{fbL}}{R_{fbL}} \quad \text{(eq. 19)}$$

The feedback signal V_{fb} represents the output voltage V_{out} and will be used in the output voltage regulation, Overvoltage protection (OVP), fast transient response, and Undervoltage protection (UVP)

Output Voltage Regulation

NCP1654 uses a high gain Operational Trans−conductance Amplifier (OTA) as error amplifier. Refer to Figure 38, the output of OTA $V_{control}$ operating range is from $V_{CONTROL(min)}$ to $V_{CONTROL(max)}$.

Fast Transient Response

Given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over or under−shoots because of abrupt load or input voltage variations (such as start−up duration). As shown in Figure 40, if the output voltage is out of regulation, NCP1654 has 2 functions to maintain the output voltage regulation.

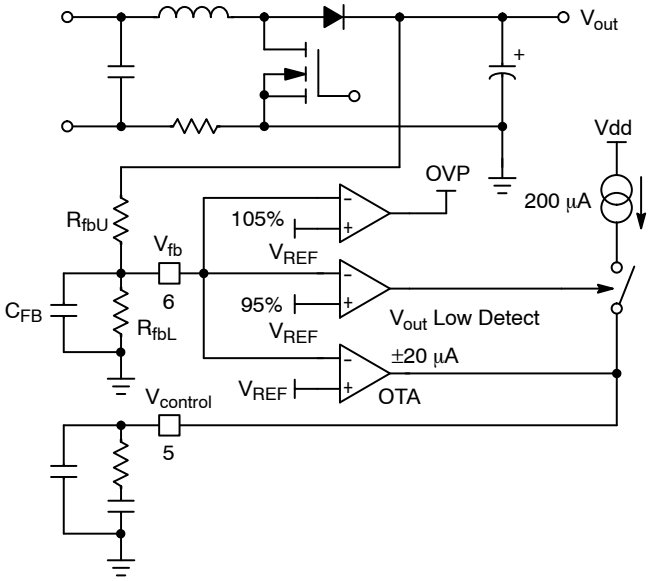


Figure 40. OVP and Fast Transient Response

- Overvoltage Protection: When V_{fb} is higher than 105% of V_{REF} (i.e. V_{out} > 105% of nominal output voltage), the Driver output of the device goes low for protection. The circuit automatically resumes operation when V_{fb} becomes lower than 105% of V_{REF}. If the nominal V_{out} is set at 390 V, then the maximum output voltage is 105% of 390 V = 410 V. Hence a cost & size effective bulk capacitor of lower voltage rating is suitable for this application,
- Dynamic response enhancer: NCP1654 drastically speeds up the regulation loop by its internal 200 μA enhanced current source when the output voltage is below 95% of its regulation level. Under normal condition, the maximum sink and source of output current capability of OTA is around 28 μA. Thanks to the "V_{out} low detect" block, when the V_{fb} is below 95% V_{REF}, an extra 200 μA current source will raise $V_{control}$ rapidly. Hence prevent the PFC output from dropping too low and improve the transient response performance. The relationship between current flowing in/out $V_{control}$ pin and V_{fb} is as shown in Figure 41.

It is recommended to add a typical 100 pF capacitor C_{FB} decoupling capacitor next to feedback pin to prevent from noise impact.

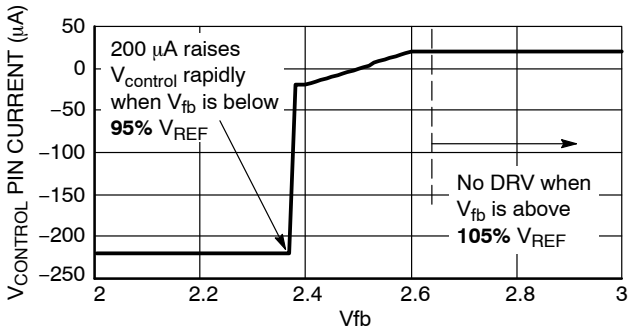


Figure 41. V_{fb} vs. Current Flowing in/out from $V_{control}$ Pin

Soft Start

The block diagram and timing diagram of soft start function are as shown in Figure 42 and Figure 43. The device provides no output (or no duty ratio) when the $V_{control}$ is lower than $V_{CONTROL(min)}$. $V_{control}$ is pulled low when:

- Brown−out, or
- Undervoltage Protection

When the IC recovers from one of the following conditions; Undervoltage Lockout, Brown−out or Undervoltage Protection, the 200 μA current source block keeps off. Hence only the Operating Trans−conductance Amplifier (OTA) raises the $V_{control}$. And $V_{control}$ rises slowly. This is to obtain a slow increasing duty cycle and hence reduce the voltage and current stress on the MOSFET. A soft−start operation is obtained.

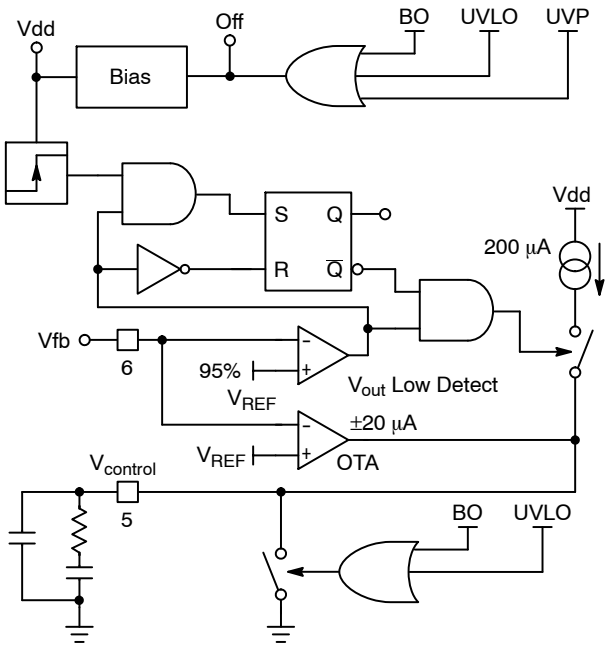


Figure 42. Soft Start Block Diagram

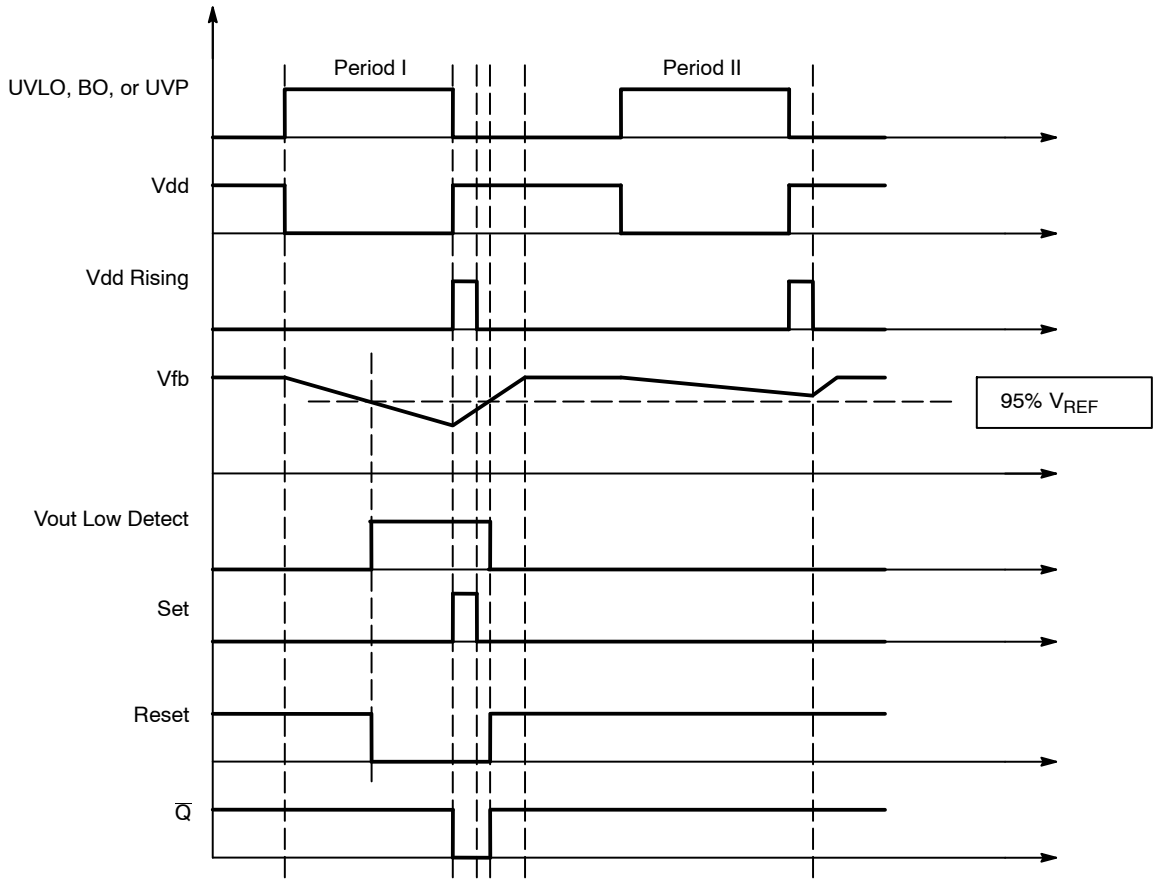


Figure 43. Soft Start Timing Diagram

Undervoltage Protection (UVP) for Open Loop Protection or Shutdown

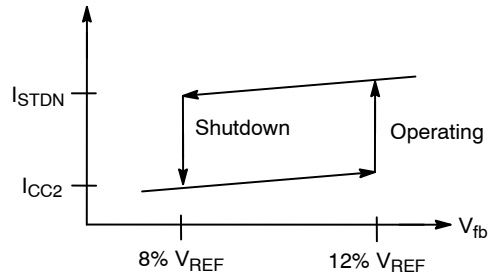


Figure 44. Undervoltage Protection

As shown in Figure 44, when V_{fb} is less than 8% of V_{REF}, the device is shut down and consumes less than 400 μA. The device automatically starts operation when the output voltage goes above 12% of V_{REF}. In normal situation of boost converter configuration, the output voltage V_{out} is always greater than the input voltage V_{in} and the feedback signal V_{fb} is always greater than 8% and 12% of V_{REF} to enable NCP1654 to operate.

This Undervoltage Protection function has 2 purposes.

- Open Loop Protection − Protect the power stage from damage at feedback loop abnormal, such as V_{fb} is shorted to ground or the feedback resistor R_{fbU} is open.
- Shutdown mode − Disables the PFC stage and forces a low consumption mode. This feature helps to meet stringent stand−by specifications. Power Factor being not necessary in stand−by, the PFC stage is generally inhibited to save the pre−converter losses. To further improve the stand−by performance, the PFC controller should consume minimum current in this mode.

Current Sense

The device senses the inductor current I_L by the current sense scheme in Figure 37. The device maintains the voltage at CS pin to be zero voltage (i.e., $V_{cs} \approx 0$ V) so that (Equation 11),

$$I_{cs} = \frac{R_{SENSE}}{R_{CS}} I_L ,$$

can be formulated.

This scheme has the advantage of the minimum number of components for current sensing. The sense current I_{cs} represents the inductor current I_L and will be used in the PFC duty modulation to generate the multiplier voltage V_m, Over−Power Limitation (OPL), and Over−Current Protection. (Equation 11) would insist in the fact that it provides the flexibility in the R_{SENSE} choice and that it allows to detect in−rush currents.

Over−Current Protection (OCP)

Over−Current Protection is reached when I_{cs} is larger than $I_{S(OCP)}$ (200 μA typical). The offset voltage of the CS pin is typical 10 mV and it is neglected in the calculation. Hence, the maximum OCP inductor current threshold $I_{L(OCP)}$ is obtained in (Equation 20).

$$I_{L(OCP)} = \frac{R_{CS} I_{S(OCP)}}{R_{SENSE}} = \frac{R_{CS}}{R_{SENSE}} \cdot 200\ \mu A \quad \text{(eq. 20)}$$

When over−current protection threshold is reached, the Drive Output of the device goes low. The device automatically resumes operation when the inductor current goes below the threshold.

Input Voltage Sense

The device senses the rms input voltage V_{ac} by the sensing scheme in Figure 45. V_{bo} senses the average rectified input voltage V_{in} via the resistor divider. An external capacitor C_{BO} is to maintain the V_{bo} the average value of V_{in}. V_{bo} is used for Brown−Out Protection, PFC duty modulation and over−power limitation (OPL).

Brown−Out Protection

The device uses the V_{bo} signal to protect the PFC stage from operating as the input voltage is lower than expected. Re−formulate (Equation 9) to get (Equation 21). Refer to Figure 45, V_{in} is different before and after the device operating.

- Before the device operates, V_{in} is equal to the peak value of rms input voltage, V_{ac}. Hence V_{bo} is as described in (Equation 21).

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} (V_{in}) = \frac{R_{boL}}{R_{boL} + R_{boU}} \sqrt{2}\, V_{ac} \quad \text{(eq. 21)}$$

- After device operates, V_{in} is the rectified sinusoidal input voltage. Thanks to C_{BO}, V_{bo} is the **average** of rectified input voltage. Hence V_{bo} decays to $2/\pi$ of the peak value of rms input voltage V_{ac} as described in (Equation 22).

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} \frac{2\sqrt{2}}{\pi} V_{ac} \quad \text{(eq. 22)}$$

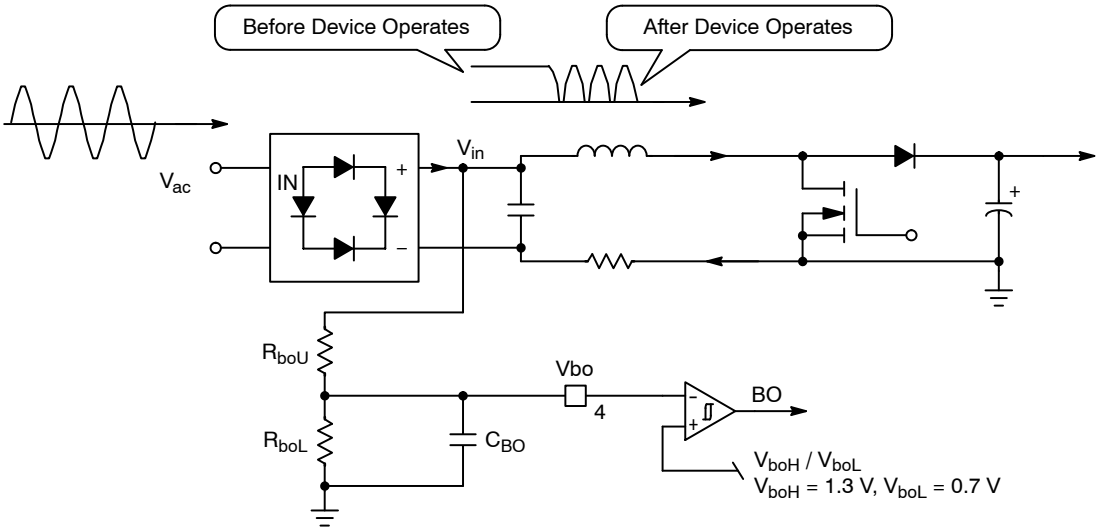


Figure 45. Brown−Out Protection

Hence a larger hysteresis of the brown out comparator is needed, which is 0.7 V typical in this device. When V_{bo} goes below than V_{BOL} (0.7 V typical), the device turns off the Drive output and keeps it off till V_{bo} exceeds V_{BOH} (1.3 V typical). When the device awakes after an off−state (Undervoltage lockout or shutdown), the default threshold is V_{BOH}.

Overpower Limitation (OPL)

This is a second OCP with a threshold that is line dependent. Sense current I_{cs} represents the inductor current I_L and hence represents the input current approximately. Input voltage signal V_{bo} represents the rms input voltage. The product ($I_{cs} \cdot V_{bo}$) represents an approximated input power ($I_L \cdot V_{ac}$). It is illustrated in Figure 46.

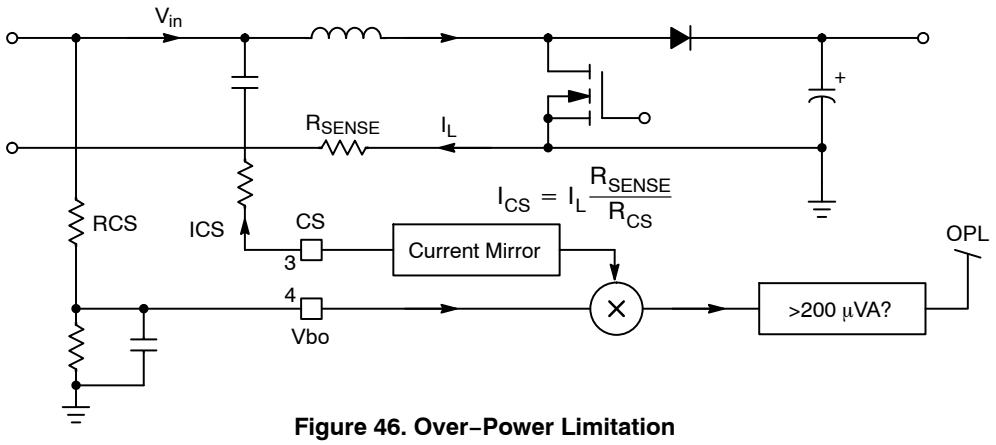


Figure 46. Over−Power Limitation

When the product ($I_{cs} \cdot V_{bo}$) is greater than a permissible level 200 μVA, the device turns off the drive output so that the input power is limited. The OPL is automatically deactivated when the product ($I_{cs} \cdot V_{bo}$) is lower than the 200 μVA level. This 200 μVA level corresponds to the approximated input power ($I_L \cdot V_{ac}$) to be smaller than the particular expression in (Equation 23).

$$I_{cs}V_{bo} < 200\ \mu VA \qquad \text{(eq. 23)}$$

$$\left(I_L \frac{R_{SENSE}}{R_{CS}}\right) \cdot \left(\frac{2\sqrt{2}K_{BO}}{\pi} \cdot V_{ac}\right) < 200\ \mu VA$$

$$I_L \cdot V_{ac} < \frac{R_{CS} \cdot \pi}{R_{SENSE} \cdot K_{BO}} \cdot 50\sqrt{2}\ \mu VA$$

Bias the Controller

It is recommended to add a typical 1 nF to 100 nF decoupling capacitor next to the V_{cc} pin for proper operation. When the NCP1654 operates in follower boost mode, the PFC output voltage is not always regulated at a particular level under all application range of input voltage and load power. It is not recommended to make a low−voltage bias supply voltage by adding an auxiliary winding on the PFC boost inductor. Alternatively, it is recommended to get the V_{cc} biasing supply from the 2nd−stage power conversion stage.

V_{cc} Undervoltage LockOut (UVLO)

The device incorporates an Undervoltage Lockout block to prevent the circuit from operating when Vcc is too low in order to ensure a proper operation. An UVLO comparator monitors V_{cc} pin voltage to allow the NCP1654 to operate when V_{cc} exceeds 10.5 V typically. The comparator incorporates some hysteresis (1.5 V) to prevent erratic operation as the V_{cc} crosses the threshold. When V_{cc} goes below the UVLO comparator lower threshold (9 V typically), the circuit turns off. It is illustrated in Figure 47. After startup, the operating range is between 9 V and 20 V.

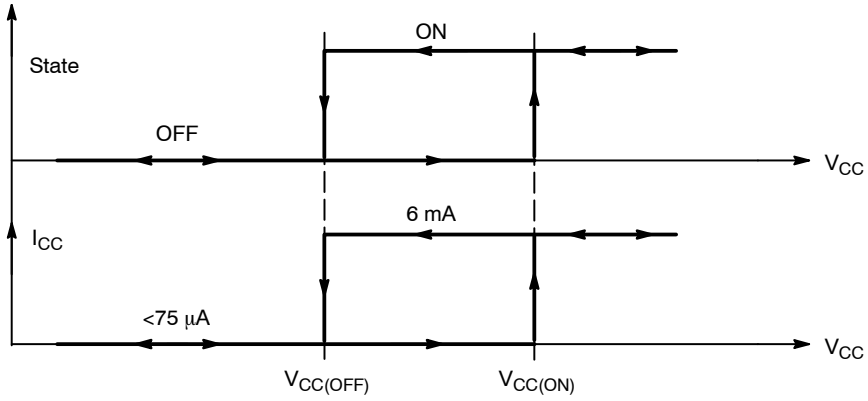


Figure 47. V_{cc} Undervoltage LockOut (UVLO)

Thermal Shutdown

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C. The output stage is then enabled once the temperature drops below typically 120°C (i.e., 30°C hysteresis). The thermal shutdown is provided to prevent possible device failures that could result from an accidental overheating.

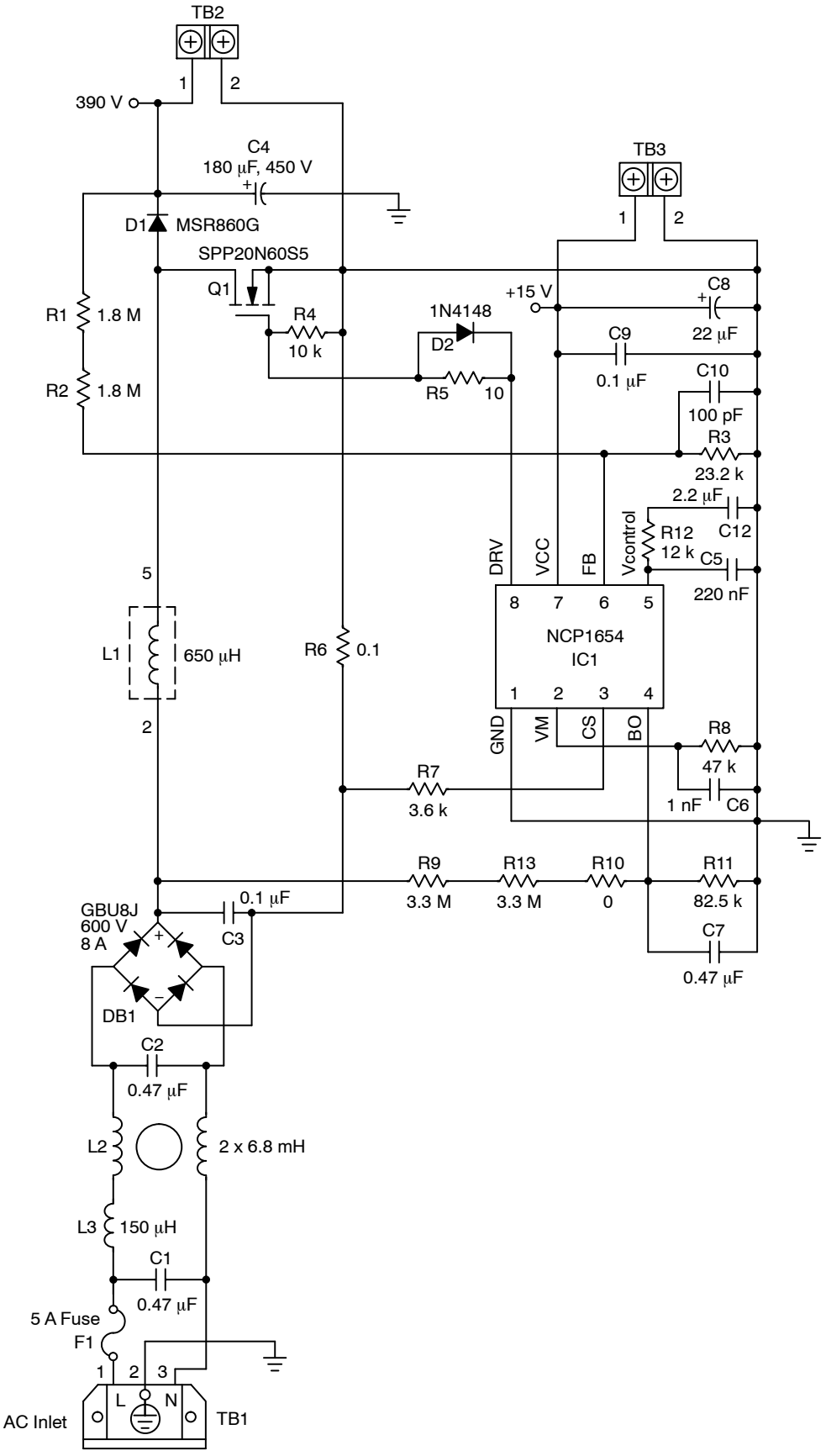


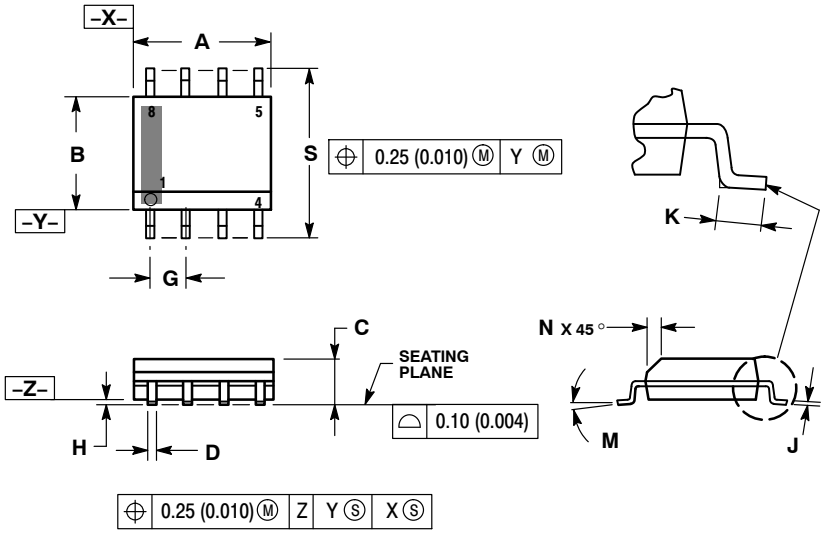
Figure 48. Application Schematic – 300 W 65 kHz Power Factor Correction Circuit

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

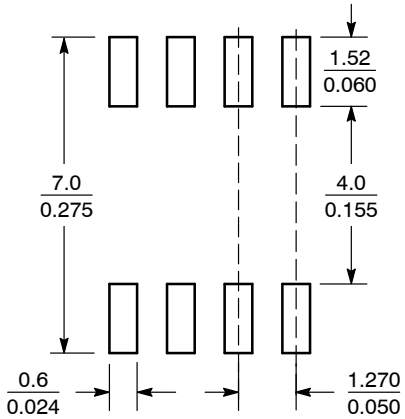
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

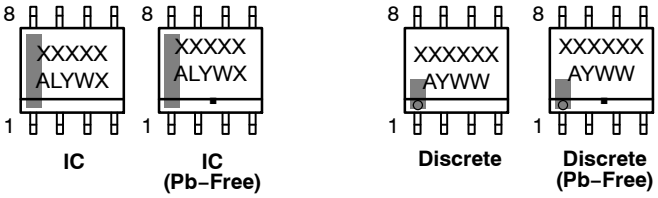
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales