NCP1395A/B

Controller, High Performance Resonant Mode

The NCP1395A/B offers everything needed to build a reliable and rugged resonant mode power supply. Its unique architecture includes a 1.0 MHz Voltage Controller Oscillator whose control mode brings flexibility when an ORing function is a necessity, e.g. in multiple feedback paths implementations. Protections featuring various reaction times, e.g. immediate shutdown or timer–based event, brown–out, broken optocoupler detection etc., contribute to a safer converter design, without engendering additional circuitry complexity. An adjustable deadtime also helps lowering the shoot–through current contribution as the switching frequency increases.

Finally, an onboard operational transconductance amplifier allows for various configurations, including constant output current working mode or traditional voltage regulation.

Features

- High Frequency Operation from 50 kHz up to 1.0 MHz
- Selectable Minimum Switching Frequency with $\pm 3\%$ Accuracy
- Adjustable Deadtime from 150 ns to 1.0 μs
- Startup Sequence via an Adjustable Soft–Start
- Brown–Out Protection for a Simpler PFC Association
- Latched Input for Severe Fault Conditions, e.g. Overtemperature or OVP
- Timer–Based Input with Auto–Recovery Operation for Delayed Event Reaction
- Enable Input for Immediate Event Reaction or Simple ON/OFF Control
- Operational Transconductance Amplifier (OTA) for Multiple Feedback Loops
- V_{CC} Operation up to 20 V
- Low Startup Current of 300 μA Max
- Common Collector Optocoupler Connection
- Internal Temperature Shutdown
- B Version Features 10 V V_{CC} Startup Threshold for Auxiliary Supply Usage
- Easy No–Load Operation and Low Standby Power Due to Programmable Skip–Cycle
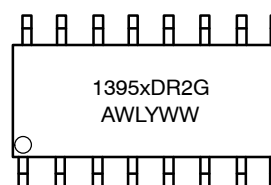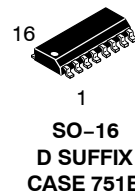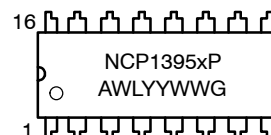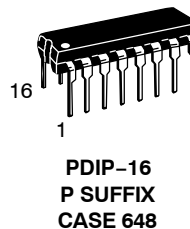- These are Pb–Free Devices

Typical Applications

- LCD/Plasma TV Converters
- High Power Ac–DC Adapters for Notebooks
- Industrial and Medical Power Sources
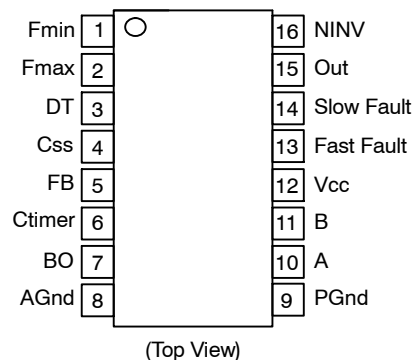- Offline Battery Chargers

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MARKING DIAGRAMS

PDIP–16
P SUFFIX
CASE 648

```
NCP1395xP
AWLYYWWG
```

SO–16
D SUFFIX
CASE 751B

```
1395xDR2G
AWLYWW
```

x	= A or B
A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb–Free Package

PIN CONNECTIONS

Fmin	1	16	NINV
Fmax	2	15	Out
DT	3	14	Slow Fault
Css	4	13	Fast Fault
FB	5	12	Vcc
Ctimer	6	11	B
BO	7	10	A
AGnd	8	9	PGnd

(Top View)

ORDERING INFORMATION

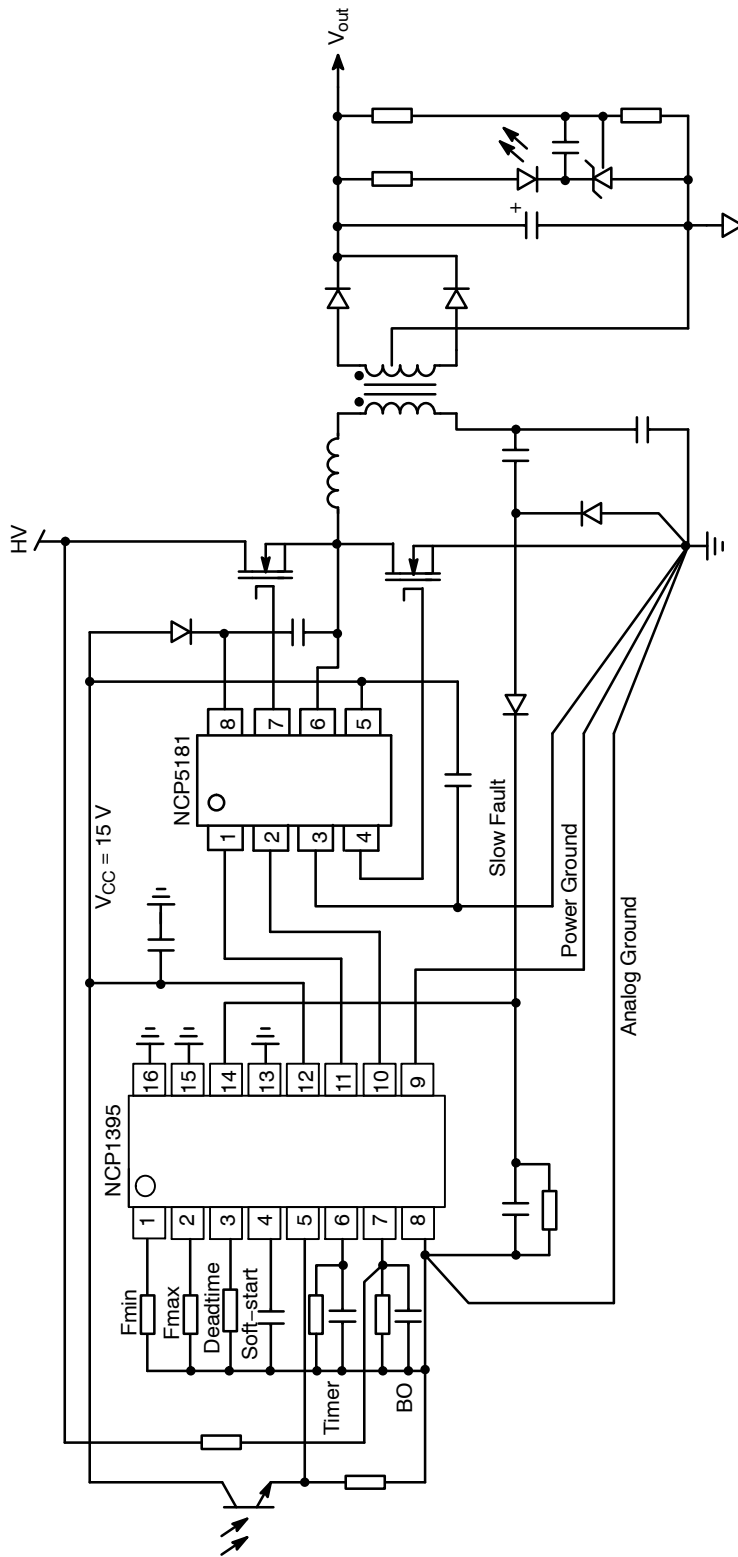See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

Figure 1. Typical Application Example

NCP1395A/B

PIN FUNCTION DESCRIPTION

| Pin No.	Symbol	Function	Description
1	Fmin	Timing Resistor	Connecting a resistor to this pin, sets the minimum oscillator frequency reached for VFB is below 1.3 V.
2	Fmax	Frequency Clamp	A resistor sets the maximum frequency excursion.
3	DT	Deadtime	A simple resistor adjusts the deadtime length.
4	Css	Soft−Start	Select the soft−start duration.
5	FB	Feedback	Applying a voltage above 1.3 V on this pin increases the oscillation frequency up to Fmax.
6	Ctimer	Timer Duration	Sets the timer duration in presence of a fault.
7	BO	Brown−Out	Detects low input voltage conditions. When brought above Vlatch, it fully latches off the controller.
8	Agnd	Analog Ground	−
9	Pgnd	Power Ground	−
10	A	Low Side Output	Drives the low side power MOSFET.
11	B	High Side Output	Drives the upper side power MOSFET.
12	Vcc	Supplies the Controller	−
13	Fast Fault	Quick Fault Detection	Fast shutdown pin, stops all pulses when brought high. Please look in the description for more details about the fast−fault sequence.
14	Slow Fault	Slow Fault Detection	When asserted, the timer starts to countdown and shuts down the controller at the end of its time duration.
15	OUT	OPAMP Output	Internal transconductance amplifier.
16	NINV	OPAMP Noninverting	Non−inverting pin of the OPAMP.
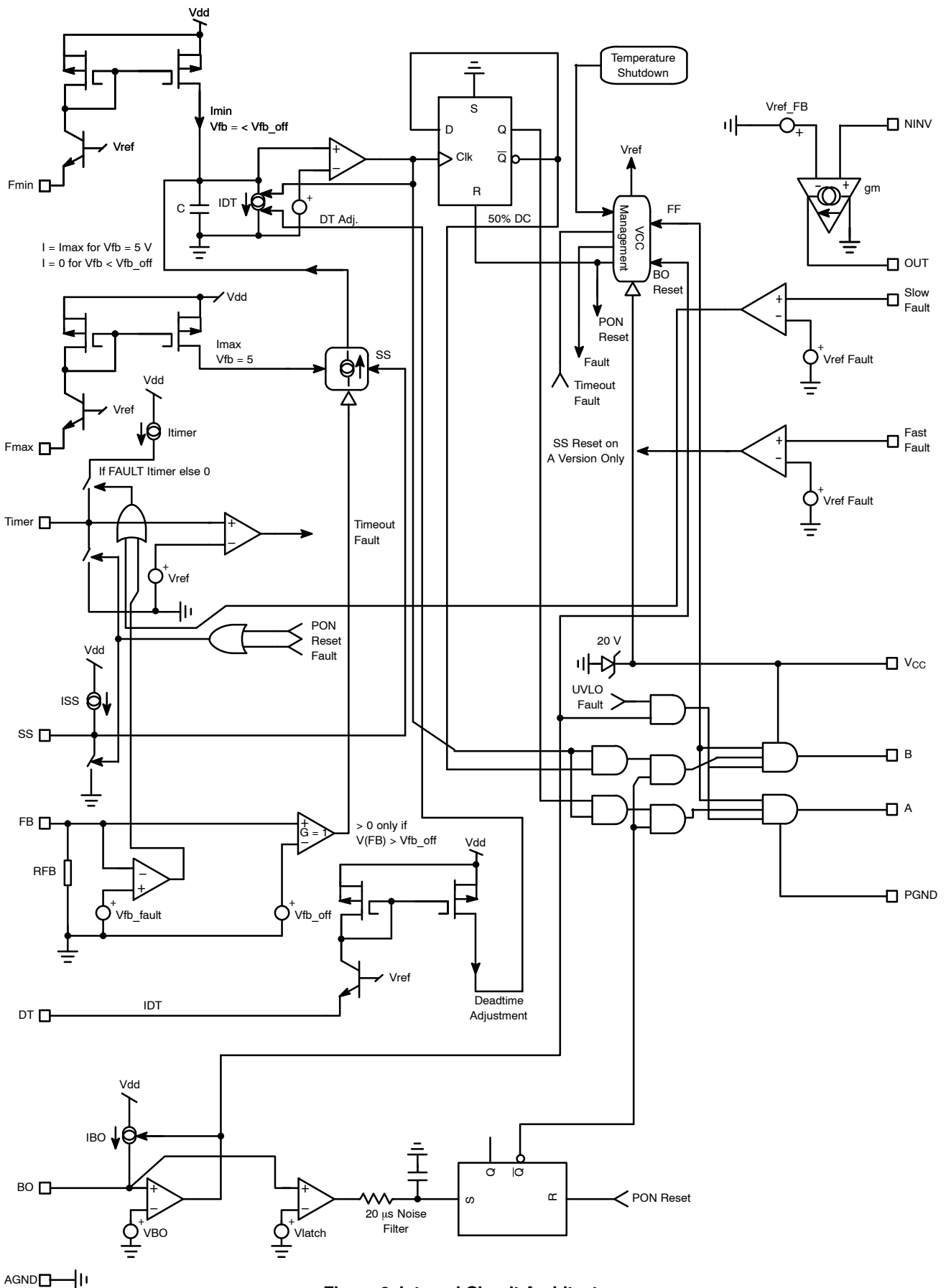
Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 12	V_{CC}	20	V
Transient Current Injected into V_{CC} when Internal Zener is Activated − Pulse Width < 10 ms	−	10	mA
Power Supply Voltage, All Pins (Except Pins 10 and 11)	−	−0.3 to 10	V
Thermal Resistance, Junction−to−Air, PDIP Version	$R_{\theta JA}$	130	°C/W
Thermal Resistance, Junction−to−Air, SOIC Version	$R_{\theta JA}$	100	°C/W
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, Human Body Model	−	2	kV
ESD Capability, Machine Model	−	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. This device series contains ESD protection and exceeds the following tests:
    Human Body Model 2000V per JESD22−A114−B
    Machine Model Method 200V per JESD22−A115−A.
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION						
Turn−On Threshold Level, V_{CC} Going Up − A Version	12	VCC_{ON}	12.3	13.3	14.3	V
Turn−On Threshold Level, V_{CC} Going Up − B Version	12	VCC_{ON}	9.3	10.3	11.3	V
Minimum Operating Voltage after Turn−On	12	$VCC_{(min)}$	8.3	9.3	10.3	V
Minimum Hysteresis between VCC_{ON} and $VCC_{(min)}$ − A Version	12	VhysteA	–	3.0	–	V
Minimum Hysteresis between VCC_{ON} and $VCC_{(min)}$ − B Version	12	VhysteB	–	1.0	–	V
Startup Current, $V_{CC} < VCC_{ON}$	12	Istartup	–	–	300	μA
V_{CC} Level at which the Internal Logic gets Reset	12	VCC_{reset}	–	5.9	–	V
Internal IC Consumption, No Output Load on Pins 11/12, Fsw = 300 kHz	12	ICC1	–	1.6	–	mA
Internal IC consumption, 100 pF output load on pin 11 / 12, Fsw = 300 kHz	12	ICC2	–	2.3	–	mA
Consumption in fault mode (All drivers disabled, Vcc > $VCC_{(min)}$)	12	ICC3	–	1.3	–	mA
VOLTAGE CONTROL OSCILLATOR (VCO)						
Minimum Switching Frequency, Rt = 120 kΩ on Pin 1, Vpin 5 = 0 V, DT = 300 ns	1	Fsw min	48.5	50	51.5	kHz
Maximum Switching Frequency, Rfmax = 22 kΩ on Pin 2, Vpin 5 > 6.0 V, DT = 300 ns − T_j = 25°C (Note 3)	2	Fsw max	0.9	1.0	1.11	MHz
Feedback Pin Swing above which Δf = 0	5	FBSW	–	6.0	–	V
VCO V_{CC} Rejection, ΔV_{CC} = 1.0 V, in Percentage of Fsw	–	PSRR	–	0.2	–	%/V
Operating Duty Cycle	11−10	DC	48	50	52	%
Reference Voltage for all Current Generations (Fosc, DT)	1, 3	VREF	1.86	2.0	2.14	V
Delay before any Driver Restart in Fault Mode	–	Tdel	–	20	–	μs
FEEDBACK SECTION						
Internal Pulldown Resistor	5	Rfb	–	20	–	kΩ
OTA Internal Offset Voltage	16	VREF_FB	2.325	2.5	2.675	V
Voltage on Pin 5 below which the FB Level has no VCO Action	5	Vfb_off	–	1.3	–	V
Voltage on Pin 5 below which the Controller Considers a Fault	5	Vfb_fault	–	0.6	–	V
Input Bias Current	16	IBias	–	–	100	nA
DC Transconductance Gain	15	OTAG	–	250	–	μS
Gain Product Bandwidth, Rload = 5.0 kΩ	15	GBW	–	1.0	–	MHz
DRIVE OUTPUT						
Output Voltage Rise Time @ CL = 100 pF, 10−90% of Output Signal	11−10	T_r	–	20	–	ns
Output Voltage Fall−Time @ CL = 100 pF, 10−90% of Output Signal	11−10	T_f	–	20	–	ns
Source Resistance	11−10	R_{OH}	20	60	120	Ω
Sink Resistance	11−10	R_{OL}	30	60	130	Ω
Deadtime with R_{DT} = 127 kΩ from Pin 3 to GND	3	T_dead	270	300	390	ns
Maximum Deadtime with R_{DT} = 540 kΩ from Pin 3 to GND	3	T_dead−max	–	1.0	–	μs
Minimum Deadtime, R_{DT} = 30 kΩ from Pin 3 to GND	3	T_dead−min	–	150	–	ns

3. Room temperature only, please look at characterization data for evolution versus junction temperature.

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
TIMERS						
Timer Charge Current	6	Itimer	–	150	–	μA
Timer Duration with a 1.0 μF Capacitor and a 1.0 MΩ Resistor	6	T–timer	–	25	–	ms
Timer Recurrence in Permanent Fault, Same Values as Above	6	T–timerR	–	1.4	–	s
Voltage at which Pin 6 Stops Output Pulses	6	VtimerON	3.7	4.1	4.5	V
Voltage at which Pin 6 Restarts Output Pulses	6	VtimerOFF	0.9	1.0	1.1	V
Soft–Start Ending Voltage, V_{FB} = 1.0 V	4	VSS	–	2.0	–	V
Soft–Start Charge Current	4	ISS	75 Note 5	95	115	μA
Soft–Start Duration with a 220 nF Capacitor (Note 4)	4	T–SS	–	5.0	–	ms
PROTECTION						
Reference Voltage for Fast Input	13	VrefFaultF	1.0	1.05	1.1	V
Reference Voltage for Slow Input	14	VrefFaultS	0.98	1.03	1.08	V
Hysteresis for Fast Input	13	HysteFaultF	–	50	–	mV
Hysteresis for Slow Input	14	HysteFaultS	–	40	–	mV
Propagation Delay for Fast Fault Input Drive Shutdown	13	TpFault	–	70	120	ns
Brown–Out Input Bias Current	7	IBObias	–	0.02	–	μA
Brown–Out Level	7	VBO	0.98	1.03	1.08	V
Hysteresis Current, Vpin 7 > VBO − A Version	7	IBO_A	23	28	33	μA
Hysteresis Current, Vpin 7 > VBO − B Version	7	IBO_B	70	83	96	μA
Latching Voltage	7	Vlatch	3.7	4.1	4.5	V
Temperature Shutdown	–	TSD	140	–	–	°C
Hysteresis	–	TSDhyste	–	40	–	°C

4. The A version does not activate soft–start when the fast–fault is released, this is for skip cycle implementation. The B version does activate the soft–start upon release of the fast–fault input.
5. Minimum current occurs at T_J = 0°C.

TYPICAL CHARACTERISTICS – A VERSION

Figure 3. VCCon A
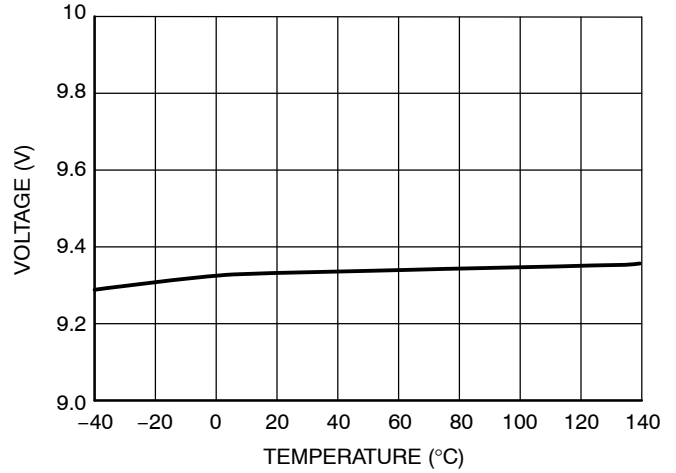
Figure 4. VCCmin
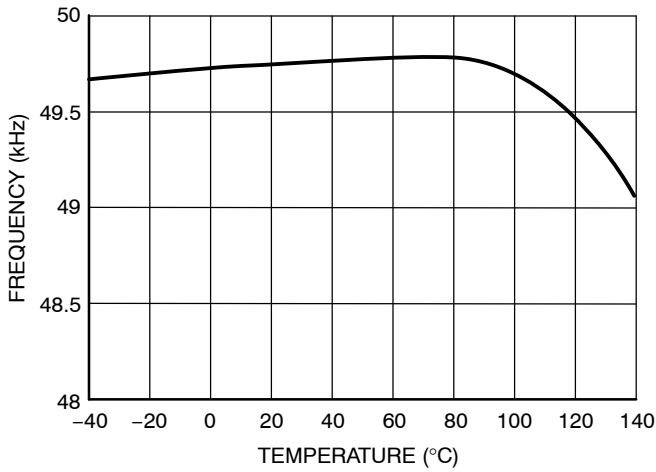
Figure 5. Fsw min
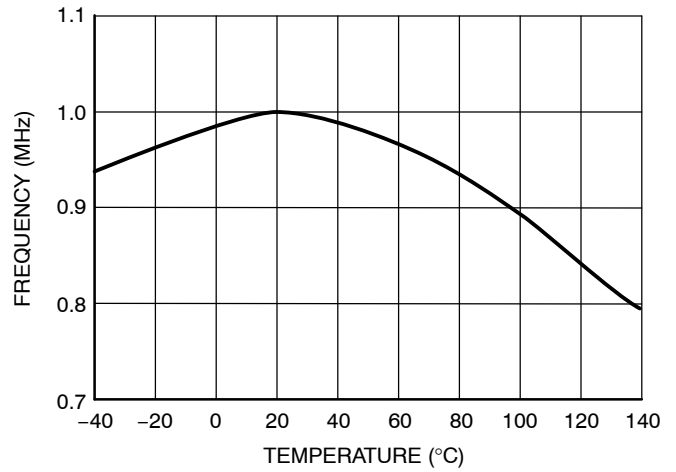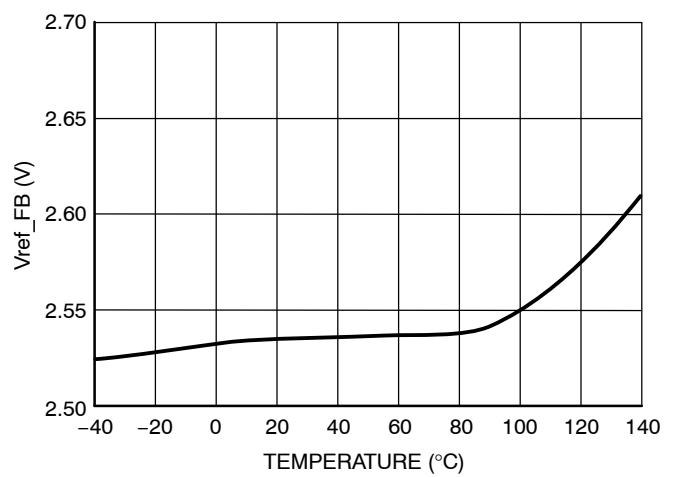
Figure 6. Fsw max
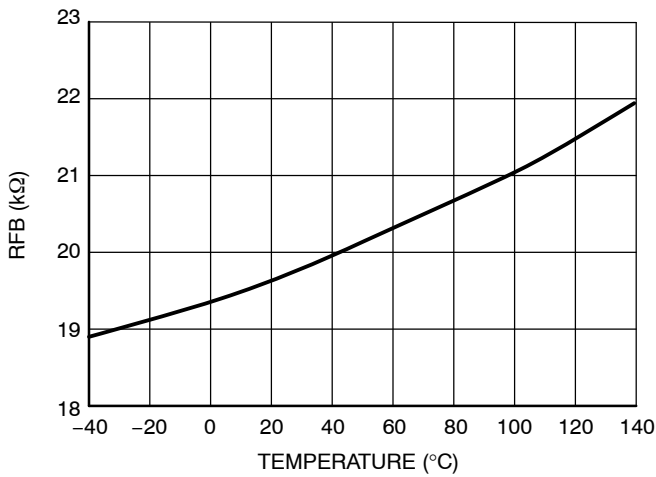
Figure 8. Pulldown Resistor (RFB)

Figure 7. Reference (Vref_FB)

TYPICAL CHARACTERISTICS – A VERSION
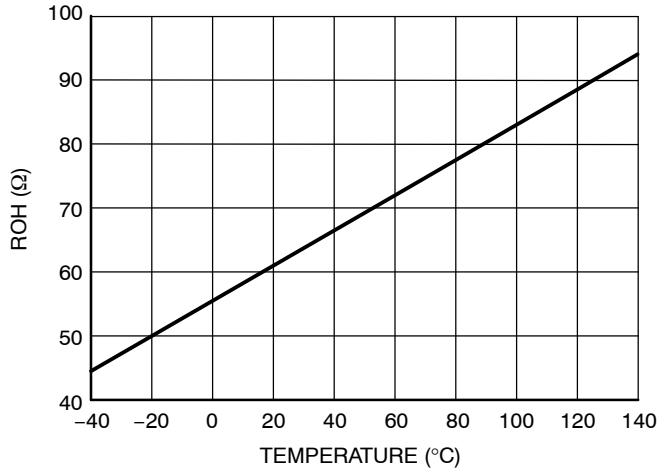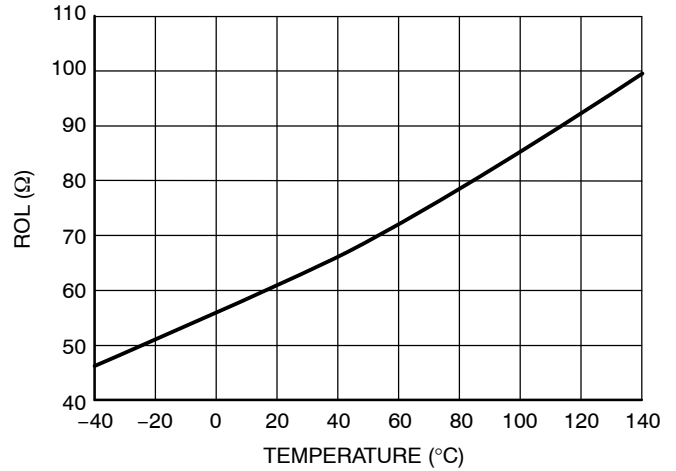
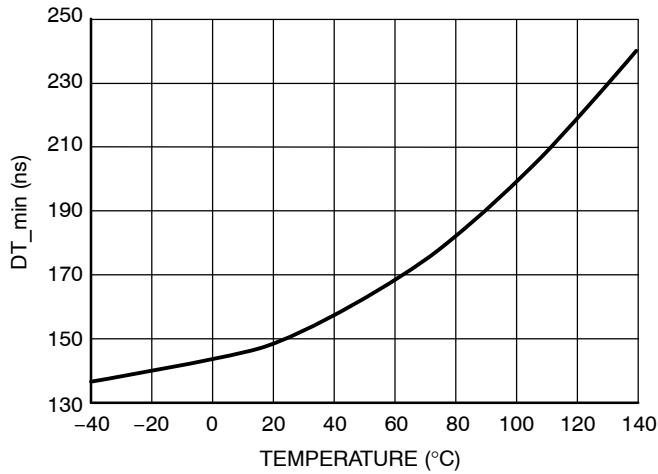Figure 9. Source Resistance (ROH)
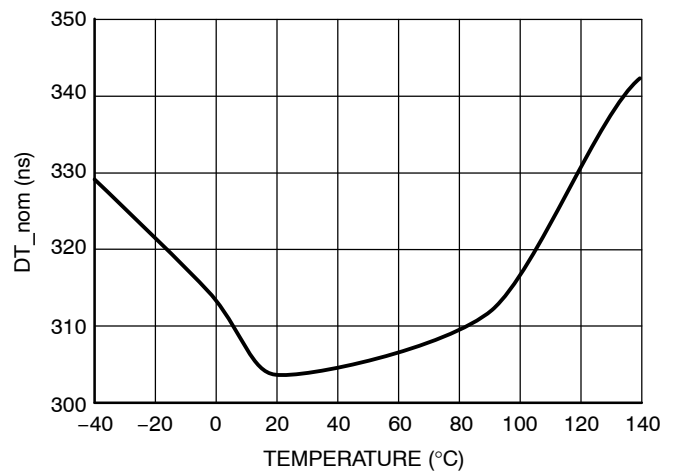
Figure 10. Sink Resistance (ROL)
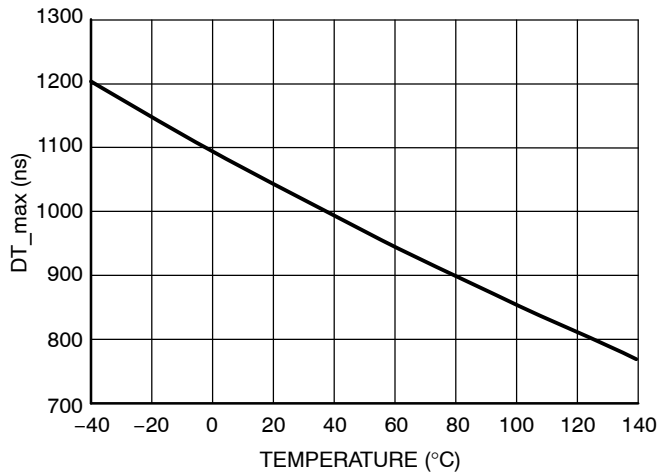
Figure 11. T_dead_min A

Figure 12. T_dead_A

Figure 14. T_dead_max A

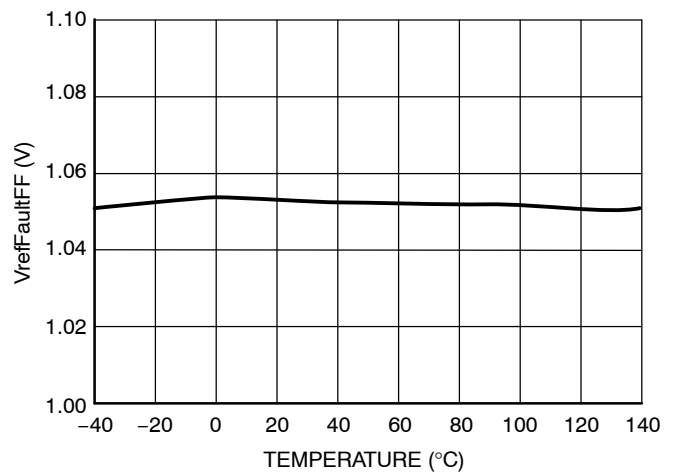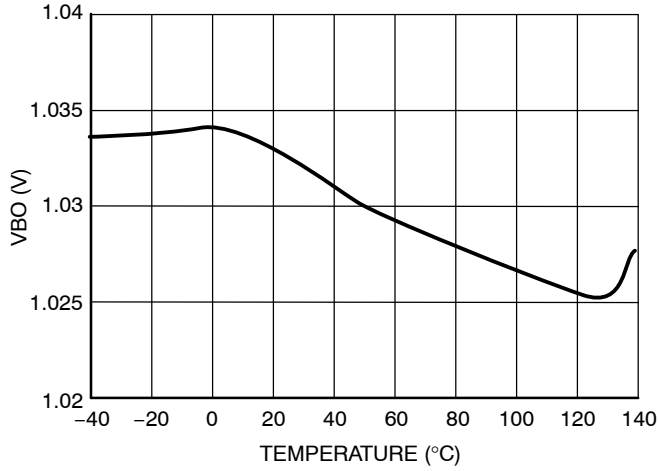Figure 13. Fast Fault (VrefFault FF)

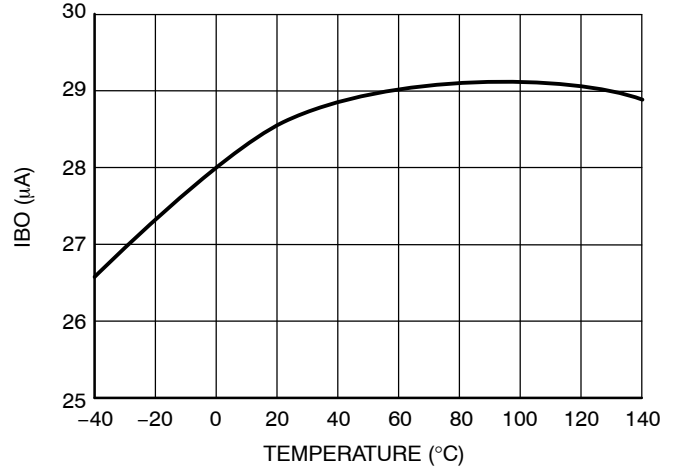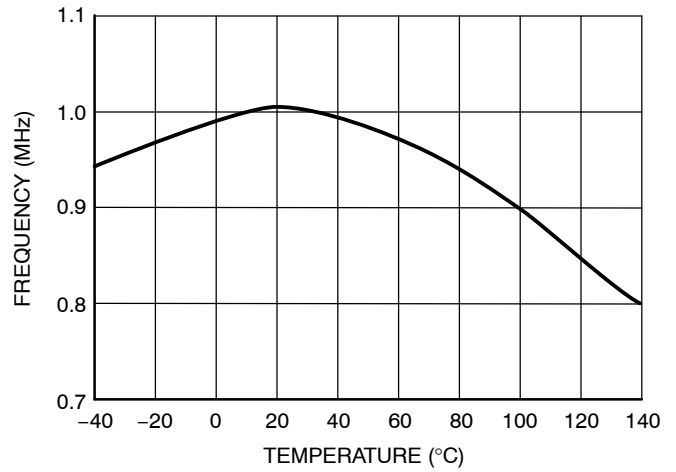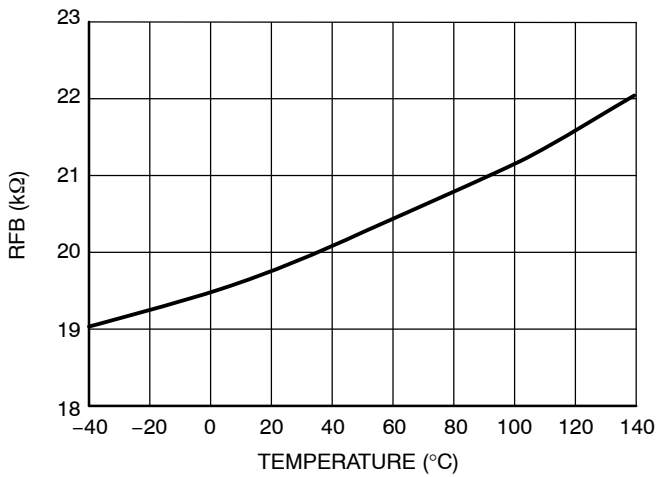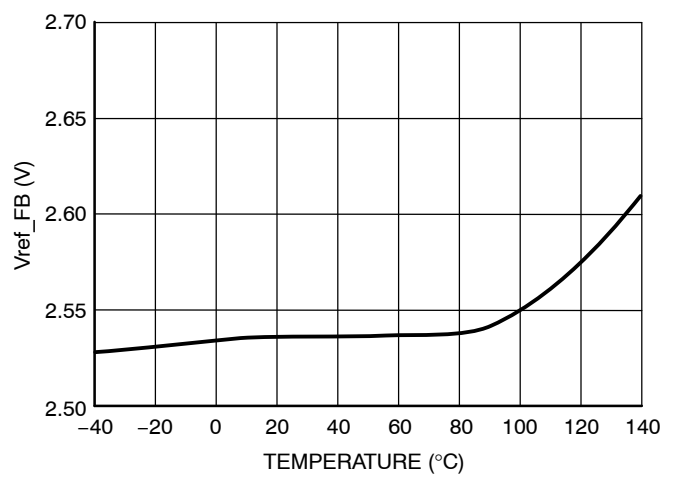## TYPICAL CHARACTERISTICS − A VERSION

Figure 15. Brown−Out Reference (VBO)

Figure 16. Brown−Out Hysteresis Current (IBO)
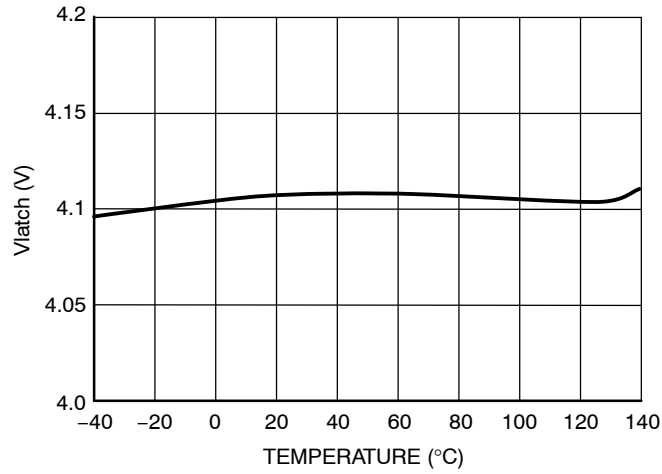
Figure 17. Latch Level (Vlatch)

TYPICAL CHARACTERISTICS − B VERSION

Figure 18. VCCon B
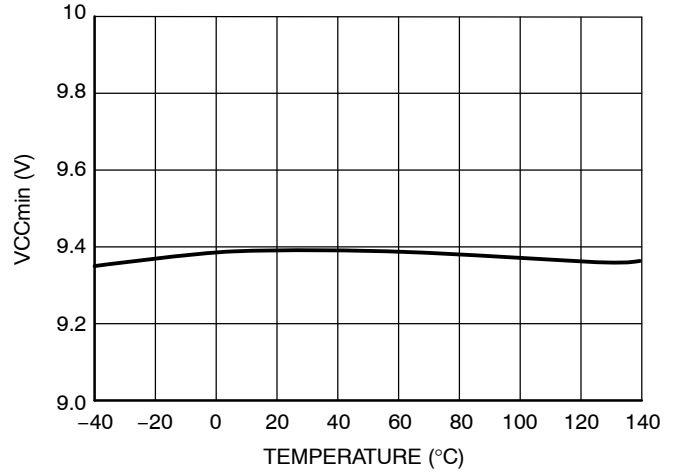
Figure 19. VCCmin
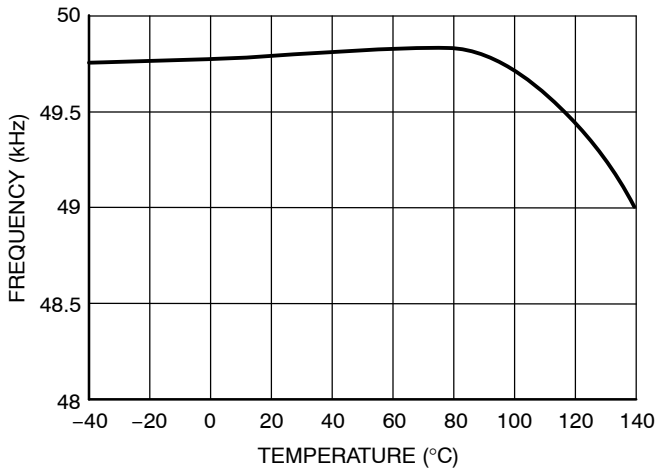
Figure 20. Fsw min

Figure 21. Fsw max

Figure 23. Pulldown Resistor (RFB)

Figure 22. Reference (Vref_FB)

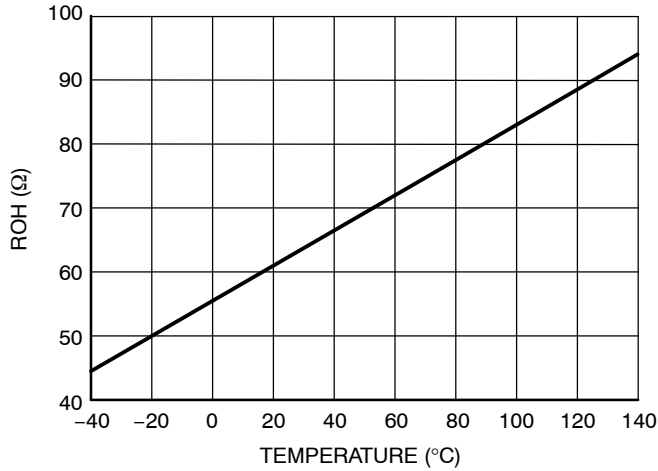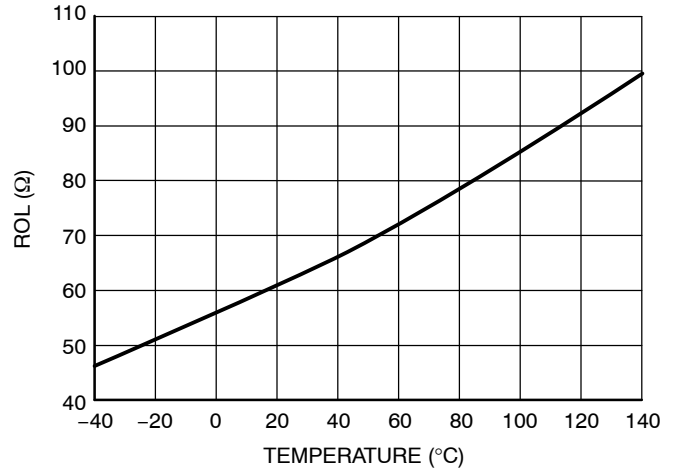## TYPICAL CHARACTERISTICS − B VERSION

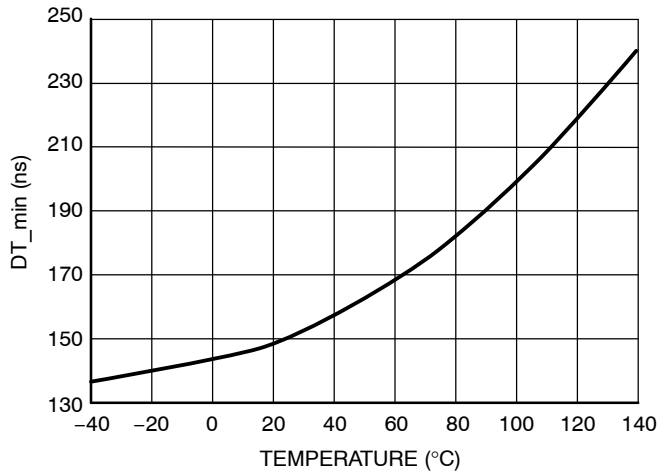**Figure 24. Source Resistance (ROH)**

Figure 25. Sink Resistance (ROL)
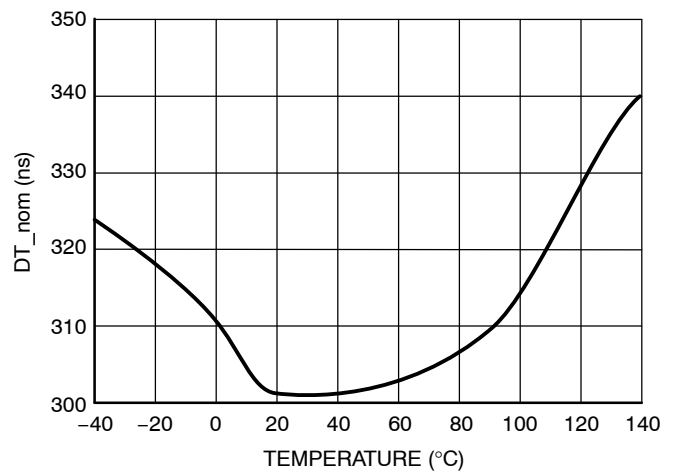
Figure 26. T_dead_min B
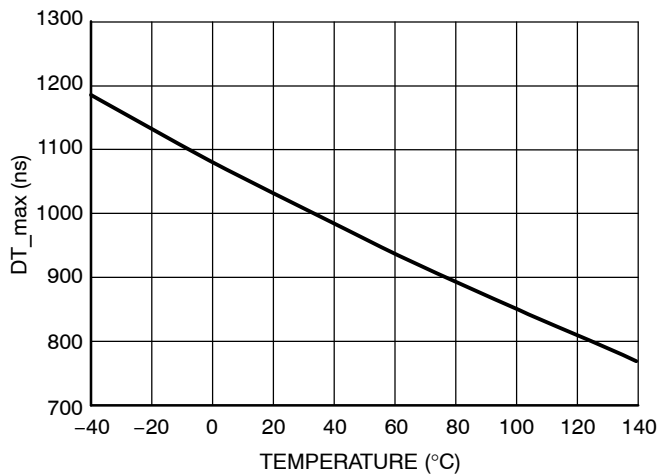
Figure 27. T_dead_B

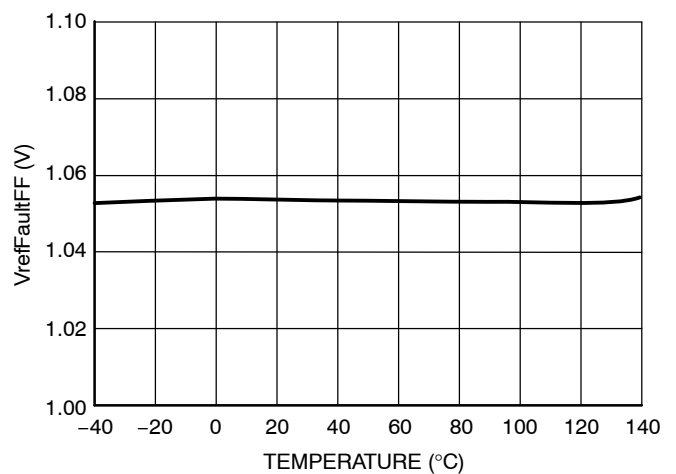**Figure 29. T_dead_max B**

Figure 28. Fast Fault (VrefFault FF)

NCP1395A/B

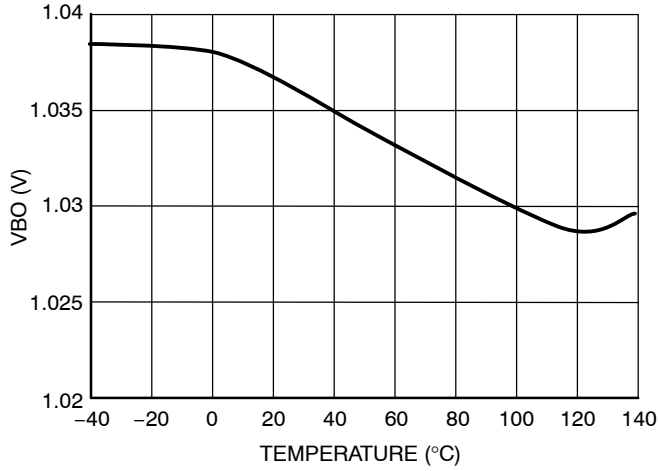## TYPICAL CHARACTERISTICS – B VERSION

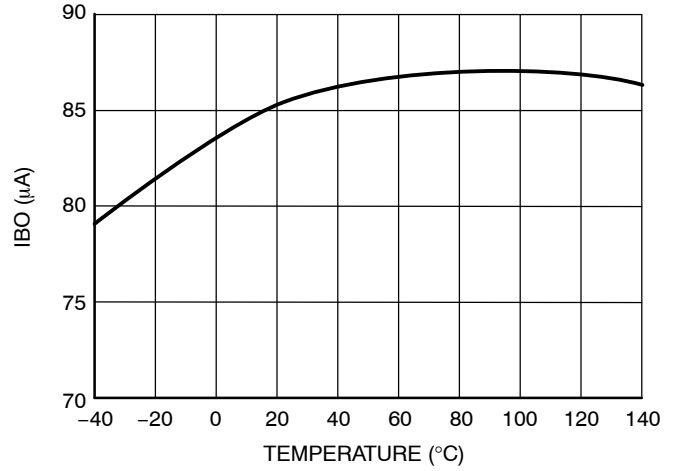**Figure 30. Brown−Out Reference (VBO)**

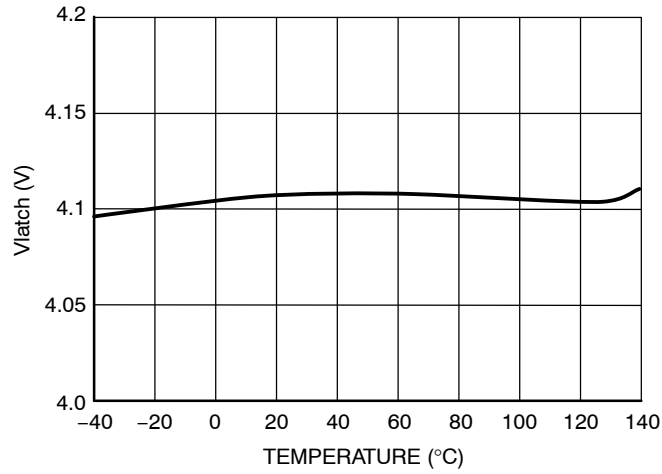**Figure 31. Brown−Out Hysteresis Current (IBO)**

Figure 32. Latch Level (Vlatch)

APPLICATION INFORMATION

The NCP1395A/B includes all necessary features to help build a rugged and safe switch−mode power supply featuring an extremely low standby power. The below bullets detail the benefits brought by implementing the NCP1395A/B controller:

- **Wide Frequency Range:** A high−speed Voltage Control Oscillator allows an output frequency excursion from 50 kHz up to 1.0 MHz on A and B outputs.

- **Adjustable Deadtime:** Due to a single resistor wired to ground, the user has the ability to include some deadtime, helping to fight cross−conduction between the upper and the lower transistor.

- **Adjustable Soft−Start:** Every time the controller starts to operate (power on), the switching frequency is pushed to the programmed maximum value and slowly moves down toward the minimum frequency, until the feedback loop closes. The soft−start sequence is activated in the following cases: a) normal startup b) back to operation from an off state: during hiccup faulty mode, brown−out or temperature shutdown (TSD). In the NCP1395A, the soft−start is not activated back to operation from the fast fault input, unless the feedback pin voltage reaches 0.6 V. To the opposite, in the B version, the soft−start is always activated back from the fast fault input whatever the feedback level is.

- **Adjustable Minimum and Maximum Frequency Excursion:** In resonant applications, it is important to stay away from the resonating peak to keep operating the converter in the right region. Due to a single external resistor, the designer can program its lowest frequency point, obtained in lack of feedback voltage (during the startup sequence or in short−circuit conditions). Internally trimmed capacitors offer a ±3% precision on the selection of the minimum switching frequency. The adjustable upper stop being less precise to ±15%.

- **Low Startup Current:** When directly powered from the high−voltage DC rail, the device only requires 300 μA to startup. In case of an auxiliary supply, the B version offers a lower startup threshold to cope with a 12 V dc rail.

- **Brown−Out Detection:** To avoid operation from a low input voltage, it is interesting to prevent the controller from switching if the high−voltage rail is not within the right boundaries. Also, when teamed with a PFC front−end circuitry, the brown−out detection can ensure a clean startup sequence with soft−start, ensuring that the PFC is stabilized before energizing the resonant tank. The A version features a

28 μA hysteresis current for the lowest consumption and the B version slightly increases this current to 83 μA in order to improve the noise immunity.

- **Adjustable Fault Timer Duration:** When a fault is detected on the slow fault input or when the FB path is broken, a timer starts to charge an external capacitor. If the fault is removed, the timer opens the charging path and nothing happens. When the timer reaches its selected duration (via a capacitor on pin 6), all pulses are stopped. The controller now waits for the discharge via an external resistor of pin 6 capacitor to issue a new clean startup sequence with soft−start.

- **Cumulative Fault Events:** In the NCP1395A/B, the timer capacitor is not reset when the fault disappears. It actually integrates the information and cumulates the occurrences. A resistor placed in parallel with the capacitor will offer a simple way to adjust the discharge rate and thus the auto−recovery retry rate.

- **Fast and Slow Fault Detection:** In some application, subject to heavy load transients, it is interesting to give a certain time to the fault circuit, before activating the protection. On the other hand, some critical faults cannot accept any delay before a corrective action is taken. For this reason, the NCP1395A/B includes a fast fault and a slow fault input. Upon assertion, the fast fault immediately stops all pulses and stays in the position as long as the driving signal is high. When released low (the fault has gone), the controller has several choices: in the A version, pulses are back to a level imposed by the feedback pin without soft−start, but in the B version, pulses are back through a regular soft−start sequence.

- **Skip Cycle Possibility:** The absence of soft−start on the NCP1395A fast fault input offers an easy way to implement skip cycle when power saving features are necessary. A simple resistive connection from the feedback pin to the fast fault input, and skip can be implemented.

- **Onboard Transconductance Op Amp:** A transconductance amplifier is used to implement various options, like monitoring the output current and maintaining it constant.

- **Broken Feedback Loop Detection:** Upon startup or any time during operation, if the FB signal is missing, the timer starts to charge a capacitor. If the loop is really broken, the FB level does not grow up before the timer ends counting. The controller then stops all pulses and waits that the timer pin voltage collapses to 1.0 V typically before a new attempt to restart, via the soft−start. If the optocoupler is permanently broken, a hiccup takes place.

- **Finally, Two Circuit Versions, A and B:** The A and B versions differ because of the following changes:

  1. The startup thresholds are different, the A starts to pulse for $V_{CC} = 12.8$ V whereas the B pulses for $V_{CC} = 10$ V. The turn off levels are the same, however. The A is recommended for consumer products where the designer can use an external startup resistor, whereas the B is more recommended for industrial/medical applications where a 12 V auxiliary supply directly powers the chip.

  2. The A version does not activate the soft−start upon release of the fast fault input. This is to let the designer implement skip cycle. To the opposite, the B version goes back to operation upon the fast fault pin release via a soft−start sequence.

Voltage−Controlled Oscillator

The VCO section features a high−speed circuitry allowing an internal operation from 100 kHz up to 2.0 MHz. However, as a division by two internally creates the two Q and Qbar outputs, the final effective signal on output A and B switches between 50 kHz and 1.0 MHz. The VCO is configured in such a way that if the feedback pin goes up, the switching frequency also goes up. Figure 33 shows the architecture of this oscillator.
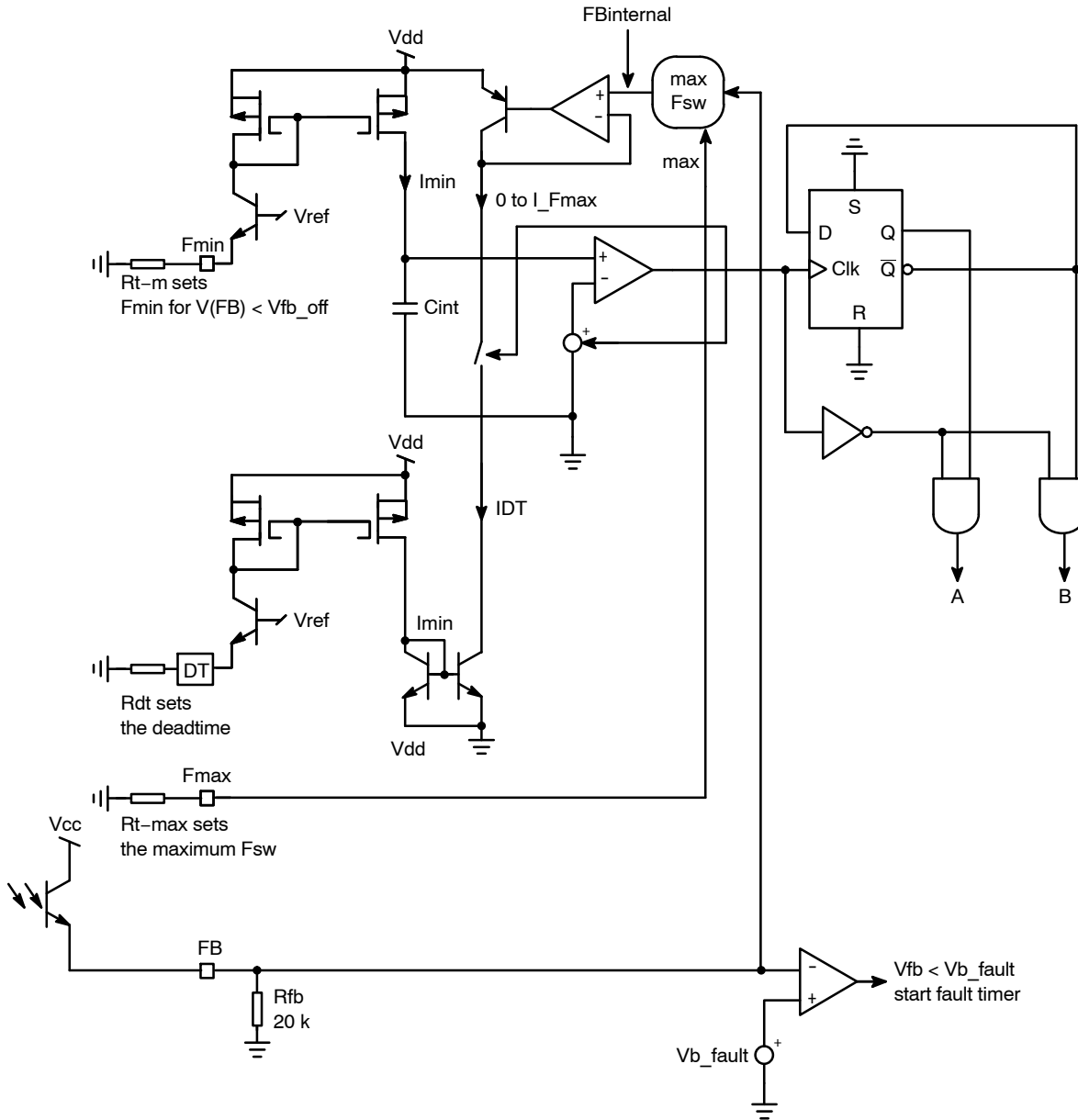

Figure 33. Simplified VCO Architecture

NCP1395A/B

The designer needs to program the maximum switching frequency and the minimum switching frequency. In LLC configurations, for circuits working above the resonant frequency, a high precision is required on the minimum frequency, hence the ±3% specification. This minimum switching frequency is actually reached when no feedback closes the loop. It can happen during the startup sequence, a strong output transient loading or in a short−circuit condition. By installing a resistor from pin 1 to AGND, the minimum frequency is set. Using the same philosophy, wiring a resistor from pin 2 to AGND will set the maximum frequency excursion. To improve the circuit protection features, we have purposely created a dead zone, where the feedback loop has no action. This is typically below 1.3 V. Figure 34 details the arrangement where the *internal* voltage (that drives the VCO) varies between 0 and 3.6 V. However, to create this swing, the feedback pin (to which the optocoupler emitter connects), will need to swing typically between 1.3 V and 6.0 V.
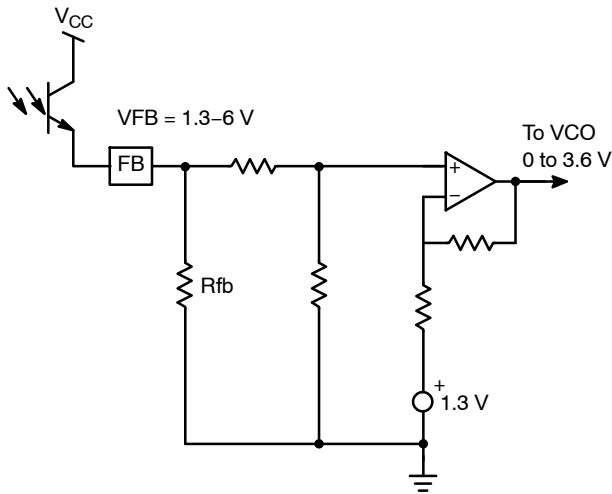
Figure 34. The OPAMP arrangement limits the VCO internal modulation signal between 0 and 5.0 V.

This technique allows us to detect a fault on the converter in case the FB pin cannot rise above 1.3 V (to actually close the loop) in less than a duration imposed by the programmable timer. Please refer to the fault section for detailed operation of this mode.

As shown in Figure 34, the *internal* dynamics of the VCO control voltage will be constrained between 0 V and 3.6 V, whereas the feedback loop will drive pin 5 (FB) between 1.3 V and 6.0 V. If we take the external excursion numbers, 1.3 V = 50 kHz, 6.0 V = 1.0 MHz, then the VCO slope will then be $\frac{1\ \text{Meg}-50\ \text{k}}{4.7}$ = 202 kHz/V.

Figures 35 and 36 portray the frequency evolution depending on the feedback pin voltage level in a different frequency clamp combination.
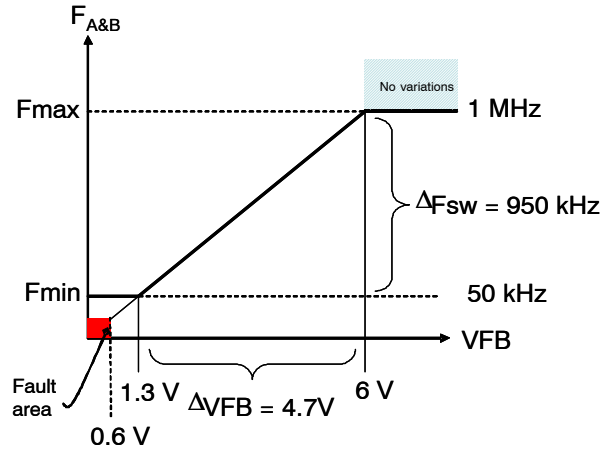

Figure 35. Maximal default excursion, Rt = 120 kΩ on pin 1 and Rfmax = 35 kΩ on pin 2.
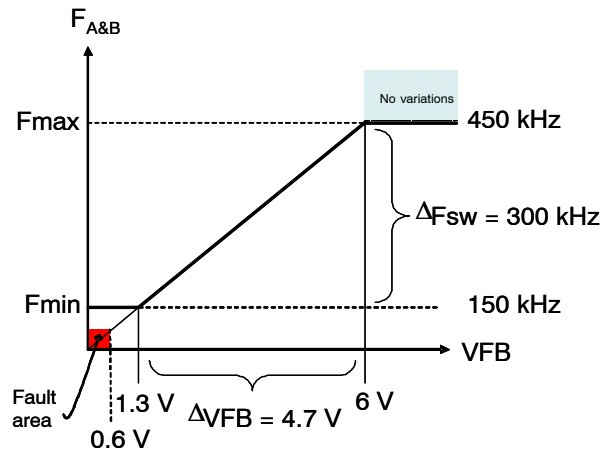

Figure 36. Here a different minimum frequency was programmed as well as a different maximum frequency excursion.

Please note that the previous small signal VCO slope has now been reduced to 300 k/5.0 = 62.5 kHz/V. This offers a mean to magnify the feedback excursion on systems where the load range does not generate a wide switching frequency excursion. Due to this option, we will see how it becomes possible to observe the feedback level and implement skip cycle at light loads. It is important to note that the frequency evolution does not have a real linear relationship with the feedback voltage. This is due to the deadtime presence which stays constant as the switching period changes.
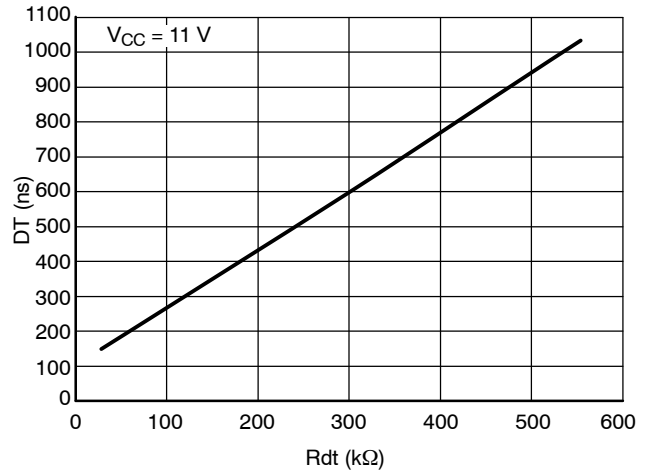
The selection of the three setting resistors (Fmax, Fmin and deadtime) requires the usage of the selection charts displayed below:
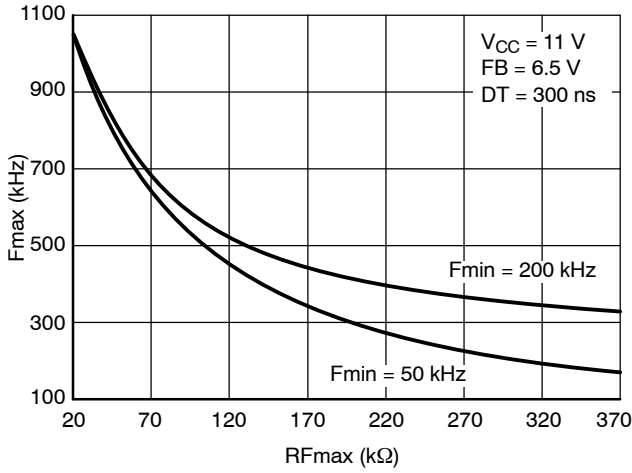
Figure 37. Maximum switching frequency resistor selection depending on the adopted minimum switching frequency.
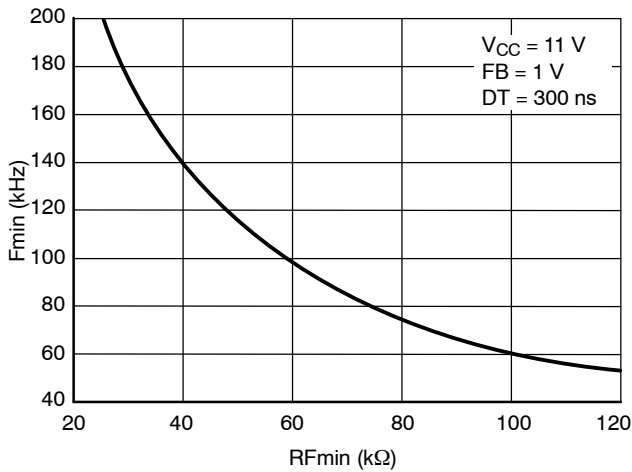

Figure 38. Minimum Switching Frequency Resistor Selection

Figure 39. Dead−Time Resistor Selection

ORing Capability

If for a particular reason, there is a need for having a frequency variation linked to an event appearance (instead of abruptly stopping pulses), then the FB pin lends itself very well to the addition of other sweeping loops. Several diodes can easily be used to perform the job in case of reaction to a fault event or to regulate on the output current (CC operation). Figure 40 shows how to do it.
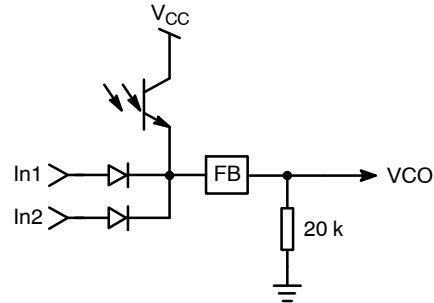
Figure 40. Due to the FB configuration, loop ORing is easy to implement.

Deadtime Control

Deadtime control is an absolute necessity when the half−bridge configuration comes to play. The deadtime technique consists of inserting a period during which both high and low side switches are off. Of course, the deadtime amount differs depending on the switching frequency, hence the ability to adjust it on this controller. The option ranges between 150 ns and 1.0 μs. The deadtime is actually made by controlling the oscillator discharge current. Figure 41 portrays a simplified VCO circuit based on Figure 33.
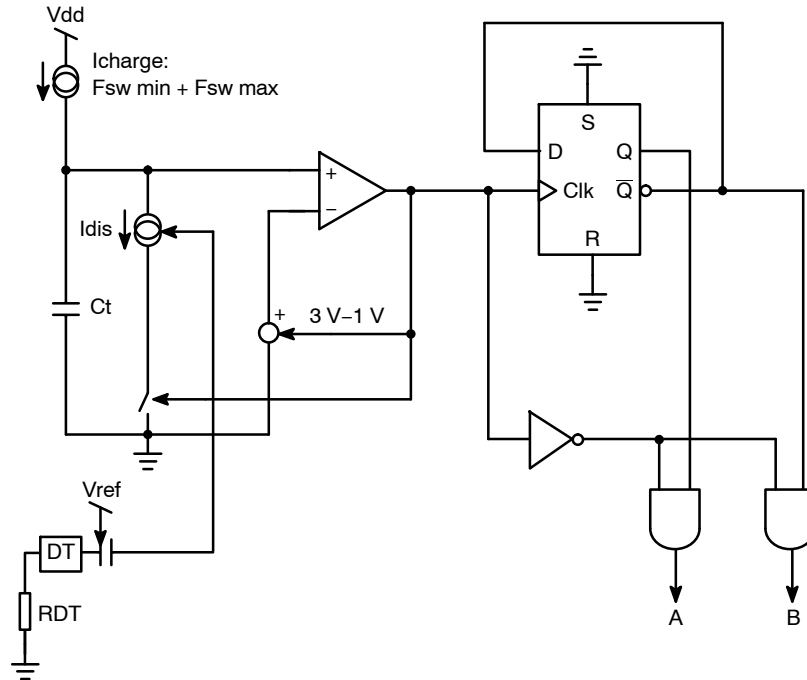
Figure 41. Deadtime Generation

During the discharge time, the clock comparator is high and unvalidates the AND gates: both outputs are low. When the comparator goes back to the high level, during the timing capacitor Ct recharge time, A and B outputs are validated. By connecting a resistor RDT to ground, it creates a current whose image serves to discharge the Ct capacitor: we control the deadtime. The typical range evolves between 150 ns (RDT = 30 kΩ) and 1.0 μs (RDT = 600 kΩ). Figure 44 shows the typical waveforms obtained on the output.

Soft−Start Sequence

In resonant controllers, a soft−start is needed to avoid suddenly applying the full current into the resonating circuit. In this controller, a soft−start capacitor connects to pin 4 and offers a smooth frequency variation upon startup: when the circuit starts to pulse, the VCO is pushed to the maximum switching frequency imposed by pin 2. Then, it linearly decreases its frequency toward the minimum frequency selected by a resistor on pin 1. Of course, practically, the feedback loop is suppose to take over the VCO lead as soon as the output voltage has reached the target. If not, then the minimum switching frequency is reached and a fault is detected on the feedback pin (typically below 600 mV). Figure 43 depicts a typical frequency evolution with soft−start.
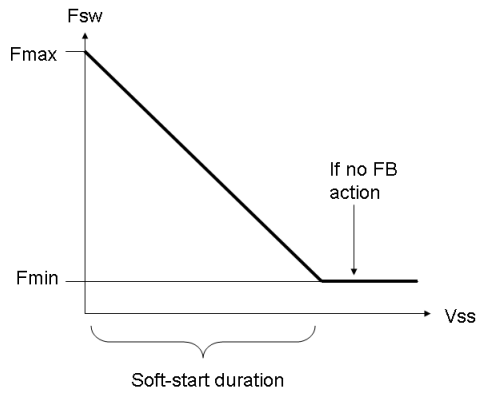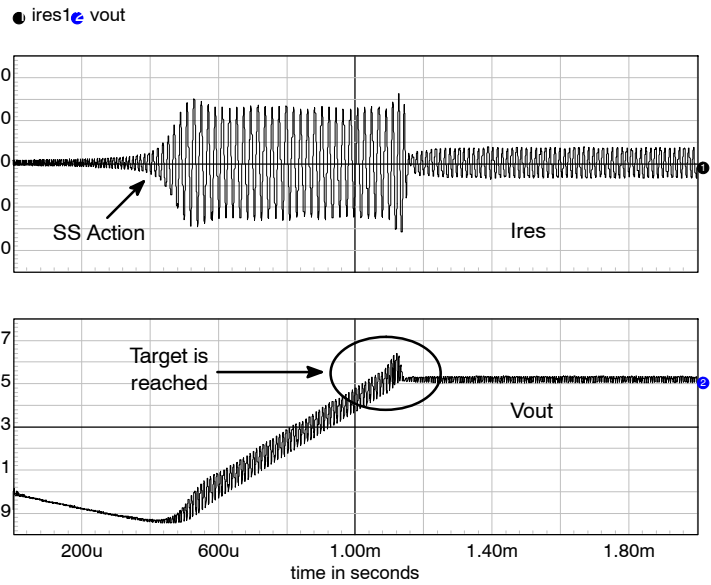
Figure 42. Soft−Start Behavior

Figure 43. A Typical Startup Sequence on an LLC Converter

Please note that the soft−start will be activated in the following conditions:

- A startup sequence
- During auto−recovery burst mode
- A brown−out recovery
- A temperature shutdown recovery

The fast fault input undergoes a special treatment. Since we want to implement skip cycle through the fast fault input on the NCP1395A, we cannot activate the soft−start every time the feedback pin stops the operations in low power mode. Therefore, when the fast fault pin is released,

no soft−start occurs to offer the best skip cycle behavior. However, it is very possible to combine skip cycle and true fast fault input, e.g. via ORing diodes driving pin 13. In that case, if a signal maintains the fast fault input high long enough to bring the feedback level down (that is to say below 0.6 V) since the output voltage starts to fall down, then the soft−start is activated after the release of the pin.

In the B version tailored to operate from an auxiliary 12 V power supply, the soft−start is always activated upon the fast fault input release, whatever the feedback condition is.

❶ vct   ❷ clock   ❺ difference
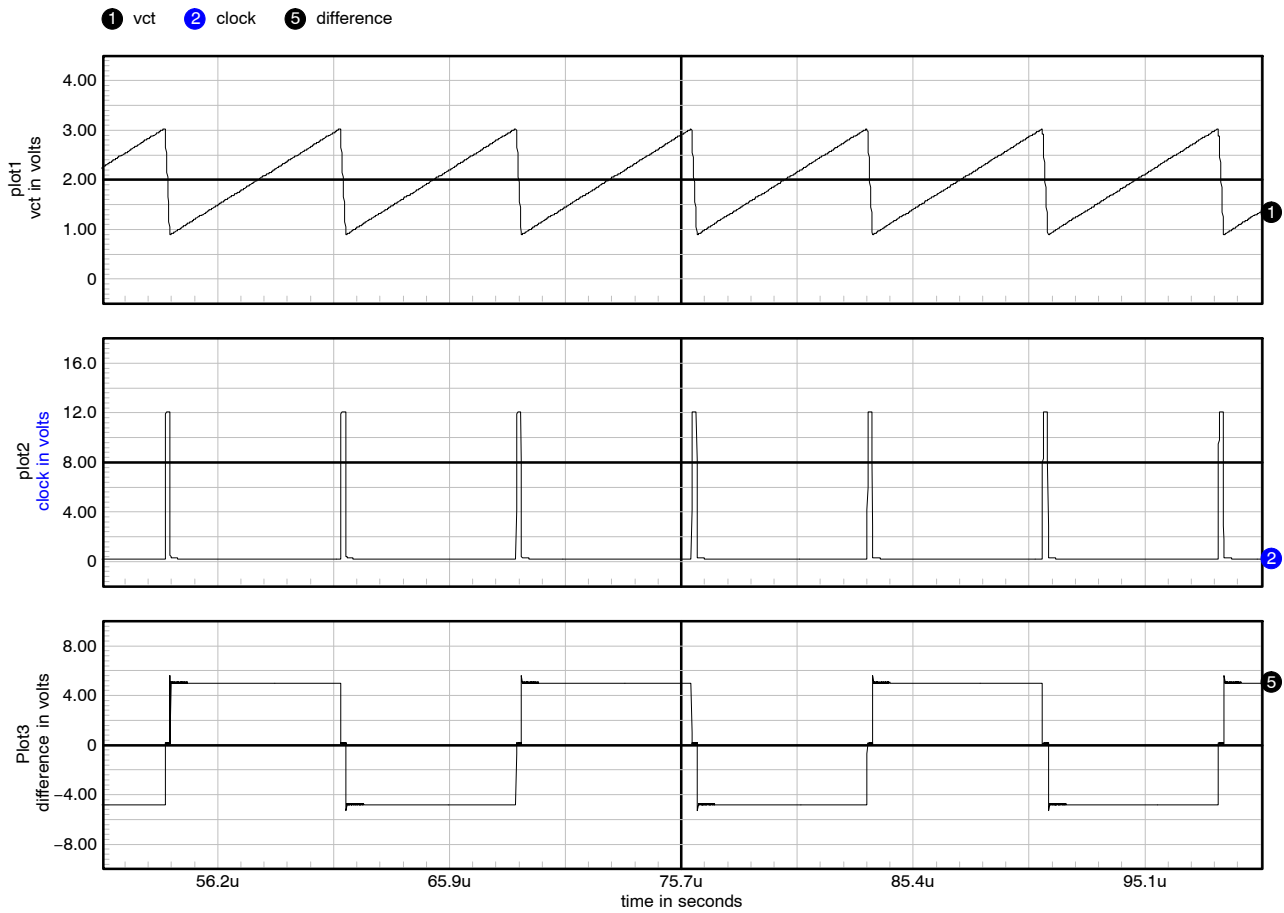
Figure 44. Typical Oscillator Waveforms

Brown−Out Protection

The Brown−Out circuitry (BO) offers a way to protect the resonant converter from low DC input voltages. Below a given level, the controller blocks the output pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 42, offers a possibility to observe the high−voltage (HV) rail. A resistive divider made of Rupper and Rlower, brings a portion of the HV rail on pin 7. Below the turn−on level, a current source IBO is off. Therefore, the turn−on level solely depends on the division ratio brought by the resistive divider.
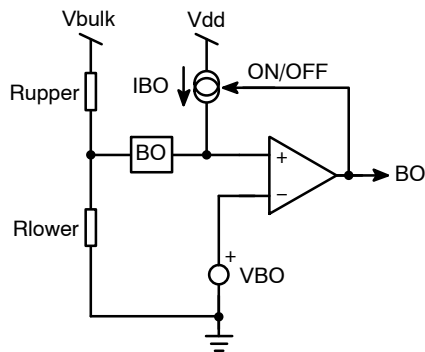
Figure 45. The Internal Brown−Out Configuration with an Offset Current Source
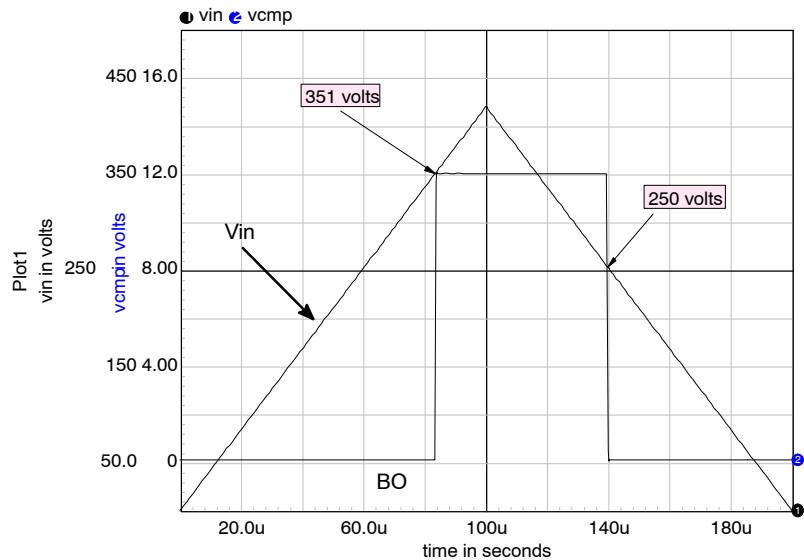
Figure 46. Simulation Results for 350/250 ON/OFF Levels

To the contrary, when the internal BO signal is high (A and B pulse), the IBO source is activated and creates a hysteresis. The hysteresis level actually depends on the circuit: NCP1395A features a 28 μA whereas the NCP1395B uses a 83 μA current. Changes are

implemented to a) reduce the standby power on the NCP1395A b) improve the noise immunity on the NCP1395B. Knowing these values, it becomes possible to select the turn−on and turn−off levels via a few lines of algebra:

IBO is off

$$V(+) = Vbulk1 \times \frac{Rlower}{Rlower + Rupper} \qquad \text{(eq. 1)}$$

IBO is on

$$V(+) = Vbulk2 \times \frac{Rlower}{Rlower + Rupper} + IBO \times \left(\frac{Rlower \times Rupper}{Rlower + Rupper}\right) \qquad \text{(eq. 2)}$$

We can now extract Rlower from Equation 1 and plug it into Equation 2, then solve for Rupper:

$$Rupper = Rlower \times \frac{Vbulk1 - VBO}{VBO}$$

$$Rlower = VBO \times \frac{Vbulk1 - Vbulk2}{IBO \times (Vbulk1 - VBO)}$$

If we decide to turn on our converter for Vbulk1 equals 350 V, and turn it off for Vbulk2 equals 250 V, then we obtain:

IBO = 28 μA

Rupper = 3.6 MΩ

Rlower = 10 kΩ

The bridge power dissipation is $400^2/3.601$ MΩ = 45 mW when the front−end PFC stage delivers 400 V.

IBO = 83 μA

Rupper = 1.2 MΩ

Rlower = 3.4 kΩ

The bridge power dissipation is 132 mW when the front−end PFC stage delivers 400 V. Figure 46 simulation result confirms our calculations.

Latch−Off Protection

There are some situations where the converter shall be fully turned off and stay latched. This can happen in presence of an overvoltage (the feedback loop is drifting) or when an overtemperature is detected. Due to the addition of a comparator on the BO pin, a simple external circuit can lift up this pin above VLATCH (5.0 V typical) and permanently disable pulses. The V_{CC} needs to be cycled down below 5.0 V typically to reset the controller.
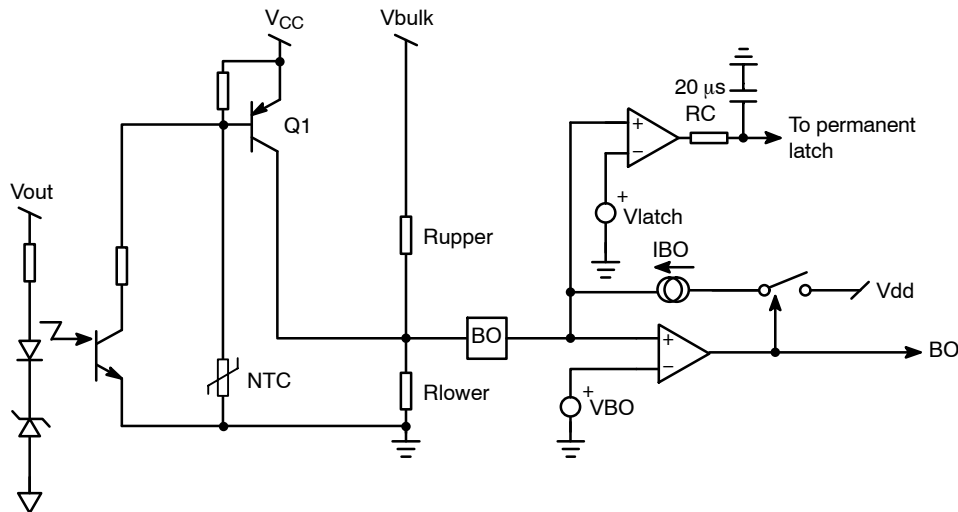

Figure 47. Adding a comparator on the BO pin offers a way to latch−off the controller.

In Figure 47, Q1 is blocked and does not bother the BO measurement as long as the NTC and the optocoupler are not activated. As soon as the secondary optocoupler senses

an OVP condition, or the NTC reacts to a high ambient temperature, Q1 base is brought to ground and the BO pin goes up, permanently latching off the controller.

Protection Circuitry

This resonant controller differs from competitors due to its protection features. The device can react to various inputs like:

- *Fast events input:* Like an overcurrent condition, a need to shutdown (sleep mode) or a way to force a controlled burst mode (skip cycle at low output power): as soon as the input level exceeds 1.0 V typical, pulses are immediately stopped. On the A version, when the input is released, the controller performs a clean startup sequence without soft−start unless the feedback voltage goes down below 0.6 V

during fault time (please see above for details). The B version restarts with a soft−start sequence.

- *Slow events input:* This input serves as a delayed shutdown, where an event like a transient overload does not immediately stopped pulses but start a timer. If the event duration lasts longer than what the timer imposes, then all pulses are disabled. The voltage on the timer capacitor (pin 3) starts to decrease until it reaches 1.0 V. The decrease rate is actually depending on the resistor the user will put in parallel with the capacitor, giving another flexibility during design.

Figure 48 depicts the architecture of the fault circuitry.
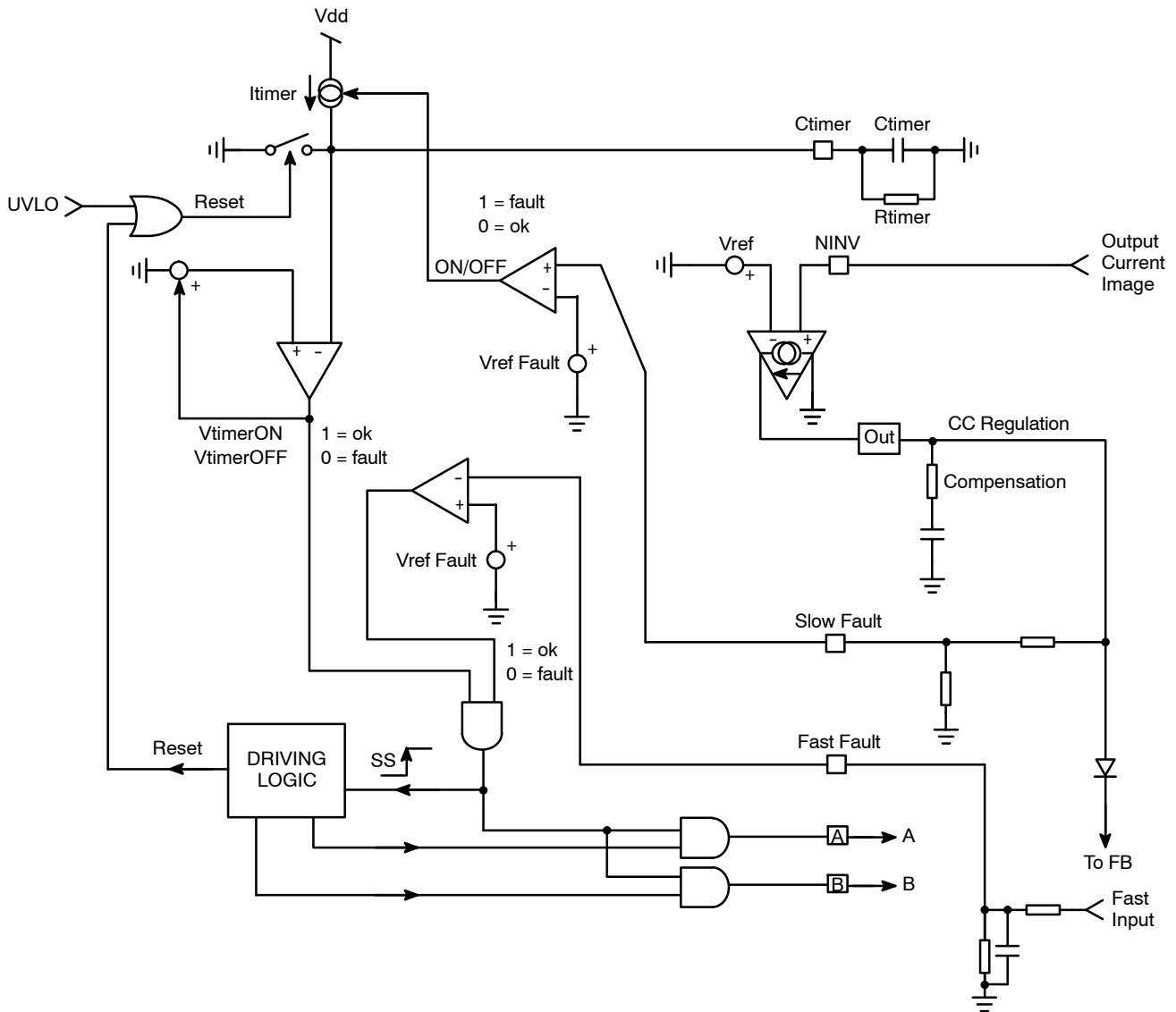
Figure 48. This Circuit Combines a Slow and Fast Input for Improved Protection Features

In this figure, the internal OPAMP is used to perform a kind of constant current operation (CC) by taking the lead when the other voltage loop is gone (CV). Due to the ORing capability on the FB pin, the OPAMP regulates in constant current mode. When the output reaches a low level close to a complete short−circuit, the OPAMP output is maximum. With a resistive divider on the slow fault, this condition can be detected to trigger the delayed fault. If no OPAMP shall be used, its input must be grounded.

Slow Input

On this circuit, the slow input goes to a comparator. When this input exceeds 1.0 V typical, the current source Itimer turns on, charging the external capacitor Ctimer. If the fault duration is long enough, when Ctimer voltage reaches the VtimerON level (4.0 V typical), then all pulses are stopped. Itimer turns off and the capacitor slowly discharges to ground via a resistor installed in parallel with it. As a result, the designer can easily determine the time during which the power supply stays locked by playing on Rtimer. Now, when the timer capacitor voltage reaches 1.0 V typical (VtimerOFF), the comparator instructs the internal logic to issues pulses as on a clean soft−start sequence (soft−start is activated). Please note that the discharge resistor cannot be lower than 4.0 V/Itimer, otherwise the voltage on Ctimer will never reach the turn−off voltage of 4.0 V.

In both cases, when the fault is validated, both outputs A and B are internally pulled down to ground.
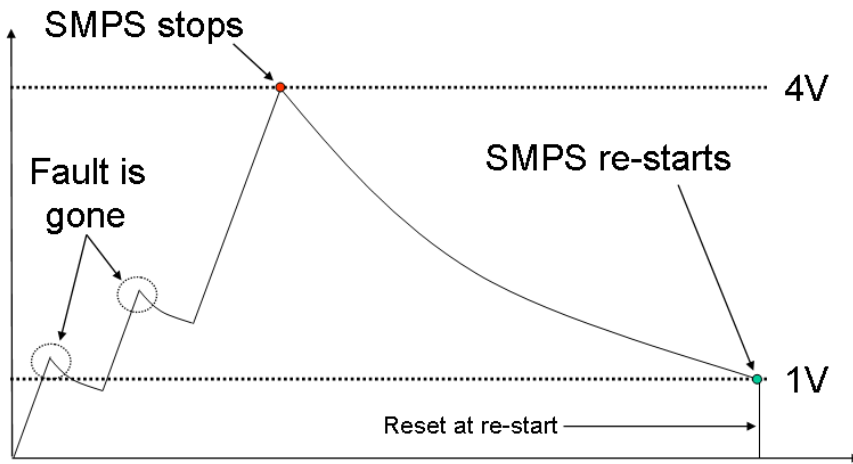
Figure 49. A resistor can easily program the capacitor discharge time.
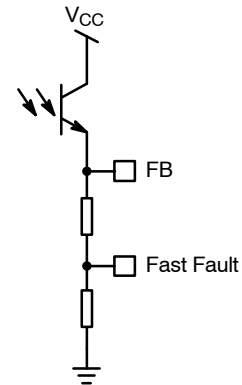
Figure 50. Skip cycle can be implemented via two resistors on the FB pin to the fast fault input.

Fast Input

The fast input is not affected by a delayed action. As soon as its voltage exceeds 1.0 V typical, all pulses are off and maintained off as long as the fault is present. When the pin is released, pulses come back without soft−start for the A version, with soft−start for the B version.

Due to the low activation level of 1.0 V, this pin can observe the feedback pin via a resistive divided and thus implement skip cycle operation. The resonant converter can be designed to lose regulation in light load conditions, forcing the FB level to increase. When it reaches the programmed level, it triggers the fast fault input and stops pulses. Then V_{out} slowly drops, the loop reacts by decreasing the feedback level which, in turn, unlocks the pulses: Vout goes up again and so on: we are in skip cycle mode.

Startup Behavior

When the V_{CC} voltage grows up, the internal current consumption is kept to Istup, allowing to crank up the converter via a resistor connected to the bulk capacitor. When V_{CC} reaches the V_{CC}ON level, output A goes high first and then output B. This sequence will always be the same, whatever triggers the pulse delivery: fault, OFF to ON etc… Pulsing the output A high first gives an immediate charge of the bootstrap capacitor when an integrated high voltage half−bridge driver is implemented such as ON Semiconductor's NCP5181. Then, the rest of pulses follow, delivered at the highest switching value, set by the resistor on pin 2. The soft−start capacitor ensures a smooth frequency decrease to either the programmed minimum value (in case of fault) or to a value corresponding to the operating point if the feedback loop closes first. Figure 51 shows typical signals evolution at power on.
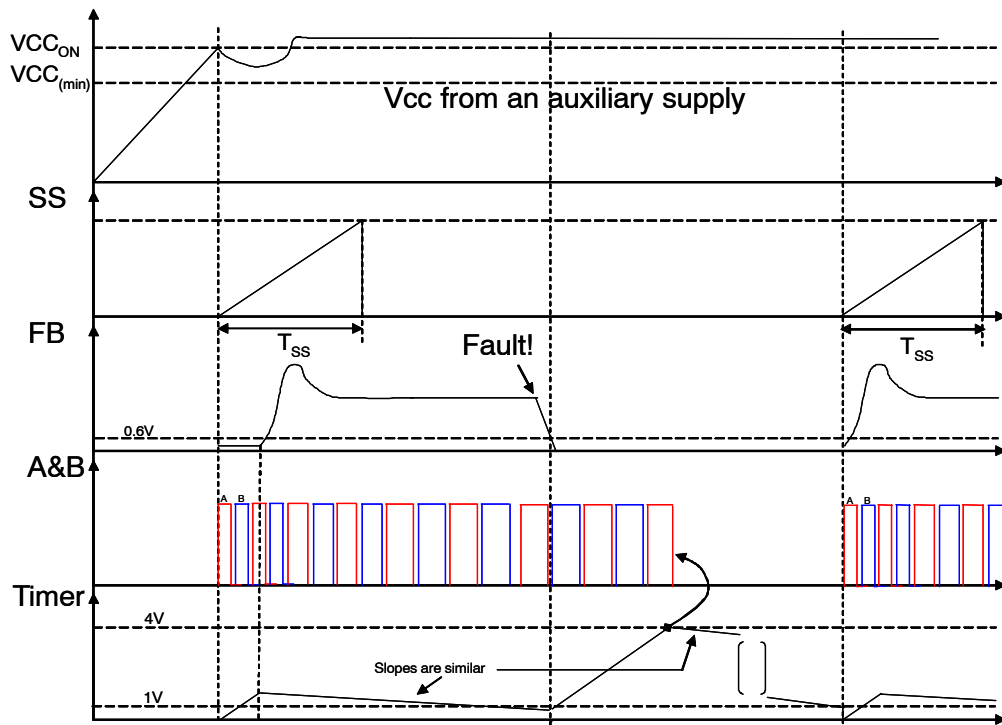
Figure 51. At power on, output A is first activated and the frequency slowly decreases via the soft−start capacitor.

Figure 51 depicts an auto−recovery situation, where the timer has triggered the end of output pulses. In that case, the V_{CC} level was given by an auxiliary power supply, hence its stability during the hiccup. A similar situation can arise if the user selects a more traditional startup method, with an auxiliary winding. In that case, the $VCC_{(min)}$ comparator stops the output pulses whenever it is activated,

that is to say, when V_{CC} falls below 10.3 V typical. At this time, the V_{CC} pin still receives its bias current from the startup resistor and heads toward VCC_{ON} via the Vcc capacitor. When the voltage reaches VCC_{ON}, a standard sequence takes place, involving a soft−start. Figure 52 portrays this behavior.
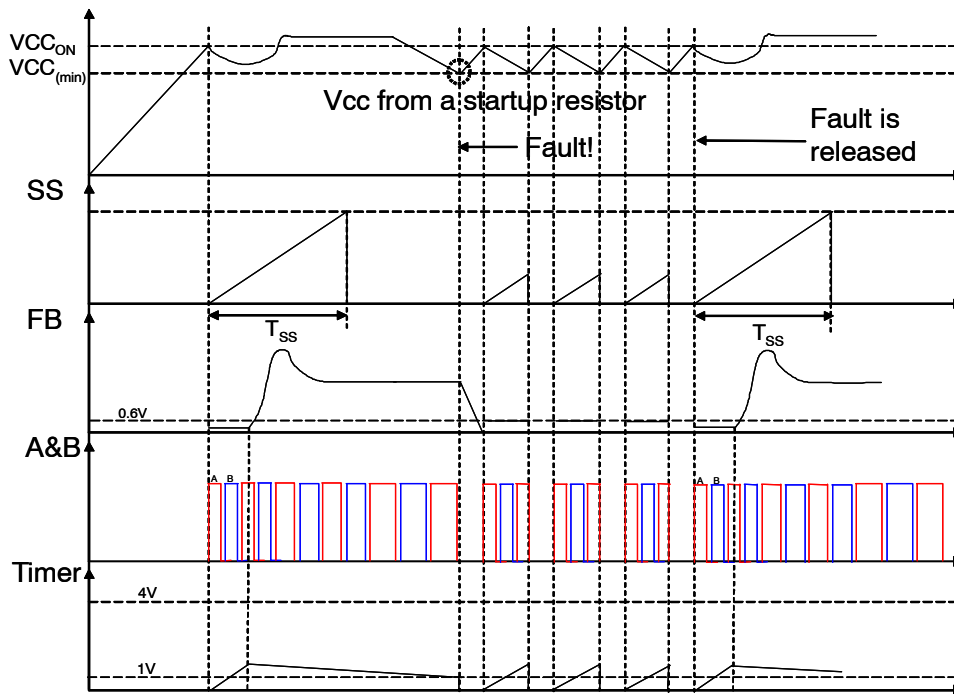
Figure 52. When the V$_{CC}$ is too low, all pulses are stopped until V$_{CC}$ goes back to the startup voltage.

As described in the data sheet, two startup levels VCC$_{ON}$ are available, via two circuit versions. The NCP1395A features a large hysteresis to allow a classical startup method with a resistor connected to the bulk capacitor. Then, at the end of the startup sequence, an auxiliary winding is supposed to take over the controller supply voltage. To the opposite, for applications where the resonant controller is powered from a standby power supply, the startup level of the NCP1395B of 10 V typically allows a direct a connection from a 12 V source. Simple ON/OFF operation is therefore feasible.

ORDERING INFORMATION

Device	Package	Shipping†
NCP1395APG	PDIP−16 (Pb−Free)	25 Units / Rail
NCP1395ADR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
NCP1395BPG	PDIP−16 (Pb−Free)	25 Units / Rail
NCP1395BDR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
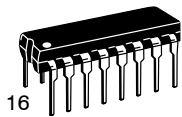
PDIP−16
CASE 648−08
ISSUE V

DATE 22 APR 2015

SCALE 1:1

TOP VIEW

END VIEW
WITH LEADS CONSTRAINED
NOTE 5

SIDE VIEW

⊕ 0.010 Ⓜ C A Ⓜ B Ⓜ

END VIEW
NOTE 6
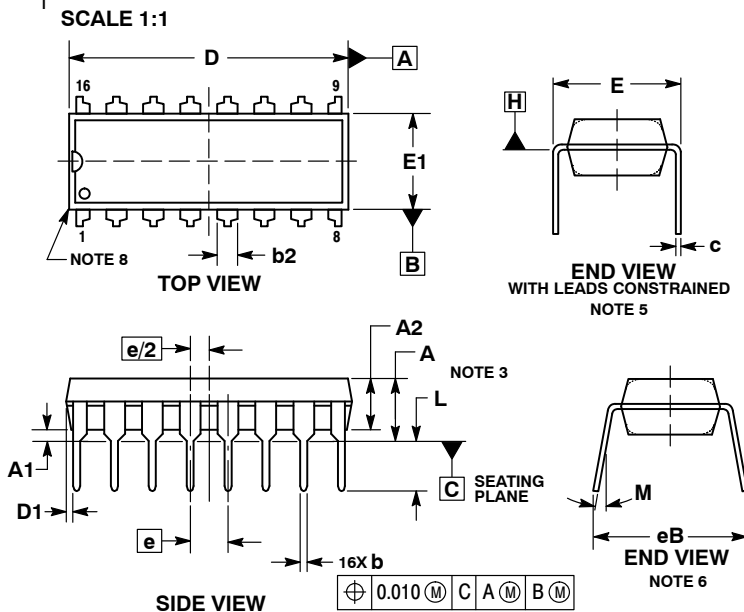
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-AGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-----	0.210	---	5.33
A1	0.015	-----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	-----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	-----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	-----	10°	---	10°

GENERIC
MARKING DIAGRAM*

XXXXXXXXXXX
XXXXXXXXXXX
AWLYYWWG
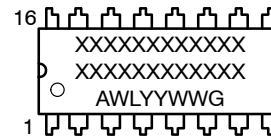
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

STYLE 1:
PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 2:
PIN 1.	COMMON DRAIN
2.	COMMON DRAIN
3.	COMMON DRAIN
4.	COMMON DRAIN
5.	COMMON DRAIN
6.	COMMON DRAIN
7.	COMMON DRAIN
8.	COMMON DRAIN
9.	GATE
10.	SOURCE
11.	GATE
12.	SOURCE
13.	GATE
14.	SOURCE
15.	GATE
16.	SOURCE

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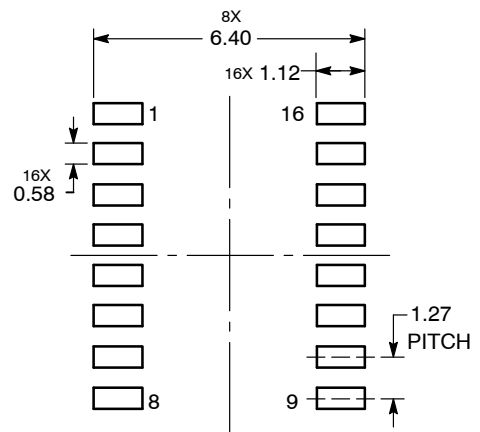ISSUE K

SCALE 1:1

DATE 29 DEC 2006
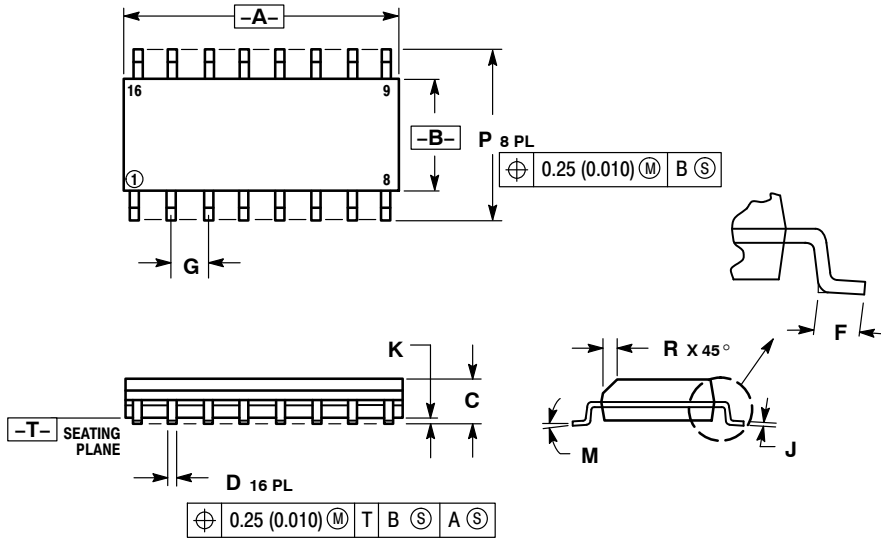
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

⊕ 0.25 (0.010) Ⓜ B Ⓢ

−T− SEATING PLANE

⊕ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT

8X 6.40

16X 1.12

16X 0.58

1.27 PITCH

DIMENSIONS: MILLIMETERS

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