NCP1271

PWM Controller, Soft-Skip ™ Standby, with Adjustable Skip Level and External Latch

The NCP1271 represents a new, pin to pin compatible, generation of the successful 7−pin current mode NCP12XX product series. The controller allows for excellent stand by power consumption by use of its adjustable Soft−Skip mode and integrated high voltage startup FET. This proprietary Soft−Skip also dramatically reduces the risk of acoustic noise. This allows the use of inexpensive transformers and capacitors in the clamping network. Internal frequency jittering, ramp compensation, timer−based fault detection and a latch input make this controller an excellent candidate for converters where ruggedness and component cost are the key constraints.

Features

- Fixed−Frequency Current−Mode Operation with Ramp Compensation and Skip Cycle in Standby Condition
- Timer−Based Fault Protection for Improved Overload Detection
- “Soft−Skip Mode” Technique for Optimal Noise Control in Standby
- Internal High−Voltage Startup Current Source for Lossless Startup
- ±5% Current Limit Accuracy over the Full Temperature Range
- Adjustable Skip Level
- Internal Latch for Easy Implementation of Overvoltage and Overtemperature Protection
- Frequency Jittering for Softened EMI Signature
- +500 mA/−800 mA Peak Current Drive Capability
- Sub−100 mW Standby Power can be Achieved
- Pin−to−Pin Compatible with the Existing NCP120X Series
- This is a Pb−Free Device

Typical Applications

- AC−DC Adapters for Notebooks, LCD Monitors
- Offline Battery Chargers
- Consumer Electronic Appliances STB, DVD, DVDR

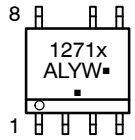
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

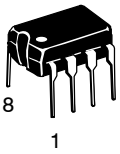
ON Semiconductor®

http://onsemi.com

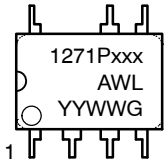
MARKING DIAGRAMS

SOIC−7
D SUFFIX
CASE 751U





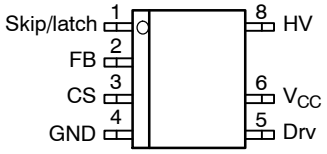
PDIP−7 VHVIC
P SUFFIX
CASE 626B



x	= A or B A= 65 kHz B= 100 kHz
xxx	= Device Code: 65, 100
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
▪ or G	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

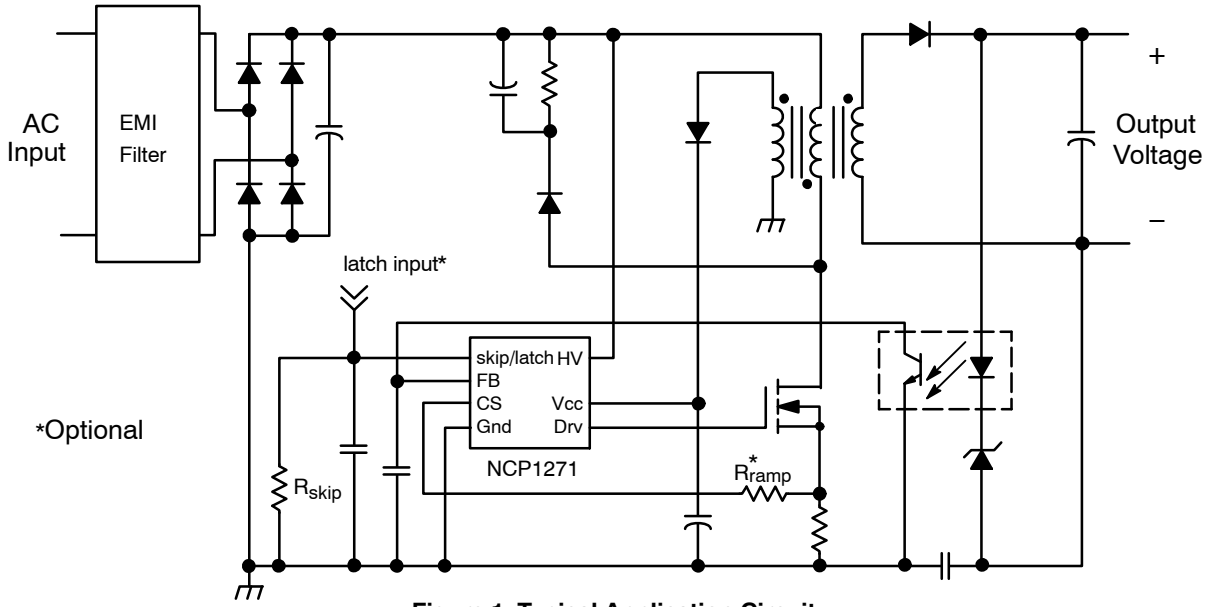


Figure 1. Typical Application Circuit

MAXIMUM RATINGS (Notes 1 and 2)

Rating	Symbol	Value	Unit
V_{CC} Pin (Pin 6)			
Maximum Voltage Range	V_{max}	−0.3 to +20	V
Maximum Current	I_{max}	100	mA
Skip/Latch, FB, CS Pin (Pins 1−3)			
Maximum Voltage Range	V_{max}	−0.3 to +10	V
Maximum Current	I_{max}	100	mA
Drv Pin (Pin 5)			
Maximum Voltage Range	V_{max}	−0.3 to +20	V
Maximum Current	I_{max}	−800 to +500	mA
HV Pin (Pin 8)			
Maximum Voltage Range	V_{max}	−0.3 to +500	V
Maximum Current	I_{max}	100	mA
Power Dissipation and Thermal Characteristics			
Thermal Resistance, Junction−to−Air, PDIP−7, Low Conductivity PCB (Note 3)	$R_{\theta JA}$	142	°C/W
Thermal Resistance, Junction−to−Lead, PDIP−7, Low Conductivity PCB	$R_{\theta JL}$	57	°C/W
Thermal Resistance, Junction−to−Air, PDIP−7, High Conductivity PCB (Note 4)	$R_{\theta JA}$	120	°C/W
Thermal Resistance, Junction−to−Lead, PDIP−7, High Conductivity PCB	$R_{\theta JL}$	56	°C/W
Thermal Resistance, Junction−to−Air, SO−7, Low Conductivity PCB (Note 3)	$R_{\theta JA}$	177	°C/W
Thermal Resistance, Junction−to−Lead, SO−7, Low Conductivity PCB	$R_{\theta JL}$	75	°C/W
Thermal Resistance, Junction−to−Air, SO−7, High Conductivity PCB (Note 4)	$R_{\theta JA}$	136	°C/W
Thermal Resistance, Junction−to−Lead, SO−7, High Conductivity PCB	$R_{\theta JL}$	69	°C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Maximum Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Protection			
Human Body Model ESD Pins 1−6	HBM	2000	V
Human Body Model ESD Pin 8	HBM	700	V
Machine Model ESD Pins 1−4, 8	MM	200	V
Machine Model ESD Pins 5, 6	MM	150	V
Charged Device Model ESD	CDM	1000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. ESD protection per JEDEC JESD22−A114−F for HBM, per JEDEC JESD22−A115−A for MM, and per JEDEC JESD22−C101D for CDM. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.
2. Guaranteed by design, not tested.
3. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 80 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection or zero air flow.

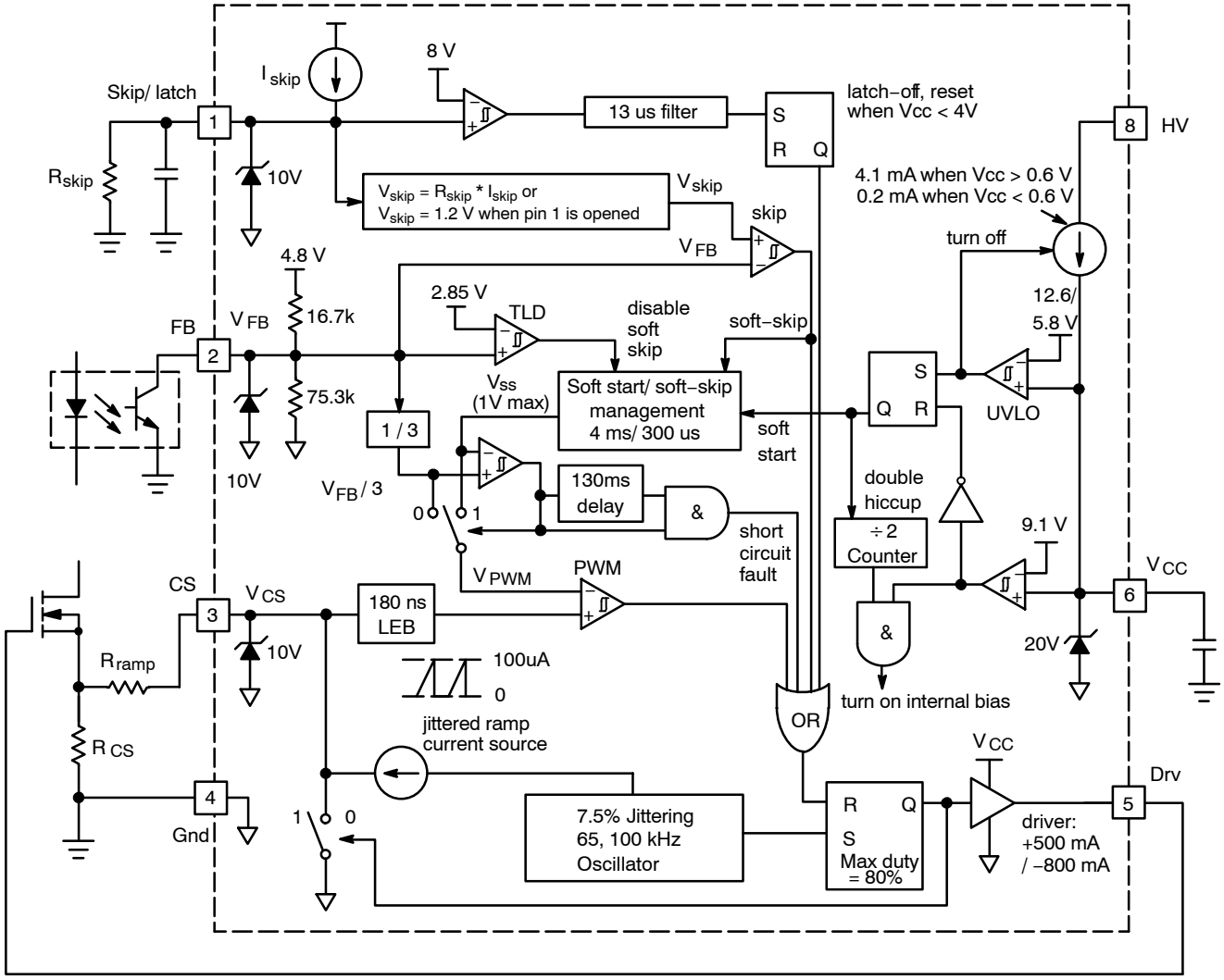


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description
1	Skip/latch	Skip Adjust or Latchoff	A resistor to ground provides the adjustable standby skip level. Additionally, if this pin is pulled higher than 8.0 V (typical), the controller latches off the drive.
2	FB	Feedback	An optocoupler collector pulls this pin low during regulation. If this voltage is less than the Skip pin voltage, then the driver is pulled low and Soft−Skip mode is activated. If this pin is open (>3 V) for more than 130 ms, then the controller is placed in a fault mode.
3	CS	Current Sense	This pin senses the primary current for PWM regulation. The maximum primary current is limited to 1.0 V / R_{CS} where R_{CS} is the current sense resistor. Additionally, a ramp resistor R_{ramp} between the current sense node and this pin sets the compensation ramp for improved stability.
4	Gnd	IC Ground	–
5	Drv	Driver Output	The NCP1271's powerful output is capable of driving the gates of large Qg MOSFETs.
6	V_{CC}	Supply Voltage	This is the positive supply of the device. The operating range is between 10 V (min) and 20 V (max) with a UVLO start threshold 12.6 V (typ).
8	HV	High Voltage	This pin provides (1) Lossless startup sequence (2) Double hiccup fault mode (3) Memory for latch−off shutdown and (4) Device protection if V_{CC} is shorted to GND.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values, T_J = −40°C to +125°C, V_{CC} = 14 V, HV = open, skip = open, FB = 2 V, CS = Ground, DRV = 1 nF, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Oscillation Frequency (65 kHz Version, T_J = 25°C) Oscillation Frequency (65 kHz Version, T_J = −40 to + 85°C) Oscillation Frequency (65 kHz Version, T_J = −40 to + 125°C) Oscillation Frequency (100 kHz Version, T_J = 25°C) Oscillation Frequency (100 kHz Version, T_J = −40 to +85°C) Oscillation Frequency (100 kHz Version, T_J = −40 to +125°C)	5	f_{osc}	61.75 58 55 95 89 85	65 65 65 100 100 100	68.25 69 69 105 107 107	kHz
Oscillator Modulation Swing, in Percentage of f_{osc}	5	–	–	±7.5	–	%
Oscillator Modulation Swing Period	5	–	–	6.0	–	ms
Maximum Duty Cycle (V_{CS} = 0 V, V_{FB} = 2.0 V)	5	D_{max}	75	80	85	%
GATE DRIVE						
Gate Drive Resistance Output High (V_{CC} = 14 V, Drv = 300 Ω to Gnd) Output Low (V_{CC} = 14 V, Drv = 1.0 V)	5	 R_{OH} R_{OL}	 6.0 2.0	 11 6.0	 20 12	Ω
Rise Time from 10% to 90% (Drv = 1.0 nF to Gnd)	5	t_r	–	30	–	ns
Fall Time from 90% to 10% (Drv = 1.0 nF to Gnd)	5	t_f	–	20	–	ns
CURRENT SENSE						
Maximum Current Threshold	3	I_{Limit}	0.95	1.0	1.05	V
Soft−Start Duration	–	t_{SS}	–	4.0	–	ms
Soft−Skip Duration	–	t_{SK}	–	300	–	μs
Leading Edge Blanking Duration	3	t_{LEB}	100	180	330	ns
Propagation Delay (Drv =1.0 nF to Gnd)	–	–	–	50	150	ns
Ramp Current Source Peak	3	$I_{ramp(H)}$	–	100	–	μA
Ramp Current Source Valley	3	$I_{ramp(L)}$	–	0	–	μA
SKIP						
Default Standby Skip Threshold (Pin 1 = Open)	2	V_{skip}	–	1.2	–	V
Skip Current (Pin 1 = 0 V, T_J = 25°C)	1	I_{skip}	26	43	56	μA
Skip Level Reset (Note 5)	1	$V_{skip-reset}$	5.0	5.7	6.5	V
Transient Load Detection Level to Disable Soft−Skip Mode	2	V_{TLD}	2.6	2.85	3.15	V
EXTERNAL LATCH						
Latch Protection Threshold	1	V_{latch}	7.1	8.0	8.7	V
Latch Threshold Margin ($V_{latch-m}$ = $V_{CC(off)}$ − V_{latch})	1	$V_{latch-m}$	0.6	1.2	–	V
Noise Filtering Duration	1	–	–	13	–	μs
Propagation Delay (Drv = 1.0 nF to Gnd)	1	T_{latch}	–	100	–	ns
SHORT−CIRCUIT FAULT PROTECTION						
Time for Validating Short−Circuit Fault Condition	2	$t_{protect}$	–	130	–	ms

5. Please refer to Figure 39 for detailed description.
6. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_J = 25°C, for min/max values, T_J = −40°C to +125°C, V_{CC} = 14 V, HV = open, skip = open, FB = 2 V, CS = Ground, DRV = 1 nF, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
STARTUP CURRENT SOURCE						
High−Voltage Current Source						
Inhibit Voltage (I_{CC} = 200 μA, HV = 50 V)	6	$V_{inhibit}$	190	600	800	mV
Inhibit Current (V_{CC} = 0 V, HV = 50 V)	6	$I_{inhibit}$	80	200	350	μA
Startup (V_{CC} = $V_{CC(on)}$ − 0.2 V, HV = 50 V)	6	I_{HV}	3.0	4.1	6.0	mA
Leakage (V_{CC} = 14 V, HV = 500 V)	8	$I_{HV-leak}$	10	25	50	μA
Minimum Startup Voltage (V_{CC} = $V_{CC(on)}$ − 0.2 V, I_{CC} = 0.5 mA)	8	$V_{HV(min)}$	–	20	28	V
SUPPLY SECTION						
V_{CC} Regulation	6					
Startup Threshold, V_{CC} Increasing		$V_{CC(on)}$	11.2	12.6	13.8	V
Minimum Operating Voltage After Turn−On		$V_{CC(off)}$	8.2	9.1	10	V
V_{CC} Operating Hysteresis		$V_{CC(on)}$ − $V_{CC(off)}$	3.0	3.6	4.2	V
Undervoltage Lockout Threshold Voltage, V_{CC} Decreasing		$V_{CC(latch)}$	5.0	5.8	6.5	V
Logic Reset Level ($V_{CC(latch)}$ −$V_{CC(reset)}$ > 1.0 V) (Note 7)		$V_{CC(reset)}$	–	4.0	–	V
V_{CC} Supply Current	6					
Operating (V_{CC} = 14 V, 1.0 nF Load, V_{FB} = 2.0 V, 65 kHz Version)		I_{CC1}	–	2.3	3.0	mA
Operating (V_{CC} = 14 V, 1.0 nF Load, V_{FB} = 2.0 V, 100 kHz Version)		I_{CC1}	–	3.1	3.5	mA
Output Stays Low (V_{CC} = 14 V, V_{FB} = 0 V)		I_{CC2}	–	1.3	2.0	mA
Latchoff Phase (V_{CC} = 7.0 V, V_{FB} = 2.0 V)		I_{CC3}	–	500	720	μA

7. Guaranteed by design.

TYPICAL CHARACTERISTICS

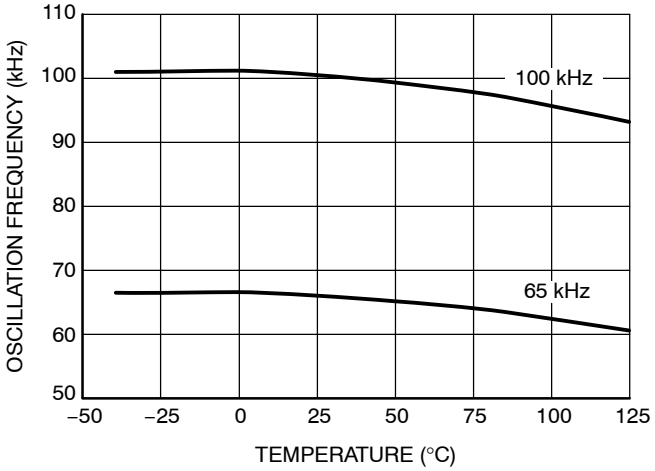


Figure 3. Oscillation Frequency vs. Temperature

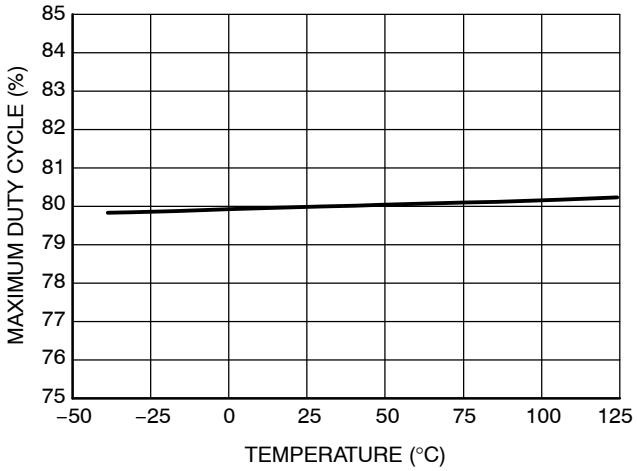


Figure 4. Maximum Duty Cycle vs. Temperature

TYPICAL CHARACTERISTICS

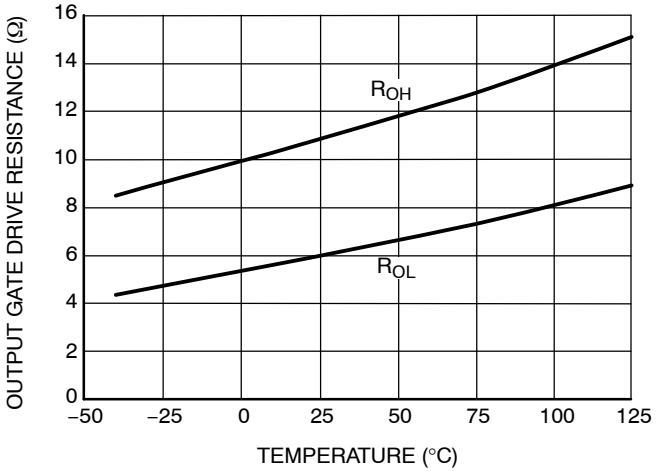


Figure 5. Output Gate Drive Resistance vs. Temperature

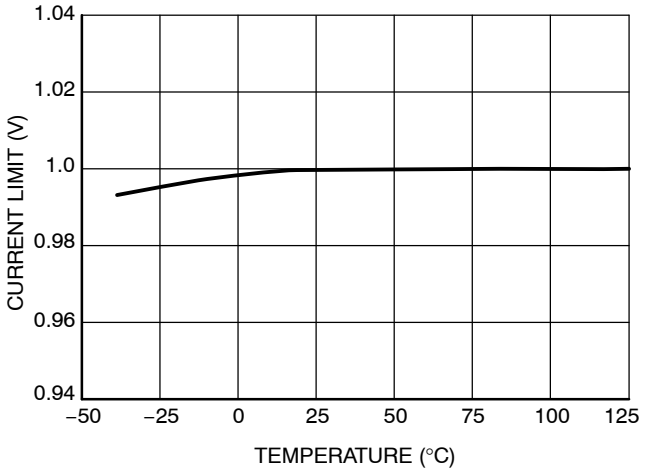


Figure 6. Current Limit vs. Temperature

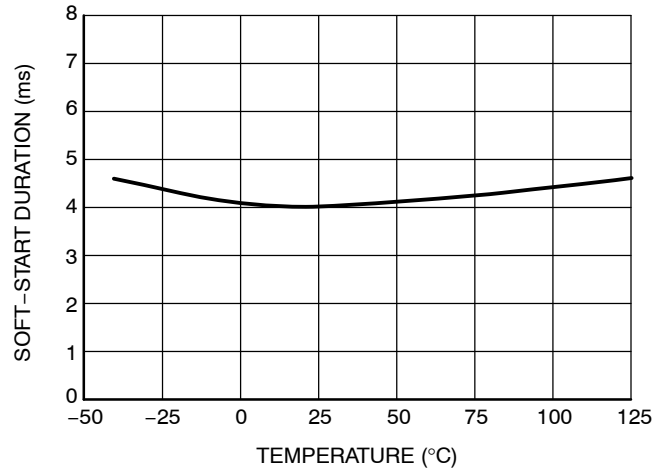


Figure 7. Soft−Start Duration vs. Temperature

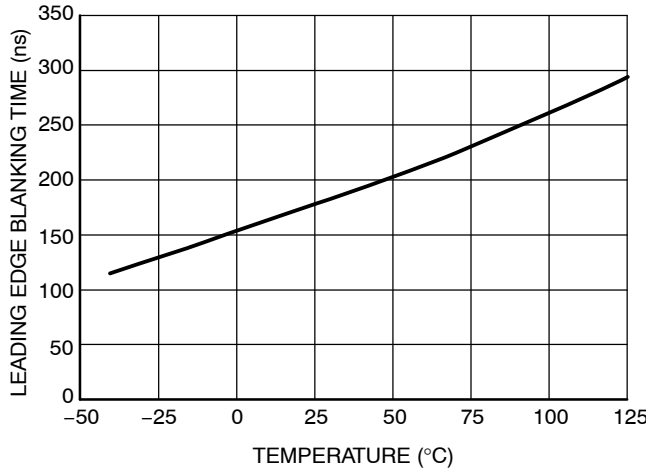


Figure 8. Leading Edge Blanking Time vs. Temperature

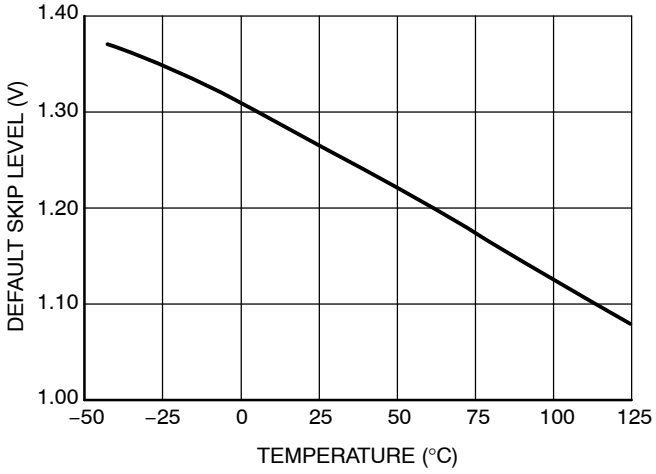


Figure 9. Default Skip Level vs. Temperature

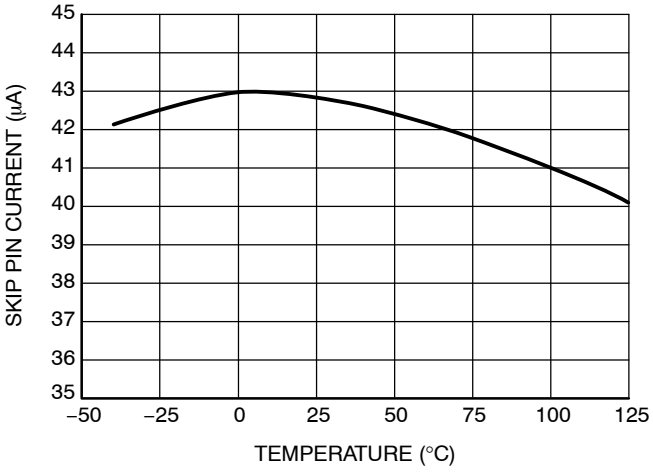


Figure 10. Skip Pin Current vs. Temperature

TYPICAL CHARACTERISTICS

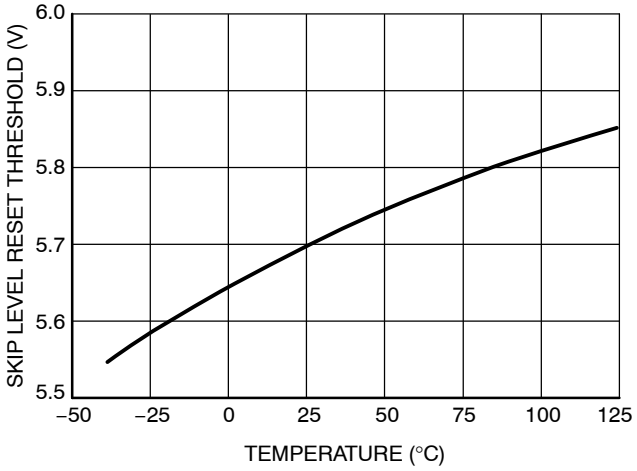


Figure 11. Skip Level Reset Threshold vs. Temperature

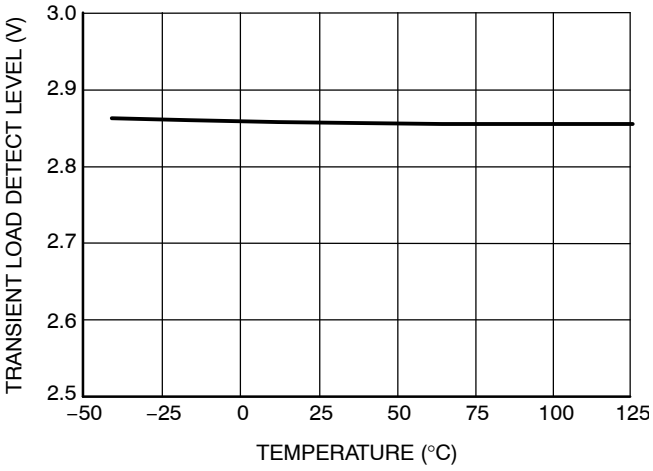


Figure 12. Transient Load Detection Level vs. Temperature

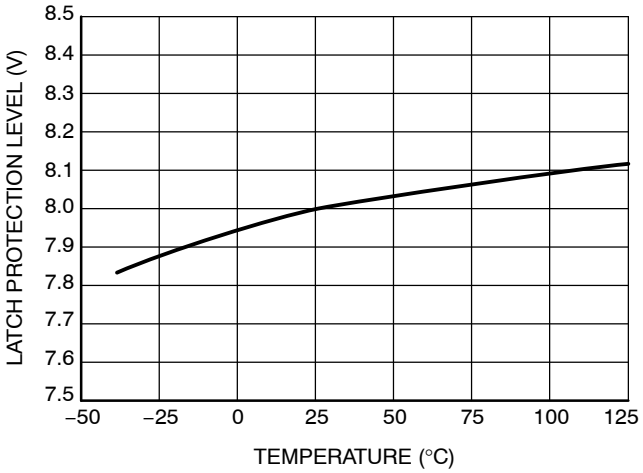


Figure 13. Latch Protection Level vs. Temperature

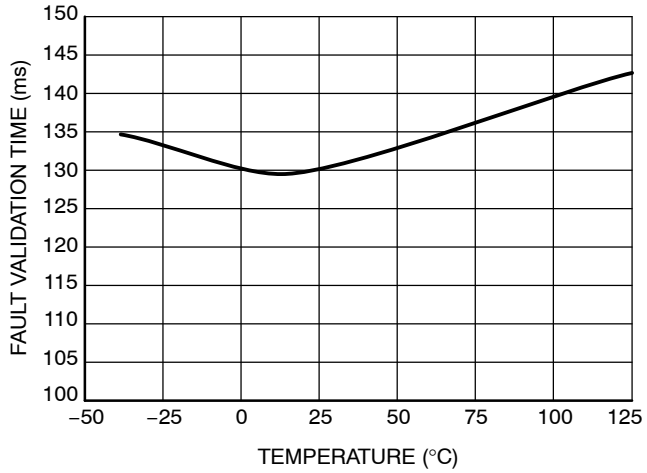


Figure 14. Fault Validation Time vs. Temperature

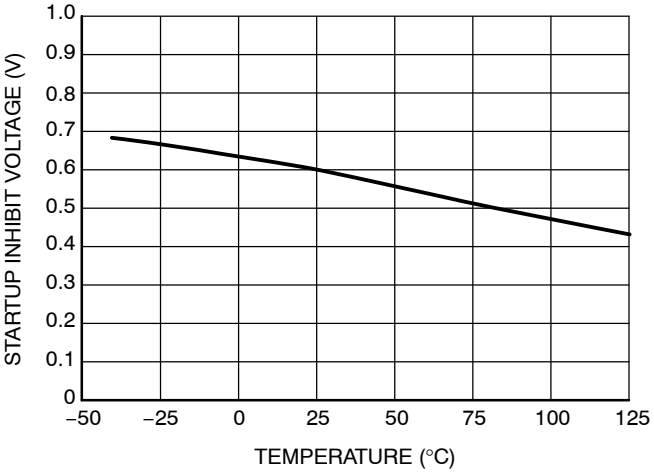


Figure 15. Startup Inhibit Voltage vs. Temperature

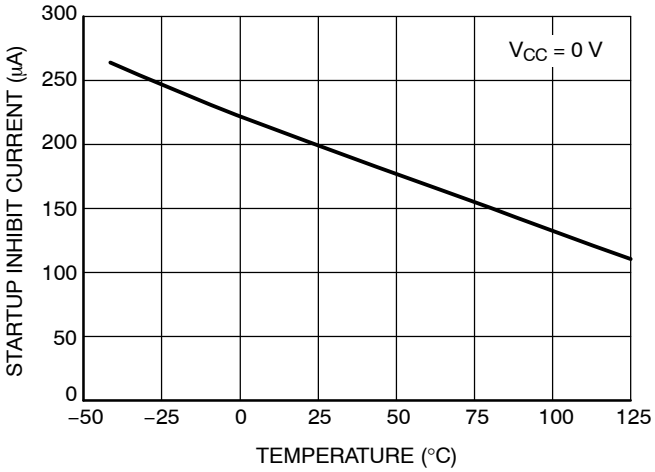


Figure 16. Startup Inhibit Current vs. Temperature

TYPICAL CHARACTERISTICS

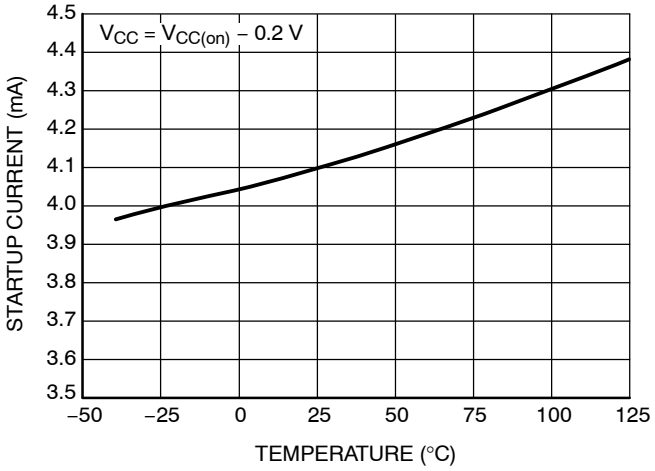


Figure 17. High Voltage Startup Current vs. Temperature

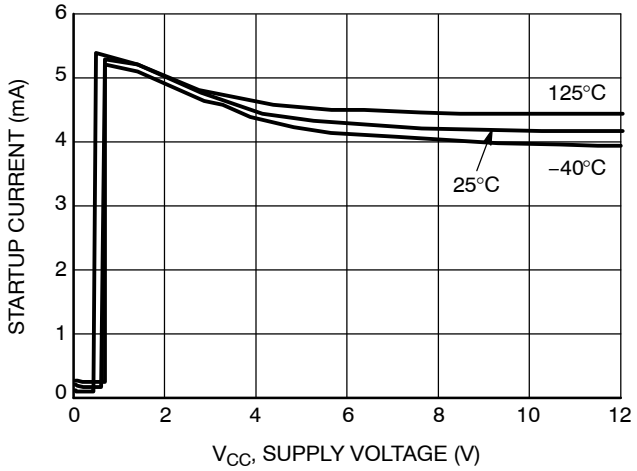


Figure 18. Startup Current vs. V_{CC} Voltage

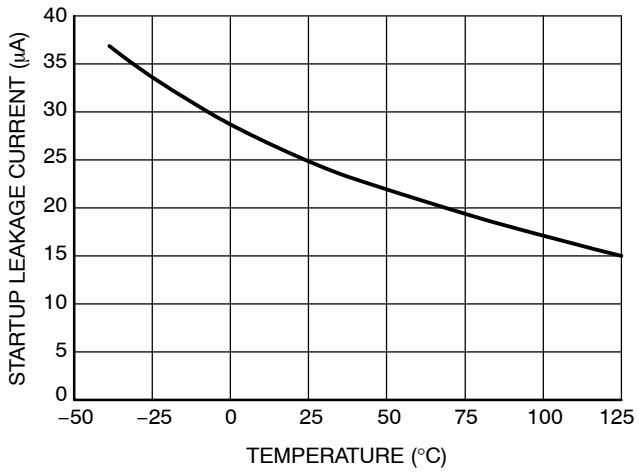


Figure 19. Startup Leakage Current vs. Temperature

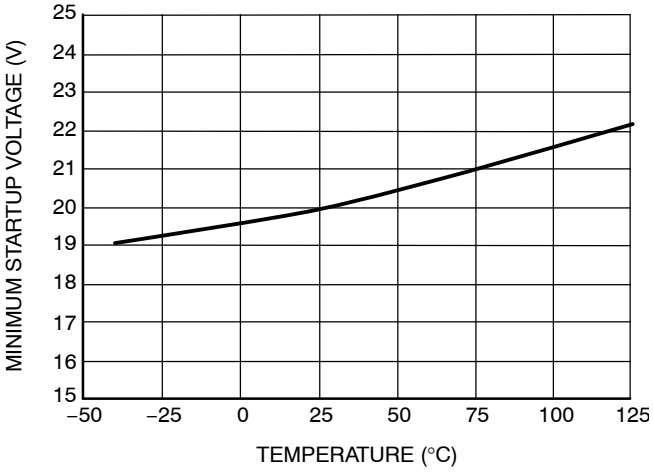


Figure 20. Minimum Startup Voltage vs. Temperature

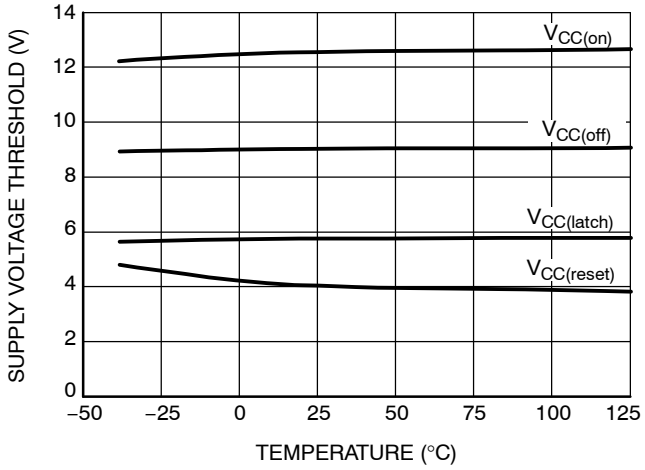


Figure 21. Supply Voltage Thresholds vs. Temperature

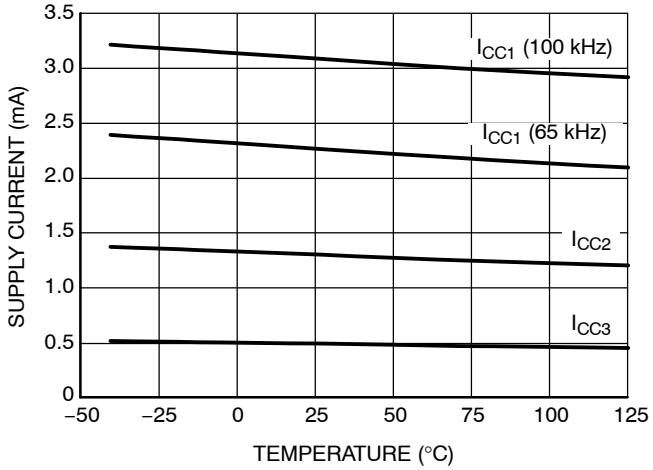


Figure 22. Supply Currents vs. Temperature

OPERATING DESCRIPTION

Introduction

The NCP1271 represents a new generation of the fixed−frequency PWM current−mode flyback controllers from ON Semiconductor. The device features integrated high−voltage startup and excellent standby performance. The proprietary **Soft−Skip Mode** achieves extremely low−standby power consumption while keeping power supply acoustic noise to a minimum. The key features of the NCP1271 are as follows:

- **Timer−Based Fault Detection:** In the event that an abnormally large load is applied to the output for more than 130 ms, the controller will safely shut the application down. This allows accurate overload (OL) or short−circuit (SC) detection which is not dependent on the auxiliary winding.
- **Soft−Skip Mode:** This proprietary feature of the NCP1271 minimizes the standby low−frequency acoustic noise by ramping the peak current envelope whenever skip is activated.
- **Adjustable Skip Threshold:** This feature allows the power level at which the application enters skip to be fully adjusted. Thus, the standby power for various applications can be optimized. The default skip level is 1.2 V (40% of the maximum peak current).
- **500 V High−Voltage Startup Capability:** This AC−DC application friendly feature eliminates the need for an external startup biasing circuit, minimizes the standby power loss, and saves printed circuit board (PCB) space.
- **Dual High−Voltage Startup−Current Levels:** The NCP1271 uniquely provides the ability to reduce the startup current supply when Vcc is low. This prevents damage if Vcc is ever shorted to ground. After Vcc rises above approximately 600 mV, the startup current increases to its full value and rapidly charges the Vcc capacitor.
- **Latched Protection:** The NCP1271 provides a pin, which if pulled high, places the part in a latched off mode. Therefore, overvoltage (OVP) and overtemperature (OTP) protection can be easily implemented. A noise filter is provided on this function to reduce the chances of falsely triggering the latch. The latch is released when Vcc is cycled below 4 V.
- **Non−Latched Protection/ Shutdown Option:** By pulling the feedback pin below the skip threshold level, a non−latching shutdown mode can be easily implemented.
- **4.0 ms Soft−Start:** The soft start feature slowly ramps up the drive duty cycle at startup. This forces the primary current to also ramp up slowly and dramatically reduces the stress on power components during startup.
- **Current−Mode Operation:** The NCP1271 uses current−mode control which provides better transient response than voltage−mode control. Current−mode control also inherently limits the cycle−by−cycle primary current.
- **Compensation Ramp:** A drawback of current−mode regulation is that the circuit may become unstable when the operating duty cycle is too high. The NCP1271 offers an adjustable compensation ramp to solve this instability.
- **80% Maximum Duty Cycle Protection:** This feature limits the maximum on time of the drive to protect the power MOSFET from being continuously on.
- **Frequency Jittering:** Frequency jittering softens the EMI signature by spreading out peak energy within a band +/− 7.5% from the center frequency.
- **Switching Frequency Options:** The NCP1271 is available in either 65 kHz or 100 kHz fixed frequency options. Depending on the application, the designer can pick the right device to help reduce magnetic switching loss or improve the EMI signature before reaching the 150 kHz starting point for more restrictive EMI test limits.

NCP1271 Operating Conditions

There are 5 possible operating conditions for the NCP1271:

1. **Normal Operation** – When V_{CC} is above $V_{CC(off)}$ (9.1 V typical) and the feedback pin voltage (V_{FB}) is within the normal operation range (i.e.,V_{FB} < 3.0 V), the NCP1271 operates as a fixed−frequency current−mode PWM controller.
2. **Standby Operation (or Skip−Cycle Operation)** When the load current drops, the compensation network responds by reducing the primary peak current. When the peak current reaches the skip peak current level, the NCP1271 enters Soft−Skip operation to reduce the power consumption. This Soft−Skip feature offers a modified peak current envelope and hence also reduces the risk of audible noise. In the event of a sudden load increase, the transient load detector (TLD) disables Soft−Skip and applies maximum power to bring the output into regulation as fast as possible.
3. **Fault Operation** – When no feedback signal is received for 130 ms or when V_{CC} drops below $V_{CC(off)}$ (9.1 V typical), the NCP1271 recognizes it as a fault condition. In this fault mode, the Vcc voltage is forced to go through two cycles of slowly discharging and charging. This is known as a "double hiccup." The double hiccup insures that ample time is allowed between restarts to prevent overheating of the power devices. If the fault is

cleared after the double hiccup, then the application restarts. If not, then the process is repeated.

4. **Latched Shutdown** – When the Skip/latch pin (Pin 1) voltage is pulled above 8.0 V for more than 13 μs, the NCP1271 goes into latchoff shutdown. The output is held low and V_{CC} stays in hiccup mode until the latch is reset. The reset can only occur if Vcc is allowed to fall below $V_{CC(reset)}$ (4.0 V typical). This is generally accomplished by unplugging the main input AC source.
5. **Non–Latched Shutdown** – If the FB pin is pulled below the skip level, then the device will enter a non–latched shutdown mode. This mode disables the driver, but the controller automatically recovers when the pulldown on FB is released. Alternatively, Vcc can also be pulled low (below 190 mV) to shutdown the controller. This has the added benefit of placing the part into a low current consumption mode for improved power savings.

Biasing the Controller

During startup, the Vcc bias voltage is supplied by the HV Pin (Pin 8). This pin is capable of supporting up to 500 V, so it can be connected directly to the bulk capacitor. Internally, the pin connects to a current source which rapidly charges V_{CC} to its $V_{CC(on)}$ threshold. After this level is reached, the controller turns on and the transformer auxiliary winding delivers the bias supply voltage to V_{CC}. The startup FET is then turned off, allowing the standby power loss to be minimized. This in–chip startup circuit minimizes the number of external components and Printed Circuit Board (PCB) area. It also provides much lower power dissipation and faster startup times when compared to using startup resistors to V_{CC}. The auxiliary winding needs to be designed to supply a voltage above the $V_{CC(off)}$ level but below the maximum V_{CC} level of 20 V.

For added protection, the NCP1271 also include a dual startup mode. Initially, when V_{CC} is below the inhibit voltage $V_{inhibit}$ (600 mV typical), the startup current source is small (200 uA typical). The current goes higher (4.1 mA typical) when V_{CC} goes above $V_{inhibit}$. This behavior is illustrated in Figure 23. The dual startup feature protects the device by limiting the maximum power dissipation when the V_{CC} pin (Pin 6) is accidentally grounded. This slightly increases the total time to charge V_{CC}, but it is generally not noticeable.

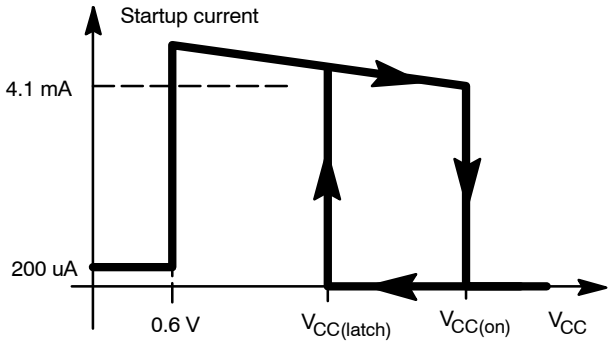


Figure 23. Startup Current at Various V_{CC} Levels

V_{CC} Double Hiccup Mode

Figure 24 illustrates the block diagram of the startup circuit. An undervoltage lockout (UVLO) comparator monitors the V_{CC} supply voltage. If V_{CC} falls below $V_{CC(off)}$, then the controller enters "double hiccup mode."

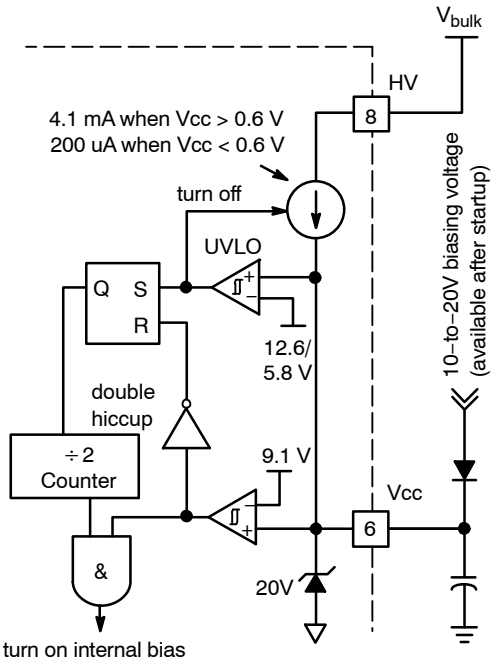


Figure 24. V_{CC} Management

During double hiccup operation, the Vcc level falls to $V_{CC(latch)}$ (5.8 V typical). At this point, the startup FET is turned back on and charges V_{CC} to $V_{CC(on)}$ (12.6 V typical). V_{CC} then slowly collapses back to the $V_{CC(latch)}$ level. This cycle is repeated twice to minimize power dissipation in

external components during a fault event. After the second cycle, the controller tries to restart the application. If the restart is not successful, then the process is repeated. During this mode, V_{CC} never drops below the 4 V latch reset level. Therefore, latched faults will not be cleared unless the application is unplugged from the AC line (i.e., V_{bulk} discharges).

Figure 25 shows a timing diagram of the V_{CC} double hiccup operation. Note that at each restart attempt, a soft start is issued to minimize stress.

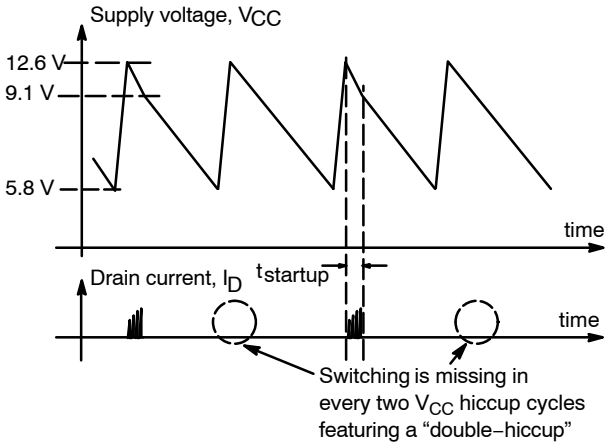


Figure 25. V_{CC} Double Hiccup Operation in a Fault Condition

V_{CC} Capacitor

As stated earlier, the NCP1271 enters a fault condition when the feedback pin is open (i.e. FB is greater than 3 V) for 130 ms or V_{CC} drops below $V_{CC(off)}$ (9.1 V typical). Therefore, to take advantage of these features, the V_{CC} capacitor needs to be sized so that operation can be maintained in the absence of the auxiliary winding for at least 130 ms.

The controller typically consumes 2.3 mA at a 65 kHz frequency with a 1 nF switch gate capacitance. Therefore, to ensure at least 130 ms of operation, equation 1 can be used to calculate that at least an 85 μF capacitor would be necessary.

$$t_{startup} = \frac{C_{VCC}\Delta V}{I_{CC1}} = \frac{85\ \mu F \cdot (12.6\ V - 9.1\ V)}{2.3\ mA} = 130\ ms \quad \text{(eq. 1)}$$

If the 130 ms timer feature will not be used, then the capacitance value needs to at least be large enough for the output to charge up to a point where the auxiliary winding can supply V_{CC}. Figure 26 describes different startup scenarios with different V_{CC} capacitor values. If the V_{CC} cap is too small, the application fails to start because the bias supply voltage cannot be established before V_{CC} is reduced to the $V_{CC(off)}$ level.

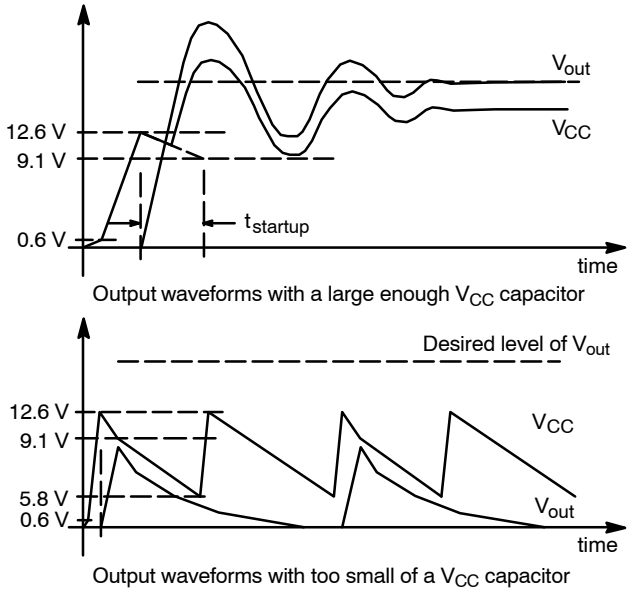


Figure 26. Different Startup Scenarios of the Circuits with Different V_{CC} Capacitors

It is highly recommended that the V_{CC} capacitor be as close as possible to the V_{CC} and ground pins of the product to reduce switching noise. A small bypass capacitor on this pin is also recommended. If the switching noise is large enough, it could potentially cause V_{CC} to go below $V_{CC(off)}$ and force a restart of the controller.

It is also recommended to have a margin between the winding bias voltage and $V_{CC(off)}$ so that all possible transient swings of the auxiliary winding are allowed. In standby mode, the V_{CC} voltage swing can be higher due to the low−frequency skip−cycle operation. The V_{CC} capacitor also affects this swing. Figure 27 illustrates the possible swings.

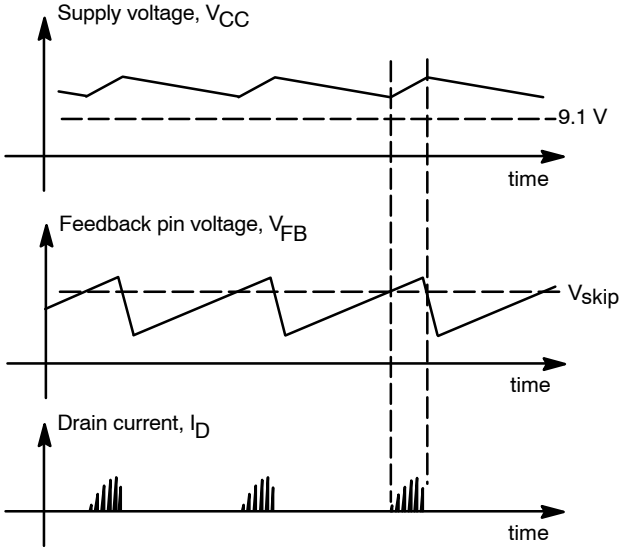


Figure 27. Timing Diagram of Standby Condition

Soft−Start Operation

Figures 28 and 29 show how the soft−start feature is included in the pulse−width modulation (PWM) comparator. When the NCP1271 starts up, a soft−start voltage V_{SS} begins at 0 V. V_{SS} increases gradually from 0 V to 1.0 V in 4.0 ms and stays at 1.0 V afterward. This voltage V_{SS} is compared with the divided−by−3 feedback pin voltage (V_{FB}/3). The lesser of V_{SS} and (V_{FB}/3) becomes the modulation voltage V_{PWM} in the PWM duty cycle generation. Initially, (V_{FB}/3) is above 1.0 V because the output voltage is low. As a result, V_{PWM} is limited by the soft start function and slowly ramps up the duty cycle (and therefore the primary current) for the initial 4.0 ms. This provides a greatly reduced stress on the power devices during startup.

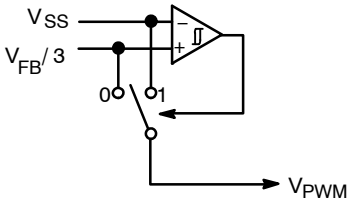


Figure 28. V_{PWM} is the lesser of V_{SS} and (V_{FB}/3)

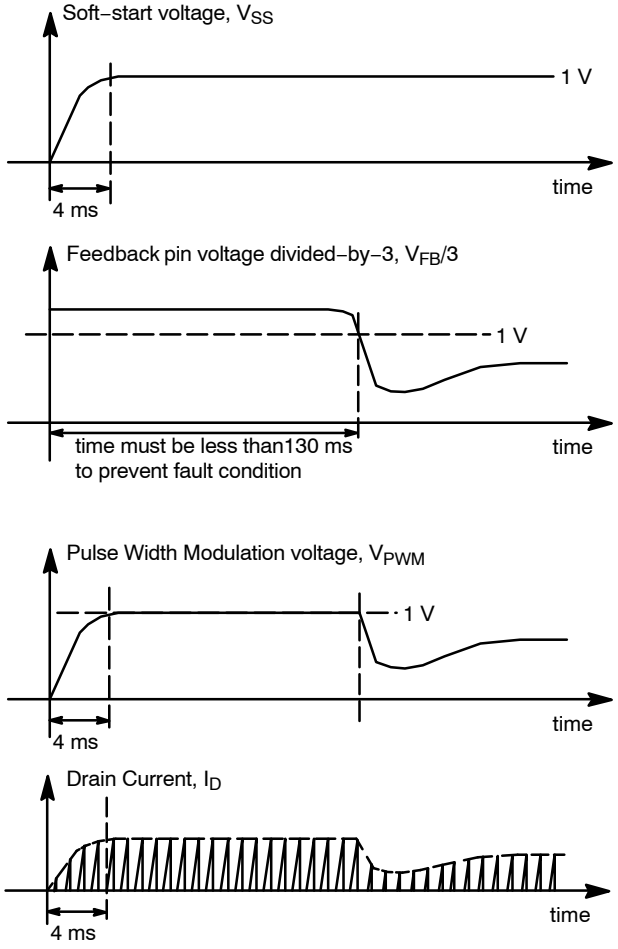


Figure 29. Soft−Start (Time = 0 at V_{CC} = $V_{CC(on)}$)

Current−Mode Pulse−Width Modulation

The NCP1271 uses a current−mode fixed−frequency PWM with internal ramp compensation. A pair of current sense resistors R_{CS} and R_{ramp} sense the flyback drain current I_D. As the drain current ramps up through the inductor and current sense resistor, a corresponding voltage ramp is placed on the CS pin (pin 3). This voltage ranges from very low to as high as the modulation voltage V_{PWM} (maximum of 1.0 V) before turning the drive off. If the internal current ramp is ignored (i.e., $R_{ramp} \approx 0$) then the maximum possible drain current $I_{D(max)}$ is shown in Equation 2. This sets the primary current limit on a cycle by cycle basis.

$$I_{D(max)} = \frac{1\ V}{R_{CS}} \qquad \text{(eq. 2)}$$

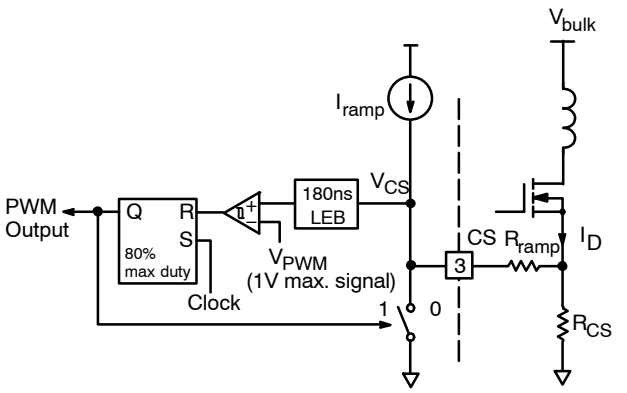


Figure 30. Current−Mode Implementation

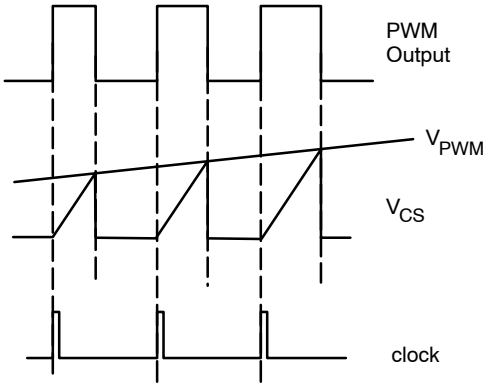


Figure 31. Current−Mode Timing Diagram

The timing diagram of the PWM is in Figure 31. An internal clock turns the Drive Output (Pin 5) high in each switching cycle. The Drive Output goes low when the CS (Pin 3) voltage V_{CS} intersects with the modulation voltage V_{PWM}. This generates the pulse width (or duty cycle). The maximum duty cycle is limited to 80% (typically) in the output RS latch.

Ramp Compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during continuous conduction mode (CCM) with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50 and 75% of the inductor down slope. The NCP1271 generates an internal current ramp that is synchronized with the clock. This current ramp is then routed to the CS pin. Figures 32 and 33 depict how the ramp is generated and utilized. Ramp compensation is simply formed by placing a resistor, R_{ramp}, between the CS pin and the sense resistor.

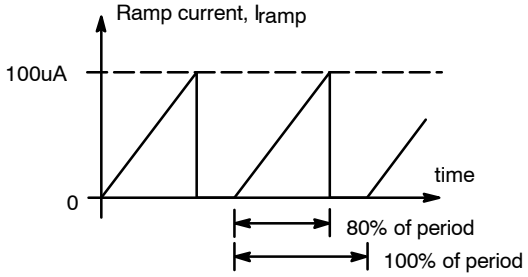


Figure 32. Internal Ramp Current Source

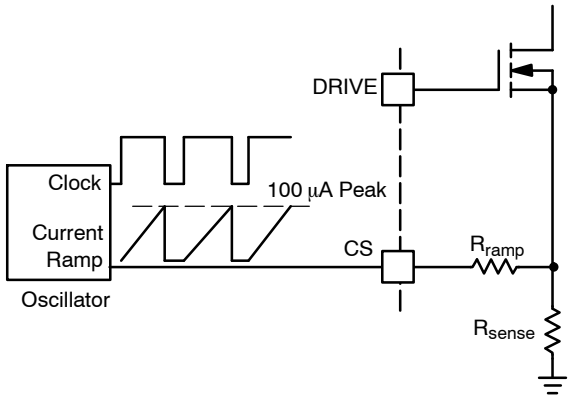


Figure 33. Inserting a Resistor in Series with the Current Sense Information brings Ramp Compensation

For the NCP1271, the current ramp features a swing of 100 μA. Over a 65 kHz frequency with an 80% max duty cycle, that corresponds to an 8.1 μA/μs ramp. For a typical flyback design, let's assume that the primary inductance (Lp) is 350 μH, the SMPS output is 19 V, the Vf of the output diode is 1 V and the Np:Ns ratio is 10:1. The OFF time primary current slope is given by:

$$\frac{(Vout + Vf) \cdot \frac{Np}{Ns}}{Lp} = 571\ V/mH = 571\ mA/\mu s \quad \text{(eq. 3)}$$

When projected over an Rsense of 0.1 Ω (for example), this becomes or 57 mV/μs. If we select 75% of the downslope as the required amount of ramp compensation, then we shall inject 43 mV/μs. Therefore, R_{ramp} is simply equal to:

$$R_{ramp} = \frac{43\ mV/\mu s}{8.1\ \mu A/\mu s} = 5.3\ k\Omega \quad \text{(eq. 4)}$$

It is recommended that the value of R_{ramp} be limited to less then 10 kΩ. Values larger than this will begin to limit the effective duty cycle of the controller and may result in reduced transient response.

Frequency Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP1271 switching frequency ranges from +7.5% to −7.5% of the switching frequency in a linear ramp with a typical period of 6 ms. Figure 34 demonstrates how the oscillation frequency changes.

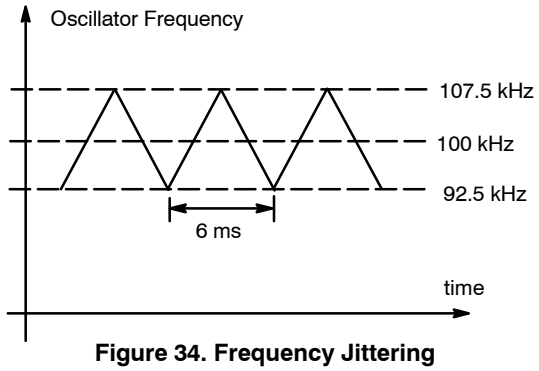


Figure 34. Frequency Jittering (The values are for the 100 kHz frequency option)

Fault Detection

Figure 35 details the timer−based fault detection circuitry. When an overload (or short circuit) event occurs, the output voltage collapses and the optocoupler does not conduct current. This opens the FB pin (pin 2) and V_{FB} is internally pulled higher than 3.0 V. Since (V_{FB}/3) is greater than 1 V, the controller activates an error flag and starts a 130 ms timer. If the output recovers during this time, the timer is reset and the device continues to operate normally. However, if the fault lasts for more than 130 ms, then the driver turns off and the device enters the V_{CC} Double Hiccup mode discussed earlier. At the end of the double hiccup, the controller tries to restart the application.

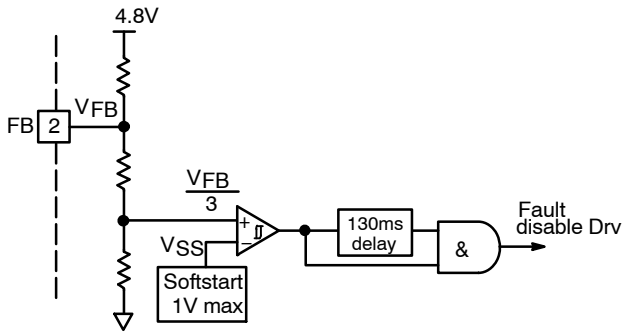


Figure 35. Block Diagram of Timer−Based Fault Detection

Besides the timer−based fault detection, the NCP1271 also enters fault condition when V_{CC} drops below $V_{CC(off)}$ (9.1 V typical). The device will again enter a double hiccup mode and try to restart the application.

Operation in Standby Condition

During standby operation, or when the output has a light load, the duty cycle on the controller can become very small. At this point, a significant portion of the power dissipation is related to the power MOSFET switching on and off. To reduce this power dissipation, the NCP1271 "skips" pulses when the FB level (i.e. duty cycle) drops too low. The level that this occurs at is completely adjustable by setting a resistor on pin 1.

By discontinuing pulses, the output voltage slowly drops and the FB voltage rises. When the FB voltage rises above the V_{skip} level, the drive is turned back on. However, to minimize the risk of acoustic noise, when the drive turns back on the duty cycle of its pulses are also ramped up. This is similar to the soft start function, except the period of the Soft−Skip operation is only 300 μs instead of 4.0 ms for the soft start function. This feature produces a timing diagram shown in Figure 36.

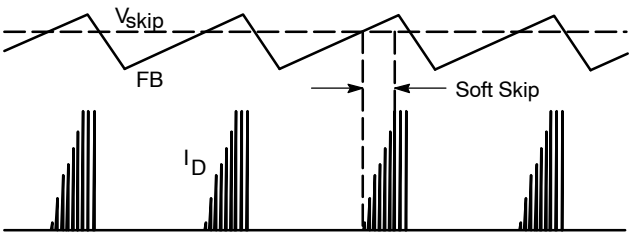


Figure 36. Soft−Skip Operation

Skip Duty Cycle

Skip peak current, $\%Ics_{skip}$, is the percentage of the maximum peak current at which the controller enters skip mode. Ics_{skip} can be any value from 0 to 100% as defined by equation 5. However, the higher that $\%Ics_{skip}$ is, the greater the drain current when skip is entered. This increases the risk of acoustic noise. Conversely, the lower that $\%Ics_{skip}$ is the larger the percentage of energy is expended turning the switch on and off. Therefore it is important to adjust $\%Ics_{skip}$ to the optimal level for a given application.

$$\% \, Ics_{skip} = \frac{V_{skip}}{3 \, V} \cdot 100\% \qquad \text{(eq. 5)}$$

Skip Adjustment

By default, when the Skip/latch Pin (Pin 1) is opened, the skip level is 1.2 V (V_{skip} = 1.2 V). This corresponds to a 40% Ics_{skip} ($\%Ics_{skip}$ = 1.2 V / 3.0 V × 100% = 40%). Therefore, the controller will enter skip mode when the peak current is less than 40% of the maximum peak current. However, this level can be externally adjusted by placing a resistor R_{skip} between skip/latch pin (Pin 1) and Ground (Pin 4). The level will change according to equation 6.

$$V_{skip} = R_{skip} \times I_{skip} \qquad \text{(eq. 6)}$$

To operate in skip cycle mode, V_{skip} must be between 0 V and 3.0 V. Therefore, R_{skip} must be within the levels given in Table 1.

Table 1. Skip Resistor R_{skip} Range for D_{max} = 80% and I_{skip} = 43 μA

$\%Ics_{skip}$	V_{skip} or V_{pin1}	R_{skip}	Comment
0%	0 V	0 Ω	Never skips.
12%	0.375 V	8.7 kΩ	–
25%	0.75 V	17.4 kΩ	–
40%	1.2 V	28 kΩ	–
50%	1.5 V	34.8 kΩ	–
100%	3.0 V	70 kΩ	Always skips.

Recover from Standby

In the event that a large load is encountered during skip cycle operation, the circuit automatically disables the normal Soft−Skip procedure and delivers maximum power to the load (Figure 37). This feature, the Transient Load Detector (TLD), is initiated anytime a skip event is exited and the FB pin is greater than 2.85 V, as would be the case for a sudden increase in output load.

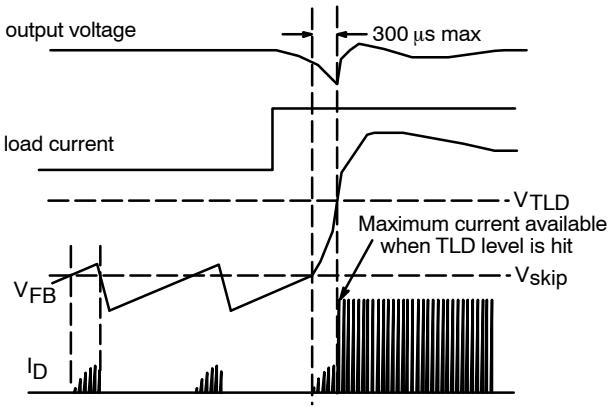


Figure 37. Transient Response from Standby

External Latchoff Shutdown

When the Skip/Latch input (Pin 1) is pulled higher than V_{latch} (8.0 V typical), the drive output is latched off until V_{CC} drops below $V_{CC(reset)}$ (4.0 $V_{typical}$). If Vbulk stays above approximately 30 Vdc, then the HV FET ensure that V_{CC} remains above $V_{CC(latch)}$ (5.8 $V_{typical}$). Therefore, the controller is reset by unplugging the power supply from the wall and allowing V_{bulk} to discharge. Figure 38 illustrates the timing diagram of V_{CC} in the latchoff condition.

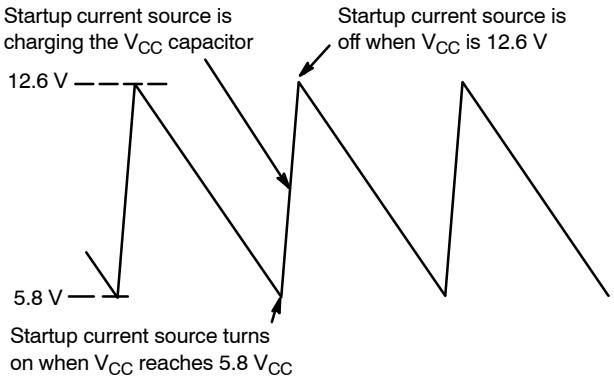


Figure 38. Latchoff V_{CC} Timing Diagram

Figure 39 defines the different voltage regions of the Skip/latch Pin (Pin 1) operation.

1. When the voltage is above V_{latch} (7.1 V min, 8.7 V max), the circuit is in latchoff and all drive pulses are disabled until V_{CC} cycles below 4.0 V (typical).
2. When the voltage is between $V_{skip−reset}$ (5.0 V min, 6.5 V max) and V_{latch}, the pin is considered to be opened. The skip level V_{skip} is restored to the default 1.2 V.
3. When the voltage is between about 3.0 V and $V_{skip−reset}$, the V_{skip} level is above the normal operating range of the feedback pin. Therefore, the output does not switch.
4. When the voltage is between 0 V and 3.0 V, the V_{skip} is within the operating range of the feedback pin. Then the voltage on this pin sets the skip level as explained earlier.

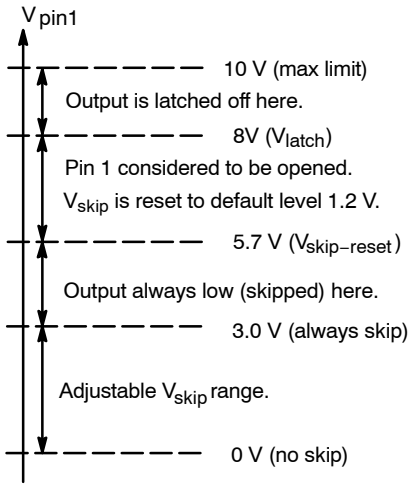


Figure 39. NCP1271 Pin 1 Operating Regions

The external latch feature allows the circuit designers to implement different kinds of latching protection. The NCP1271 applications note (AND8242/D) details several simple circuits to implement overtemperature protection (OTP) and overvoltage protection (OVP).

In order to prevent unexpected latchoff due to noise, it is very important to put a noise decoupling capacitor near Pin 1 to increase the noise immunity. It is also recommended to always have a resistor from pin 1 to GND. This further reduces the risk of premature latchoff. Also note that if the additional latch−off circuitry has leakage, it will modify the skip adjust setup.

External Non−Latched Shutdown

Figure 40 illustrates the Feedback (pin 2) operation. An external non−latched shutdown can be easily implemented by simply pulling FB below the skip level. This is an inherent feature from the standby skip operation. Hence, it allows the designer to implement additional non−latched shutdown protection.

The device can also be shutdown by pulling the V_{CC} pin to GND (<190 mV). In addition to shutting off the output, this method also places the part into a low current consumption state.

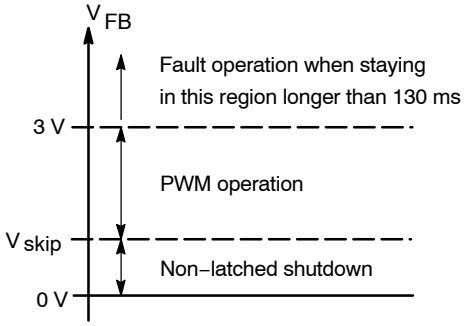


Figure 40. NCP1271 Operation Threshold

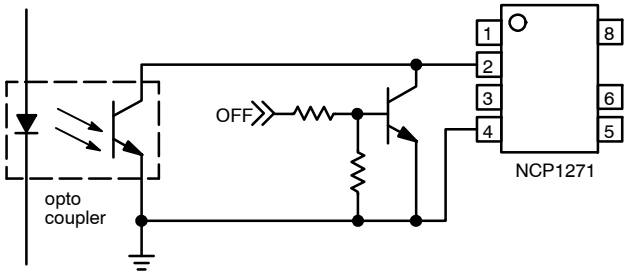


Figure 41. Non−Latchoff Shutdown

Output Drive

The output stage of the device is designed to directly drive a power MOSFET. It is capable of up to +500 mA and −800 mA peak drive currents and has a typical rise and fall time of 30 ns and 20 ns with a 1.0 nF load. This allows the NCP1271 to drive a high−current power MOSFET directly for medium−high power application.

Noise Decoupling Capacitors

There are three pins in the NCP1271 that may need external decoupling capacitors.

1. **Skip/Latch Pin (Pin 1)** – If the voltage on this pin is above 8.0 V, then the circuit enters latchoff. Hence, a decoupling capacitor on this pin is essential for improved noise immunity. Additionally, a resistor should always be placed from this pin to GND to prevent noise from causing the pin 1 level to exceed the latchoff level.
2. **Feedback Pin (Pin 2)** – The FB pin is a high impedance point and is very easily polluted in a noisy environment. This could effect the circuit operation.
3. **V_{CC} Pin (Pin 6)** – The circuit maintains normal operation when V_{CC} is above $V_{CC(off)}$ (9.1 V typical). But, if V_{CC} drops below $V_{CC(off)}$ because of switching noise, then the circuit can incorrectly recognize it as a fault condition. Hence, it is important to locate the V_{CC} capacitor or an additional decoupling capacitor as close as possible to the device.

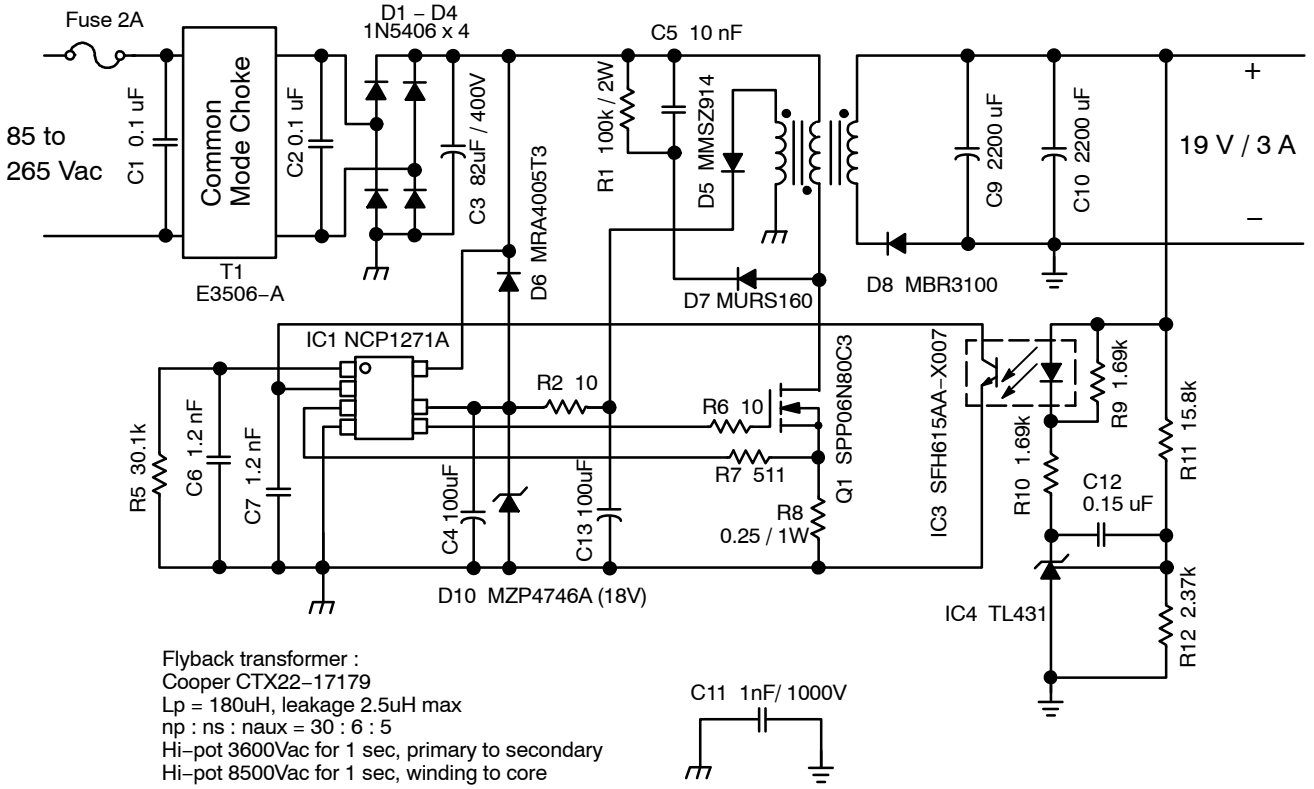


Figure 42. 57 W Example Circuit Using NCP1271

Figure 42 shows a typical application circuit using the NCP1271. The standby power consumption of the circuit is 83 mW with 230 Vac input. The details of the application circuit are described in application note AND8242/D. The efficiency of the circuit at light load up to full load is shown in Figure 43.

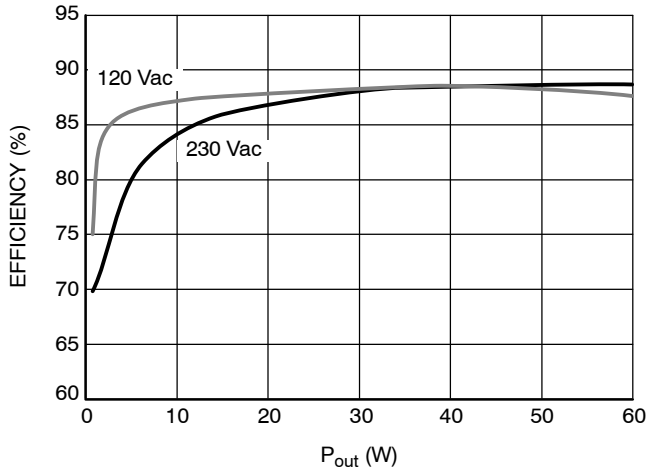


Figure 43. Efficiency of the NCP1271 Demo Board at Nominal Line Voltages

ORDERING INFORMATION

Device	Frequency	Package	Shipping†
NCP1271D65R2G	65 kHz	SOIC−7 (Pb−Free)	2500 / Tape & Reel
NCP1271D100R2G	100 kHz	SOIC−7 (Pb−Free)	2500 / Tape & Reel
NCP1271P65G	65 kHz	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1271P100G	100 kHz	PDIP−7 (Pb−Free)	50 Units / Rail

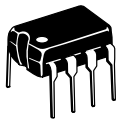
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

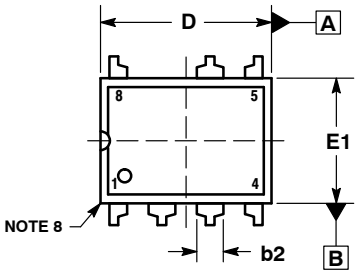
ON Semiconductor®

PDIP−7 (PDIP−8 LESS PIN 7)
CASE 626B
ISSUE D

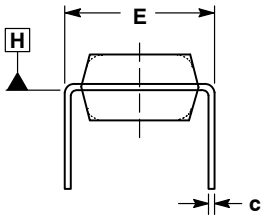
DATE 22 APR 2015



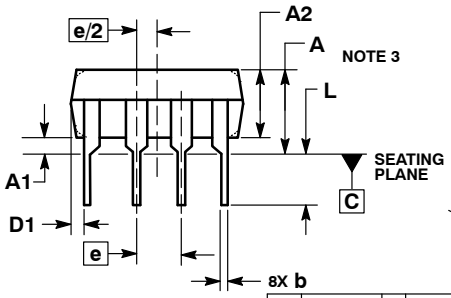
SCALE 1:1



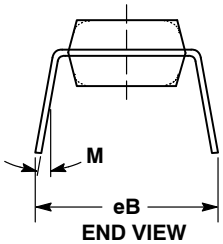
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



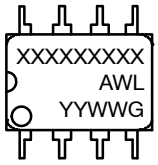
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

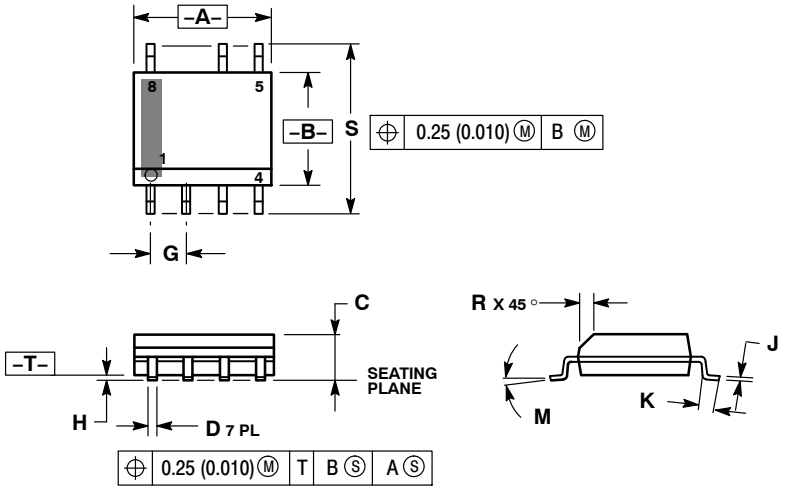
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98AON12198D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP−7 (PDIP−8 LESS PIN 7)	PAGE 1 OF 1

SOIC–7
CASE 751U–01
ISSUE E

DATE 20 OCT 2009

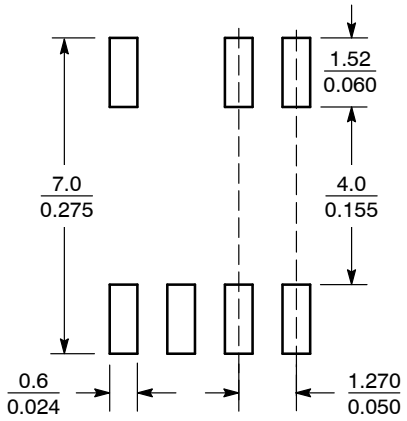
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

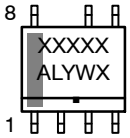
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

SOIC−7
CASE 751U−01
ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales