PWM Current-Mode Controller for Free Running Quasi-Resonant Operation

NCP1207A, NCP1207B

The NCP1207A/B combines a true current mode modulator and a demagnetization detector to ensure full borderline/critical Conduction Mode in any load/line conditions and minimum drain voltage switching (Quasi−Resonant operation). Due to its inherent skip cycle capability, the controller enters burst mode as soon as the power demand falls below a predetermined level. As this happens at low peak current, no audible noise can be heard. For the NCP1207A, an internal 8.0 μs timer prevents the free−run frequency to exceed 125 kHz (therefore below the 150 kHz CISPR−22 EMI starting limit), while the skip adjustment capability lets the user select the frequency at which the burst foldback takes place. For the NCP1207B, the internal timer duration is reduced to 4.5 μs to allow operation at higher frequencies (up to 200 kHz).

The Dynamic Self−Supply (DSS) drastically simplifies the transformer design in avoiding the use of an auxiliary winding to supply the NCP1207A/B. This feature is particularly useful in applications where the output voltage varies during operation (e.g. battery chargers). Due to its high−voltage technology, the IC is directly connected to the high−voltage DC rail. As a result, the short−circuit trip point is not dependent upon any V_{CC} auxiliary level.

The transformer core reset detection is done through an auxiliary winding which, brought via a dedicated pin, also enables fast Overvoltage Protection (OVP). Once an OVP has been detected, the IC permanently latches off.

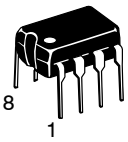
Finally, the continuous feedback signal monitoring implemented with an overcurrent fault protection circuitry (OCP) makes the final design rugged and reliable.

Features

- Free−Running Borderline/Critical Mode Quasi−Resonant Operation
- Current−Mode with Adjustable Skip−Cycle Capability
- No Auxiliary Winding V_{CC} Operation
- Auto−Recovery Overcurrent Protection
- Latching Overvoltage Protection
- External Latch Triggering, e.g. Via Overtemperature Signal
- 500 mA Peak Current Source/Sink Capability
- Undervoltage Lockout for V_{CC} Below 10 V
- Internal 1.0 ms Soft−Start
- Internal 8.0 μs Minimum T_{OFF} for NCP1207A, 4.5 μs Minimum T_{OFF} for NCP1207B
- Adjustable Skip Level
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient Analysis
- These are Pb−Free and Halide−Free Devices

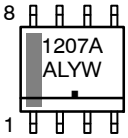
SOIC−8
D SUFFIX
CASE 751

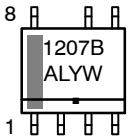
SOIC−7
D SUFFIX
CASE 751U

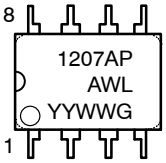


PDIP−8
P SUFFIX
CASE 626

MARKING DIAGRAM

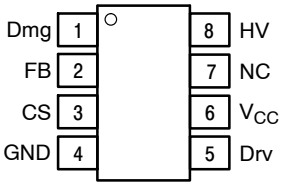






1207A/B/AP	= Device Code
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
▪ or G	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1207ADR2G	SOIC−8 (Pb−Free)	2500/Tape & Reel
NCP1207APG	PDIP−8 (Pb−Free)	50 Units / Tube
NCP1207BDR2G	SOIC−7 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Typical Applications

- AC−DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Consumer Electronics (DVD Players, Set−Top Boxes, TVs, etc.)
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

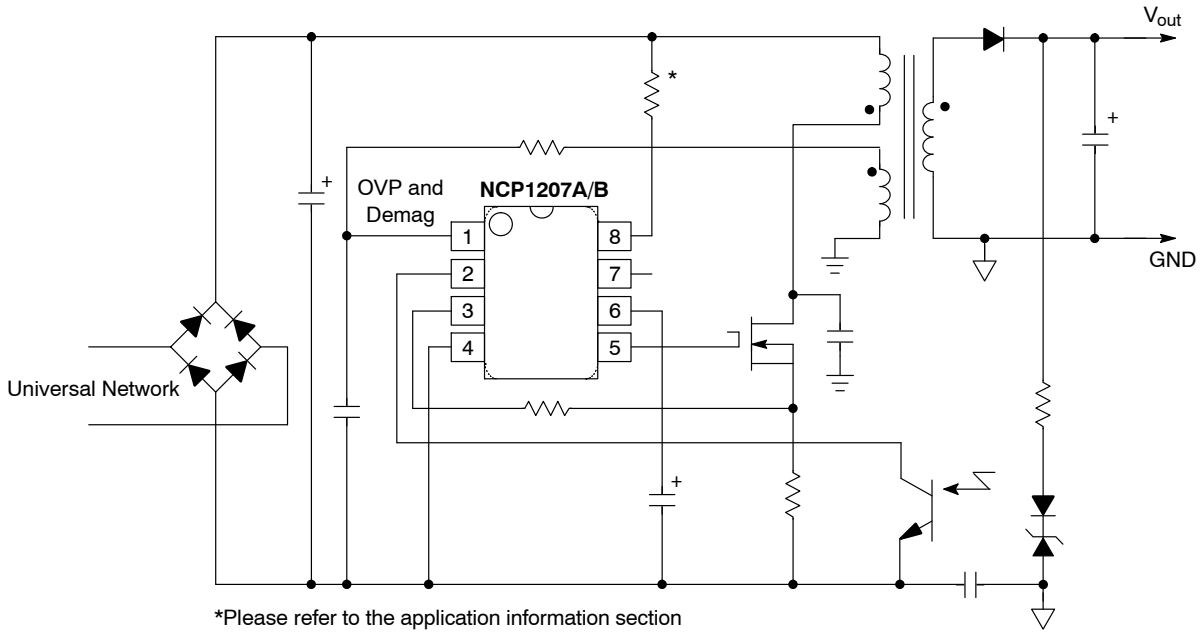


Figure 1. Typical Application

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Function	Description
1	Demag	Core reset detection and OVP	The auxiliary FLYBACK signal ensures discontinuous operation and offers a fixed overvoltage detection level of 7.2 V.
2	FB	Sets the peak current setpoint	By connecting an Optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. By bringing this pin below the internal skip level, device shuts off.
3	CS	Current sense input and skip cycle level selection	This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the level at which the skip operation takes place.
4	GND	The IC ground	–
5	Drv	Driving pulses	The driver's output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 10 μF.
7	NC	–	This unconnected pin ensures adequate creepage distance. (No pin on NCP1207B)
8	HV	High−voltage pin	Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor.

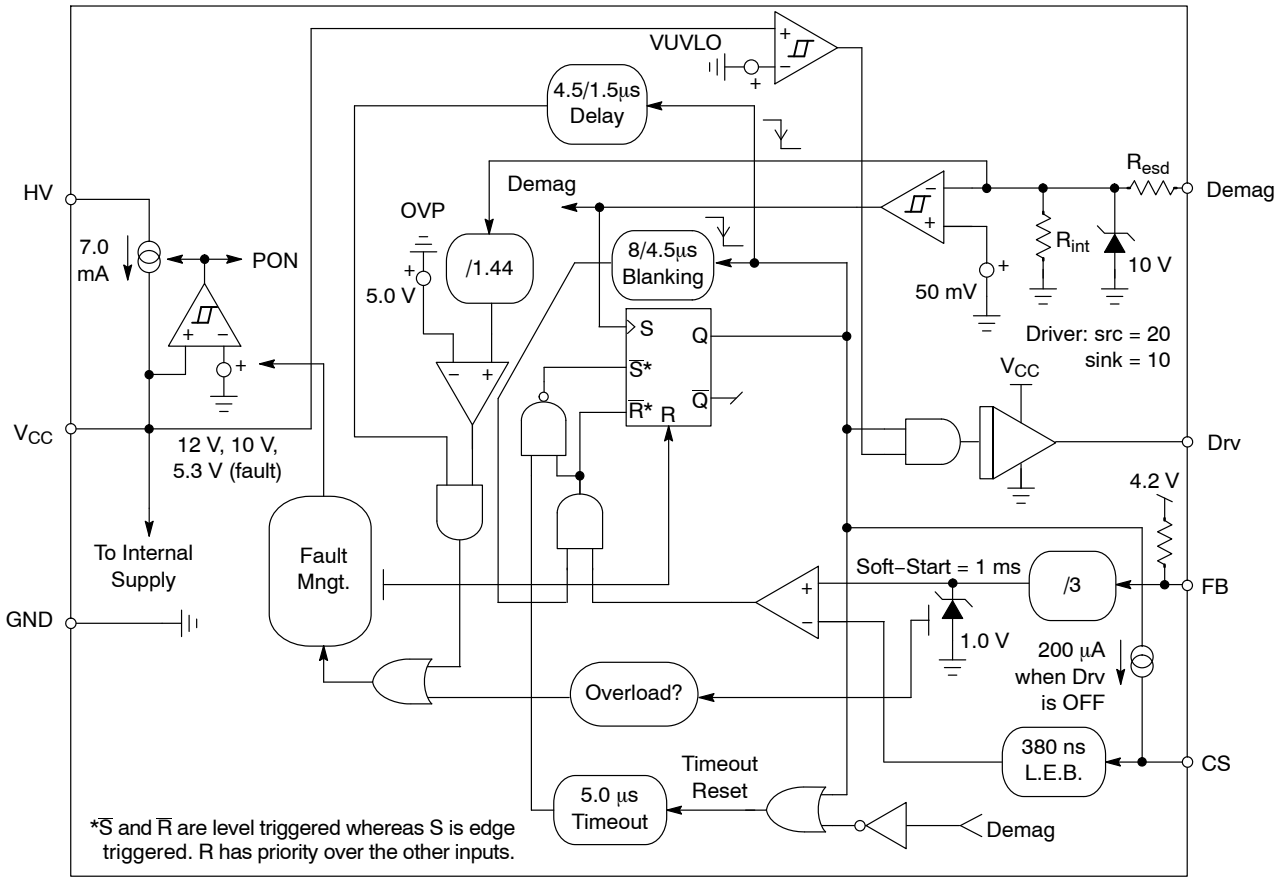


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage, V_{CC} Pin, Continuous Voltage	V_{CC} Static	20	V
Transient Power Supply Voltage, Duration < 10 ms, I_{VCC} < 20 mA	V_{CC} Pulse	25	V
Maximum Voltage on Pin 5 (Drv)	–	20	V
Maximum Voltage on all other pins except Pin 8 (HV), Pin 6 (V_{CC}) and Pin 5 (Drv)	–	−0.3 to 10	V
Maximum Current for all pins except V_{CC} (6), HV (8) and Demag (1) when 10 V ESD diodes are activated	–	5.0	mA
Maximum Current in Pin 1	Idem	+3.0/−2.0	mA
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	57	°C/W
Thermal Resistance, Junction−to−Air, SOIC version	$R_{\theta JA}$	178	°C/W
Thermal Resistance, Junction−to−Air, DIP8 version	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	−40 to +125	°C
Maximum Junction Temperature	TJ_{MAX}	150	°C
Temperature Shutdown	–	155	°C
Hysteresis in Shutdown	–	30	°C
Storage Temperature Range	–	−60 to +150	°C
ESD Capability, HBM Model (All pins except HV)	–	2.0	kV
ESD Capability, Machine Model	–	200	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) decoupled to ground with 10 μF	V_{HVMAX}	500	V
Minimum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) decoupled to ground with 10 μF	V_{HVMIN}	40	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection rated using the following tests:
   Human Body Model (HBM) 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V unless otherwise noted)

Rating	Pin	Symbol	Min	Typ	Max	Unit
DYNAMIC SELF−SUPPLY						
V_{CC} Increasing Level at which the Current Source Turns−off	6	VCC_{OFF}	10.8	12	12.9	V
V_{CC} Decreasing Level at which the Current Source Turns−on	6	VCC_{ON}	9.1	10	10.6	V
V_{CC} Decreasing Level at which the Latchoff Phase Ends	6	VCC_{latch}	–	5.3	–	V
V_{CC} Level at which Output Pulses are Disabled	6	UVLO	–	VCC_{ON} −200mV	–	V
Internal IC Consumption, No Output Load on Pin 5, F_{SW} = 60 kHz	6	ICC1	–	1.0	1.3 (Note 2)	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 60 kHz	6	ICC2	–	1.6	2.0 (Note 2)	mA
Internal IC Consumption in Latchoff Phase	6	ICC3	–	330	–	μA
INTERNAL STARTUP CURRENT SOURCE (T_J > 0°C)						
High−voltage Current Source, V_{CC} = 10 V	8	IC1	4.3	7.0	9.6	mA
High−voltage Current Source, V_{CC} = 0	8	IC2	–	8.0	–	mA
DRIVE OUTPUT						
Output Voltage Rise−time @ CL = 1.0 nF, 10−90% of Output Signal	5	T_r	–	40	–	ns
Output Voltage Fall−time @ CL = 1.0 nF, 10−90% of Output Signal	5	T_f	–	20	–	ns
Source Resistance	5	R_{OH}	12	20	36	Ω
Sink Resistance	5	R_{OL}	5.0	10	19	Ω
CURRENT COMPARATOR (Pin 5 Unloaded)						
Input Bias Current @ 1.0 V Input Level on Pin 3	3	I_{IB}	–	0.02	–	μA
Maximum Internal Current Setpoint	3	I_{Limit}	0.92	1.0	1.12	V
Propagation Delay from Current Detection to Gate OFF State	3	T_{DEL}	–	100	160	ns
Leading Edge Blanking Duration	3	T_{LEB}	–	380	–	ns
Internal Current Offset Injected on the CS Pin during OFF Time	3	Iskip	–	200	–	μA
OVERVOLTAGE SECTION (V_{CC} = 11 V)						
Sampling Delay after ON Time NCP1207A NCP1207B	1	T_{sample}	–	4.5 1.5	–	μs
OVP Internal Reference Level	1	V_{ref}	6.4	7.2	8.0	V
FEEDBACK SECTION (V_{CC} = 11 V, Pin 5 Loaded by 1.0 kΩ)						
Internal Pull−up Resistor	2	Rup	–	20	–	kΩ
Pin 3 to Current Setpoint Division Ratio	–	Iratio	–	3.3	–	–
Internal Soft−start	–	Tss	–	1.0	–	ms
DEMAGNETIZATION DETECTION BLOCK						
Input Threshold Voltage (Vpin 1 Decreasing)	1	V_{th}	35	50	90	mV
Hysteresis (Vpin 1 Decreasing)	1	V_H	–	20	–	mV
Input Clamp Voltage High State (Ipin 1 = 3.0 mA) Low State (Ipin 1 = −2.0 mA)	1 1	VC_H VC_L	8.0 −0.9	10 −0.7	12 −0.5	V V
Demag Propagation Delay	1	T_{dem}	–	210	–	ns
Internal Input Capacitance at Vpin 1 = 1.0 V	1	C_{par}	–	10	–	pF
Minimum T_{OFF} (Internal Blanking Delay after T_{ON}) NCP1207A NCP1207B	1	T_{blank}	– 3.5	8.0 4.5	– 5.5	μs
Timeout After Last Demag Transition	1	T_{out}	–	5.0	–	μs
Pin 1 Internal Impedance	1	R_{int}	–	28	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Max value at T_J = 0°C.

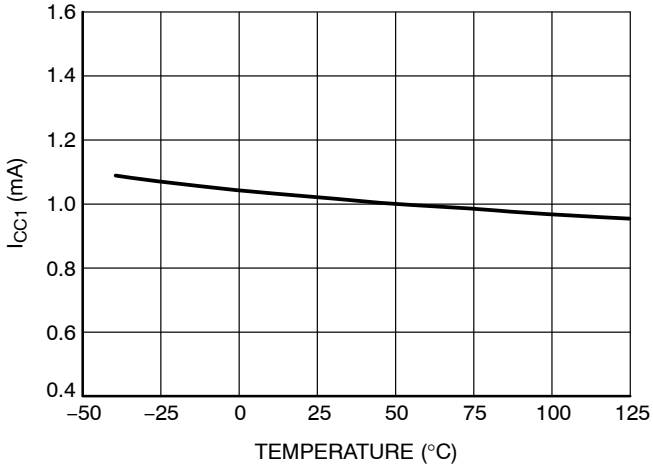


Figure 3. Internal IC Consumption (No Output Load) versus Temperature

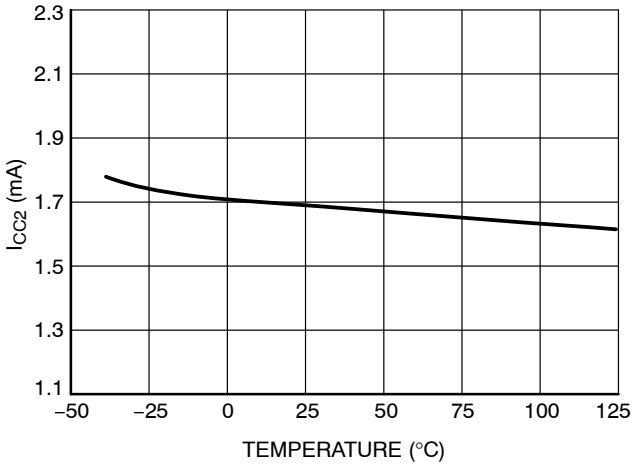


Figure 4. Internal IC Consumption (1.0 nF Output Load) versus Temperature

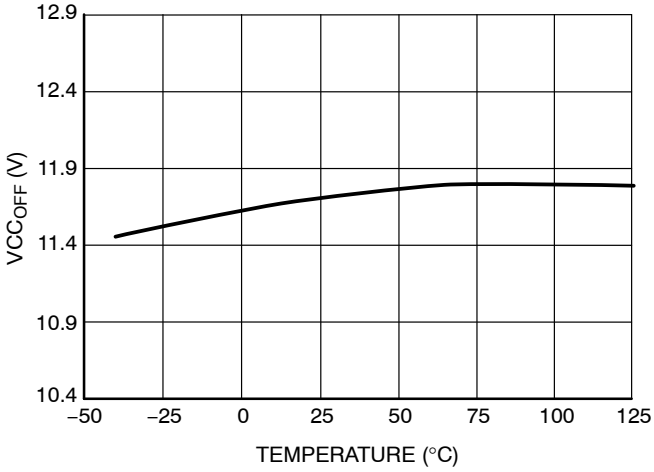


Figure 5. VCC Increasing Level at which the Current Source Turns−Off versus Temperature

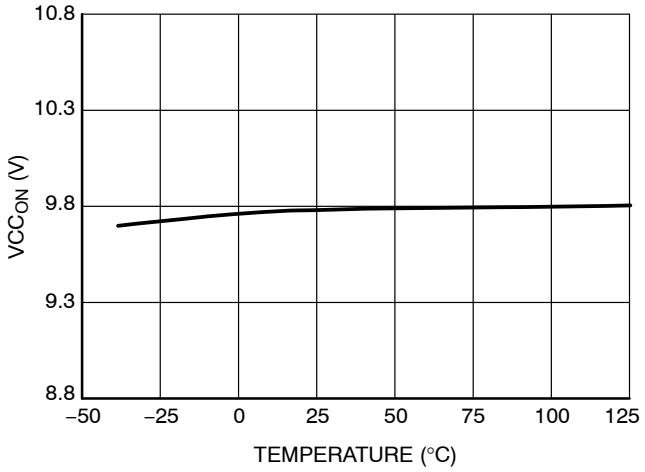


Figure 6. VCC Decreasing Level at which the Current Source Turns−On versus Temperature

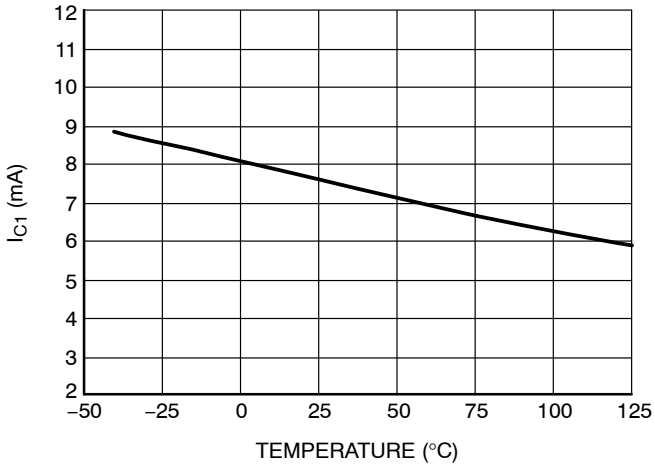


Figure 7. Internal Startup Current Source at V_{CC} = 10 V versus Temperature

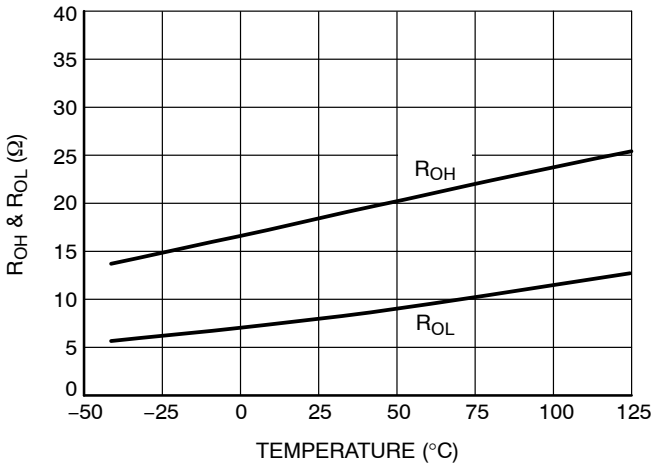


Figure 8. Source and Sink Resistance versus Temperature

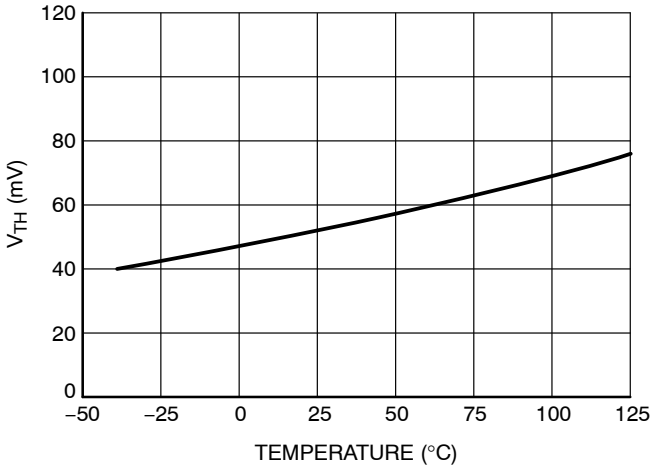


Figure 9. Input Voltage (Vpin1 Decreasing) versus Temperature

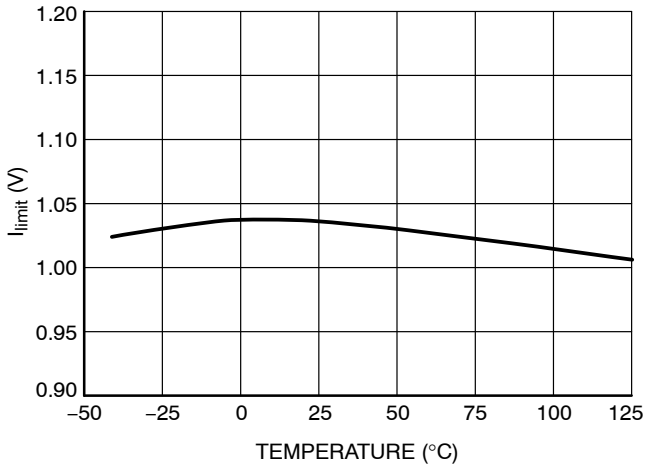


Figure 10. Maximum Internal Current Setpoint versus Temperature

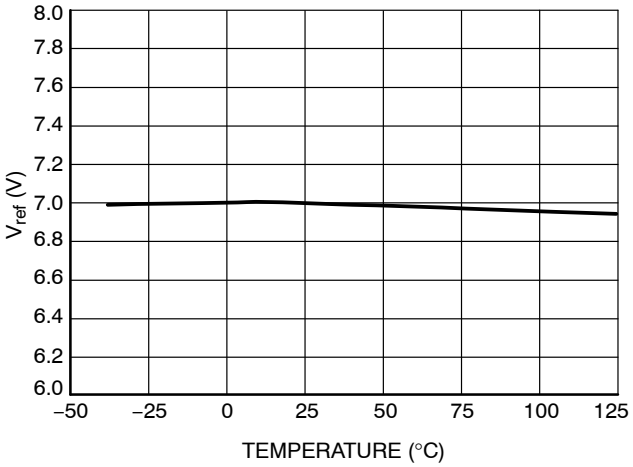


Figure 11. OVP internal Reference Level versus Temperature

APPLICATION INFORMATION

INTRODUCTION

The NCP1207A/B implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint whereas the core reset detection triggers the turn−on event. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC/DC adapters, consumer electronics, auxiliary supplies, etc. Due to its high−performance High−Voltage technology, the NCP1207A/B incorporates all the necessary components / features needed to build a rugged and reliable Switch−Mode Power Supply (SMPS):

- *Transformer core reset detection:* borderline / critical operation is ensured whatever the operating conditions are. As a result, there are virtually no primary switch turn−on losses and no secondary diode recovery losses. The converter also stays a first−order system and accordingly eases the feedback loop design.
- *Quasi−resonant operation:* by delaying the turn−on event, it is possible to re−start the MOSFET in the minimum of the drain−source wave, ensuring reduced EMI / video noise perturbations. In nominal power conditions, the NCP1207A/B operates in Borderline Conduction Mode (BCM) also called Critical Conduction Mode.
- *Dynamic Self−Supply (DSS):* due to its Very High Voltage Integrated Circuit (VHVIC) technology, **onsemi** NCP1207A/B allows for a direct pin connection to the high−voltage DC rail. A dynamic current source charges up a capacitor and thus provides a fully independent V_{CC} level to the NCP1207A/B. As a result, there is no need for an auxiliary winding whose management is always a problem in variable output voltage designs (e.g. battery chargers).
- *Overvoltage Protection (OVP):* by sampling the plateau voltage on the demagnetization winding, the NCP1207A/B goes into latched fault condition whenever an over−voltage condition is detected. The controller stays fully latched in this position until the V_{CC} is cycled down 4.0 V, e.g. when the user un−plugs the power supply from the mains outlet and re−plugs it.
- *External latch trip point:* by externally forcing a level on the OVP greater than the internal setpoint, it is possible to latchoff the IC, e.g. with a signal coming from a temperature sensor.
- *Adjustable skip cycle level:* by offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise−free operation with cheap transformer. This option also offers the ability to fix the maximum switching frequency when entering light load conditions.
- *Overcurrent Protection (OCP):* by continuously monitoring the FB line activity, NCP1207A/B enters burst mode as soon as the power supply undergoes an overload. The device enters a safe low power operation which prevents from any lethal thermal runaway. As soon as the default disappears, the power supply resumes operation. Unlike other controllers, overload detection is performed independently of any auxiliary winding level. In presence of a bad coupling between both power and auxiliary windings, the short circuit detection can be severely affected. The DSS naturally shields you against these troubles.

DYNAMIC SELF−SUPPLY

The DSS principle is based on the charge/discharge of the V_{CC} bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with some simple logical equations:

POWER−ON: IF V_{CC} < VCC_{OFF} THEN Current Source is ON, no output pulses

IF V_{CC} decreasing > VCC_{ON} THEN Current Source is OFF, output is pulsing

IF V_{CC} increasing < VCC_{OFF} THEN Current Source is ON, output is pulsing

Typical values are: VCC_{OFF} = 12 V, VCC_{ON} = 10 V

To better understand the operational principle, Figure 12's sketch offers the necessary light.

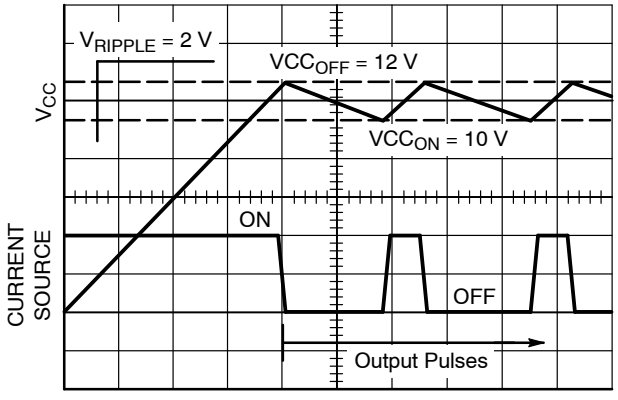


Figure 12. The Charge/Discharge Cycle Over a 10 μF V_{CC} Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge Qg. If we select a MOSFET like the MTP2N60E, Qg equals 22 nC (max). With a maximum switching frequency selected at 75 kHz, the average power necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:

$Fsw \cdot Qg \cdot V_{CC}$ with:

Fsw = maximum switching frequency

Qg = MOSFET's gate charge

$V_{CC} = V_{GS}$ level applied to the gate

To obtain the output current, simply divide this result by V_{CC}: $I_{driver} = F_{SW} \cdot Qg = 1.6$ mA. The total standby power consumption at no−load will therefore heavily rely on the internal IC consumption plus the above driving current (altered by the driver's efficiency). Suppose that the IC is supplied from a 350 VDC line. The current flowing through pin 8 is a direct image of the NCP1207A/B consumption (neglecting the switching losses of the HV current source). If I_{CC2} equals 2.3 mA @ T_J = 60°C, then the power dissipated (lost) by the IC is simply: 350 V x 2.3 mA = 805 mW. For design and reliability reasons, it would be interested to reduce this source of wasted power that increase the die temperature. This can be achieved by using different methods:

1. Use a MOSFET with lower gate charge Qg.
1. Connect pin 8 through a diode (1N4007 typically) to one of the mains input. The average value on pin 8 becomes $\frac{V_{mainsPEAK} \cdot 2}{\pi}$. Our power contribution example drops to: 223 V x 2.3 mA = 512 mW. If a resistor is installed between the mains and the diode, you further force the dissipation to migrate from the package to the resistor. The resistor value should account for low−line startups.

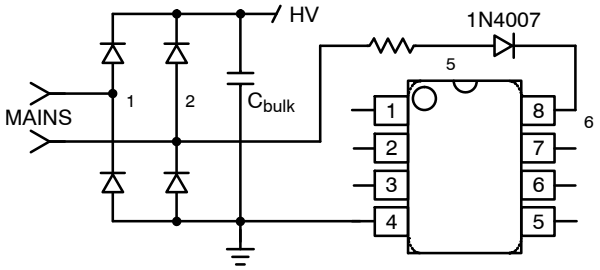


Figure 13. A simple diode naturally reduces the average voltage on Pin 8

When using Figure 13 option, it is important to check the absence of any negative ringing that could occur on pin 8. The resistor in series should help to damp any parasitic LC network that would ring when suddenly applying the power to the IC. Also, since the power disappears during 10 ms (half−wave rectification), CV_{CC} should be calculated to supply the IC during these holes in the supply

2. Permanently force the V_{CC} level above V_{CCH} with an auxiliary winding. It will automatically disconnect the internal startup source and the IC will be fully self−supplied from this winding. Again, the total power drawn from the mains will significantly decrease. Make sure the auxiliary voltage never exceeds the 16 V limit.

SKIPPING CYCLE MODE

The NCP1207A/B automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, Pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 14) and follows the following formula:

$\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \cdot D_{burst}$ with:

Lp = primary inductance

Fsw = switching frequency within the burst

Ip = peak current at which skip cycle occurs

D_{burst} = burst width / burst recurrence

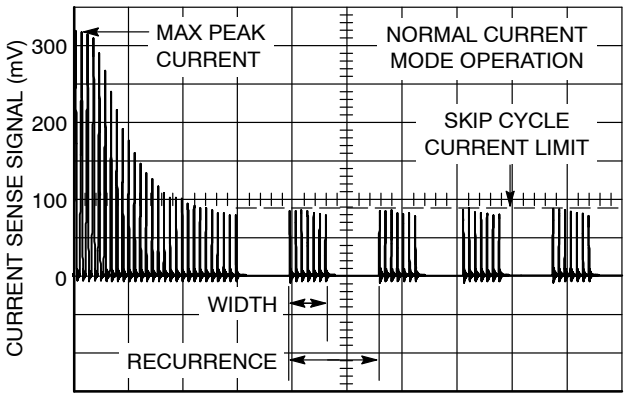


Figure 14. The skip cycle takes place at low peak currents which guaranties noise free operation

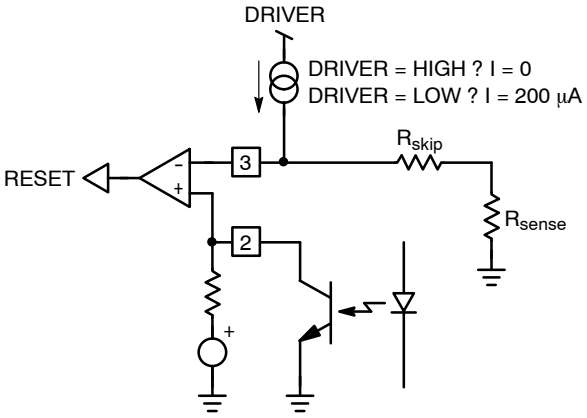


Figure 15. A patented method allows for skip level selection via a series resistor inserted in series with the current

The skip level selection is done through a simple resistor inserted between the current sense input and the sense element. Every time the NCP1207A/B output driver goes low, a 200 μA source forces a current to flow through the sense pin (Figure 15): when the driver is high, the current source is off and the current sense information is normally processed. As soon as the driver goes low, the current source delivers 200 μA and develops a ground referenced voltage across R_{skip}. If this voltage is below the feedback voltage, the current sense comparator stays in the high state and the internal latch can be triggered by the next clock cycle. Now, if because of a low load mode the feedback voltage is below R_{skip} level, then the current sense comparator permanently resets the latch and the next clock cycle (given by the demagnetization detection) is ignored: we are skipping cycles as shown by Figure 16. As soon as the feedback voltage goes up again, there can be two situations: the recurrent period is small and a new demagnetization detection (next wave) signal triggers the NCP1207A/B. To the opposite, in low output power conditions, no more ringing waves are present on the drain and the toggling of the current sense comparator together with the internal 5 μs timeout initiates a new cycle start. In normal operating conditions, e.g. when the drain oscillations are generous, the demagnetization comparator can detect the 50 mV crossing and gives the "green light", alone, to re−active the power switch. However, when skip cycle takes place (e.g. at low output power demands), the re−start event slides along the drain ringing waveforms (actually the valley locations) which decays more or less quickly, depending on the $L_{primary}$−$C_{parasitic}$ network damping factor. The situation can thus quickly occur where the ringing becomes too weak to be detected by the demagnetization comparator: it then permanently stays locked in a given position and can no longer deliver the "green light" to the controller. To help in this situation, the NCP1207A/B implements a 5 μs timeout generator: each time the 50 mV crossing occurs, the timeout is reset. So, as long as the ringing becomes too low, the timeout generator starts to count and after 5 μs, it delivers its "green light". If the skip signal is already present then the controller re−starts; otherwise the logic waits for it to set the drive output high. Figure 16 depicts these two different situations:

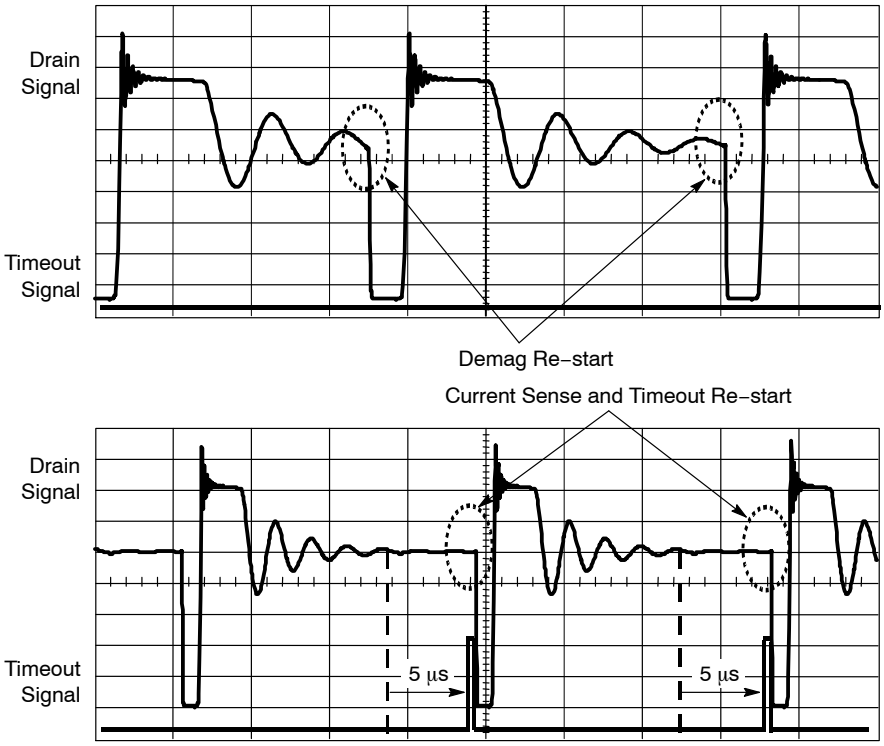


Figure 16. When the primary natural ringing becomes too low, the internal timeout together with the sense comparator initiates a new cycle when FB passes the skip level.

An optocoupler is generally used to transfer the feedback information to the FB pin while providing the necessary isolation. It introduces a limitation in how low the skip level can be adjusted since an optocoupler cannot pull the FB voltage below its Vce(sat), which is usually around 150 mV. Therefore, in order to take into account temperature and process variations, it is not recommended to set up the skip level below 250 mV, which corresponds to a minimum resistor Rskip of 420 Ω. The 150 mV is a much lower level than what will usually be used (it sets the peak current when entering skip mode at 5% of the maximum peak current). If anyway a lower skip threshold is needed, care must be taken to select an optocoupler with a Vce(sat) guaranteed to be below the chosen skip level with enough margin.

DEMAGNETIZATION DETECTION

The core reset detection is done by monitoring the voltage activity on the auxiliary winding. This voltage features a FLYBACK polarity. The typical detection level is fixed at 50 mV as exemplified by Figure 17.

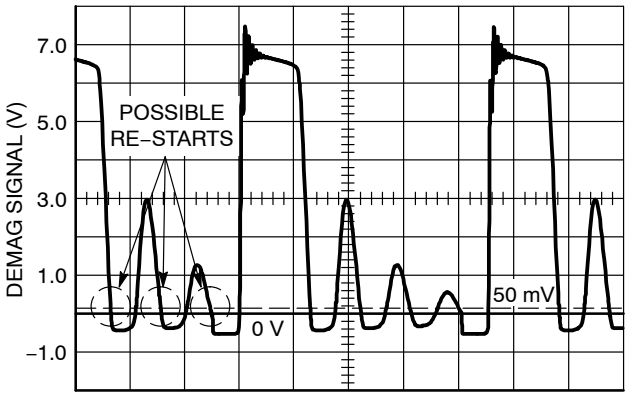


Figure 17. Core reset detection is done through a dedicated auxiliary winding monitoring

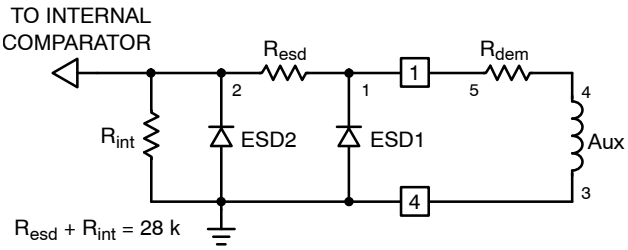


Figure 18. Internal Pad Implementation

An internal timer prevents any re−start within 8.0 μs (NCP1207A) or 4.5 μs (NCP1207B) further to the driver going−low transition. This prevents the switching frequency to exceed (1 / (T_{ON} + 8.0 μs)) or (1 / (T_{ON} + 4.5 μs)) but also avoid false leakage inductance tripping at turn−off. In some cases, the leakage inductance kick is so energetic, that a slight filtering is necessary.

The NCP1207A/B demagnetization detection pad features a specific component arrangement as detailed by Figure 18. In this picture, the zener diodes network protect the IC against any potential ESD discharge that could appear on the pins. The first ESD diode connected to the pad, exhibits a parasitic capacitance. When this parasitic capacitance (10 pF typically) is combined with R_{dem}, a re−start delay is created and the possibility to switch right in the drain−source wave exists. This guarantees QR operation with all the associated benefits (low EMI, no turn−on losses etc.). R_{dem} should be calculated to limit the maximum current flowing through pin 1 to less than +3 mA/−2 mA. If during turn−on, the auxiliary winding delivers 30 V (at the highest line level), then the minimum R_{dem} value is defined by: (30 V + 0.7 V) / 2 mA = 14.6 kΩ. This value will be further increased to introduce a re−start delay and also a slight filtering in case of high leakage energy.

Figure 19 portrays a typical V_{DS} shot at nominal output power.

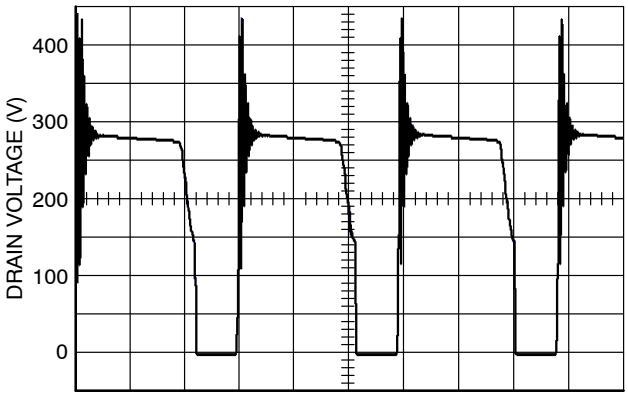


Figure 19. The NCP1207A Operates in Borderline / Critical Operation

OVERVOLTAGE PROTECTION

The overvoltage protection works by sampling the plateau voltage 4.5 μs (NCP1207A) or 1.5 μs (NCP1207B)after the turn−off sequence. This delay guarantees a clean plateau, providing that the leakage inductance ringing has been fully damped. If this would not be the case, the designer should install a small RC damper across the transformer primary inductance connections. Figure 20 shows where the sampling occurs on the auxiliary winding.

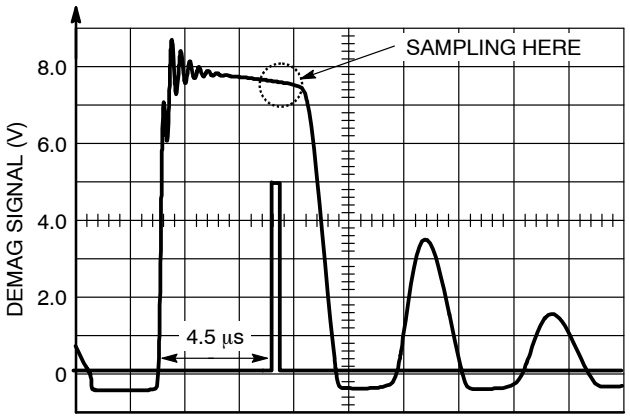


Figure 20. A voltage sample is taken 4.5 μs after the turn−off sequence

When an OVP condition has been detected, the NCP1207A/B enters a latchoff phase and stops all switching operations. The controller stays fully latched in this position and the DSS is still active, keeping the V_{CC} between 5.3 V/12 V as in normal operations. This state lasts until the V_{CC} is cycled down 4 V, e.g. when the user unplugs the power supply from the mains outlet.

By default, the OVP comparator is biased to a 5.0 V reference level and pin1 is routed via a divide by 1.44 network. As a result, when Vpin 1 reaches 7.2 V, the OVP comparator is triggered. The threshold can thus be adjusted by either modifying the power winding to auxiliary winding turn ratios to match this 7.2 V level, or insert a resistor from Pin 1 to ground to cope with your design requirement.

LATCHING OFF THE NCP1207A/B

In certain cases, it can be very convenient to externally shut down permanently the NCP1207A/B via a dedicated signal, e.g. coming from a temperature sensor. The reset occurs when the user unplugs the power supply from the mains outlet. To trigger the latchoff, a CTN (Figure 21) or a simple NPN transistor (Figure 22) can do the work.

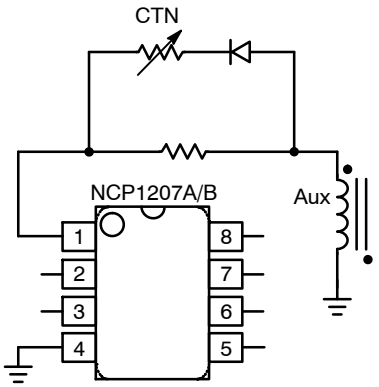


Figure 21. A simple CTN triggers the latchoff as soon as the temperature exceeds a given setpoint

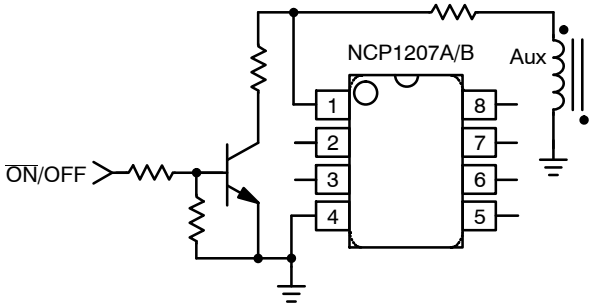


Figure 22. A simple transistor arrangement allows to trigger the latchoff by an external signal

SHUTTING OFF THE NCP1207A/B

Shutdown can easily be implemented through a simple NPN bipolar transistor as depicted by Figure 23. When OFF, Q1 is transparent to the operation. When forward biased, the transistor pulls the FB pin to ground ($V_{CE(sat)} \approx 200$ mV) and permanently disables the IC. A small time constant on the transistor base will avoid false triggering (Figure 23).

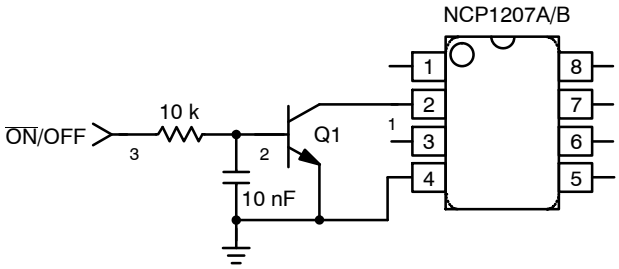


Figure 23. A simple bipolar transistor totally disables the IC

POWER DISSIPATION

The NCP1207A/B is directly supplied from the DC rail through the internal DSS circuitry. The DSS being an auto−adaptive circuit (e.g. the ON/OFF duty−cycle adjusts itself depending on the current demand), the current flowing through the DSS is therefore the direct image of the NCP1207A/B current consumption. The total power dissipation can be evaluated using: $(V_{HVDC} - 11\ V) \cdot I_{CC2}$. If we operate the device on a 250 Vac rail, the maximum rectified voltage can go up to 350 Vdc. As a result, the worse case dissipation occurs at the maximum switching frequency and the highest line. The dissipation is actually given by the internal consumption of the NCP1207A/B when driving the selected MOSFET. The best method to evaluate this total consumption is probably to run the final circuit from a 50 Vdc source applied to pin 8 and measure the average current flowing into this pin. Suppose that we find 2.0 mA, meaning that the DSS duty−cycle will be 2.0/7.0 = 28.6%. From the 350 Vdc rail, the part will dissipate: $350\ V \cdot 2.0\ mA = 700\ mW$ (however this 2.0 mA number

will drop at higher operating junction temperatures). A DIP8 package offers a junction−to−ambient thermal resistance $R_{\theta JA}$ of 100°C/W. The maximum power dissipation can thus be computed knowing the maximum operating ambient temperature (e.g. 70°C) together with the maximum allowable junction temperature (125°C): $P_{max} = \frac{T_{jmax} - T_{Amax}}{R_{\theta JA}} < 550$ mW. As we can see, we do not reach the worse consumption budget imposed by the operating conditions. Several solutions exist to cure this trouble:

- The first one consists in adding some copper area around the NCP1207A DIP8 footprint. By adding a min pad area of 80 mm^2 of 35 μm copper (1 oz.), $R_{\theta JA}$ drops to about 75°C/W. Maximum power then grows up to 730 mW.
- *A resistor R_{drop} needs to be inserted with pin 8 to* a) avoid negative spikes at turn−off (see below)
  b) split the power budget between this resistor and the package. The resistor is calculated by leaving at least 50 V on pin 8 at minimum input voltage (suppose 100 Vdc in our case): $R_{drop} \leq \frac{V_{bulkmin} - 50\ V}{7.0\ mA} < 7.1\ k\Omega$. The power dissipated by the resistor is thus:

$$P_{drop} = V_{dropRMS}^2 / R_{drop} = \frac{\left(I_{DSS} \cdot R_{drop} \cdot \sqrt{DSS_{duty-cycle}}\right)^2}{R_{drop}} = \frac{\left(7.0\ mA \cdot 7.1\ k\Omega \cdot \sqrt{0.286}\right)^2}{7.1\ k\Omega} = 99.5\ mW$$

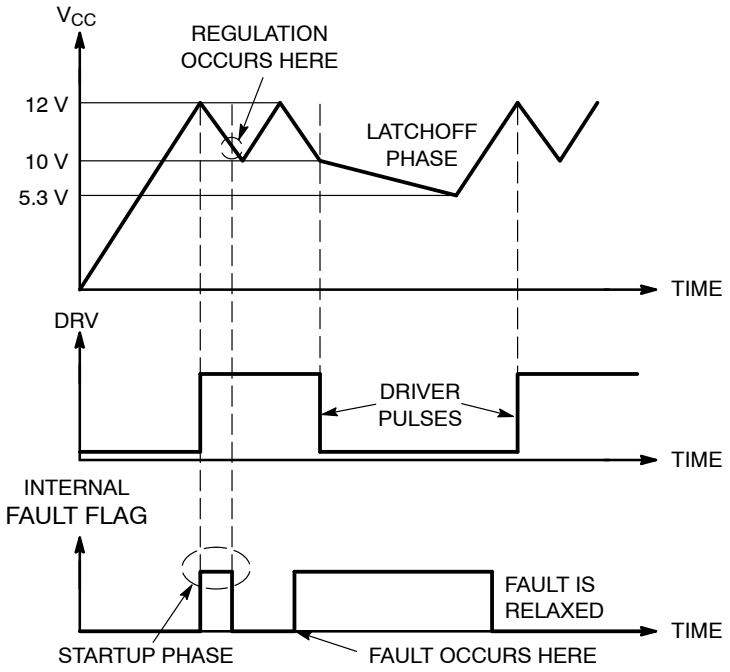
  Please refer to the application note AND8069 available from www.onsemi.com/pub/ncp1200.
- If the power consumption budget is really too high for the DSS alone, connect a diode between the auxiliary winding and the V_{CC} pin which will disable the DSS operation ($V_{CC} > 10$ V).

The SOIC package offers a 178°C/W thermal resistor. Again, adding some copper area around the PCB footprint will help decrease this number: 12 mm × 12 mm to drop $R_{\theta JA}$ down to 100°C/W with 35 μm copper thickness (1 oz) or 6.5 mm ×6.5 mm with 70 μm copper thickness (2 oz). As one can see, we do not recommend using the SO−8 package and the DSS if the part operates at high switching frequencies. In that case, an auxiliary winding is the best solution.

OVERLOAD OPERATION

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the Optocoupler LED. As a result, the FB pin level is pulled up to 4.2 V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken Optocoupler. To account for this situation, NCP1207A hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty−cycle. The system recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time−out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the VCC_{OFF} level (typically 12 V) the device internally watches for an overload current situation. If this condition is still present when the VCC_{ON} level is reached, the controller stops the driving pulses, prevents the self−supply current source to restart and puts all the circuitry in standby, consuming as little as 330 μA typical (I_{CC3} parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 5.3 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 12 V and again delivers output pulses at the VCC_{OFF} crossing point. If the fault condition has been removed before VCC_{ON} approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 24 shows the evolution of the signals in presence of a fault.



If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes.
If the fault still persists when V_{CC} reached VCC_{ON}, then the controller cuts everything off until recovery.

Figure 24.

SOFT−START

The NCP1207A/B features an internal 1 ms soft−start to soften the constraints occurring in the power supply during startup. It is activated during the power on sequence. As soon as V_{CC} reaches VCC_{OFF} , the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 1.0 V). The soft−start is also activated during the overcurrent burst (OCP) sequence. Every restart attempt is followed by a soft−start activation. Generally speaking, the soft−start will be activated when V_{CC} ramps up either from zero (fresh power−on sequence) or 5.3 V, the latchoff voltage occurring during OCP.

CALCULATING THE VCC CAPACITOR

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 12 V to 10 V? The required time depends on the startup sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 12 V to 10 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6.0 ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.8 mA (e.g. with an 11 nC MOSFET), we can calculate the required capacitor using the following formula: $\Delta t = \frac{\Delta V \cdot C}{i}$, with ΔV = 2.0 V. Then for a wanted Δt of 10 ms, C equals 9.0 μF or 22 μF for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 330 μA typical. This happens at V_{CC} = 10 V and it remains stuck until V_{CC} reaches 5.3 V: we are in latchoff phase. Again, using the calculated 22 μF and 330 μA current consumption, this latchoff phase lasts: 313 ms.

HV PIN RECOMMENDED PROTECTION

When the user unplugs a power supply built with a QR controller such as the NCP1207A/B, one instance can occur:

A negative ringing can take place on pin8 due to a resonance between the primary inductance and the bulk capacitor. As any CMOS device, the NCP1207A/B is sensitive to negative voltages that could appear on it's pins and could create an internal latch−up condition.

For this reason, we recommend adding a resistor between the bulk capacitor and the V_{CC} pin.

OPERATION SHOTS

Below are some oscilloscope shots captured at V_{in} = 120 VDC with a transformer featuring a 800 μH primary inductance.

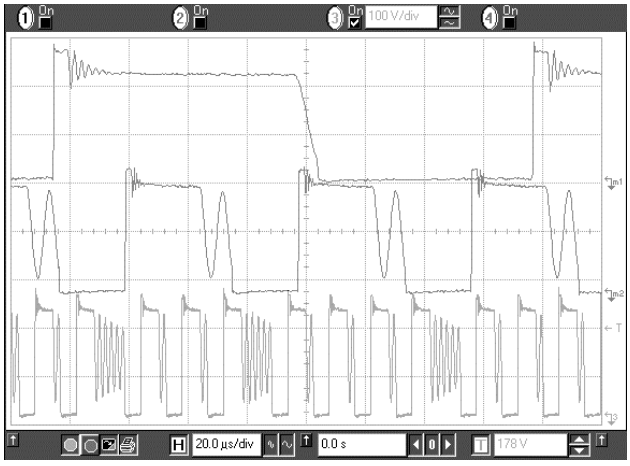


Figure 25.

This plot gathers waveforms captured at three different operating points:

1st upper plot: free run, valley switching operation, P_{out} = 26 W

2nd middle plot: min T_{off} clamps the switching frequency and selects the second valley

3rd lowest plot: the skip slices the second valley pattern and will further expand the burst as P_{out} goes low

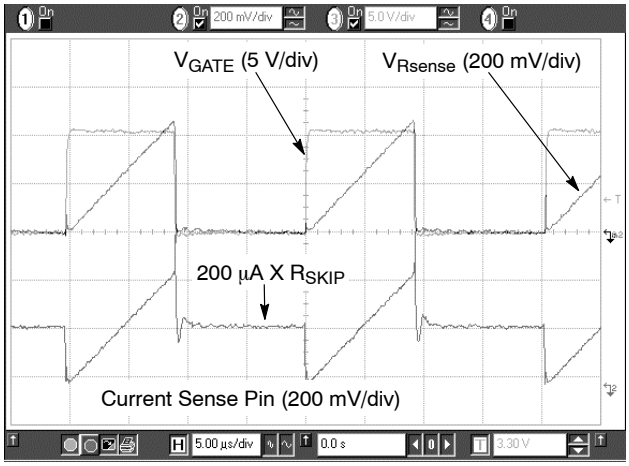


Figure 26.

This picture explains how the 200 μA internal offset current creates the skip cycle level.

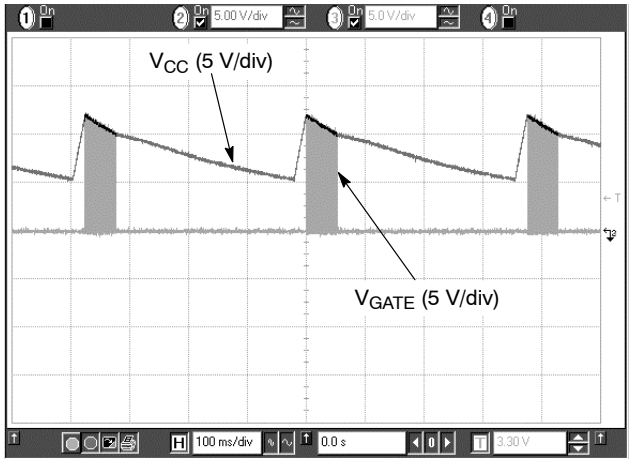


Figure 27.

The short−circuit protection forces the IC to enter burst in presence of a secondary overload.

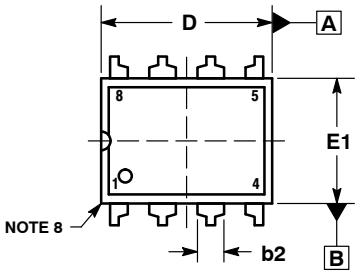
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

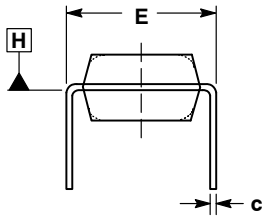
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

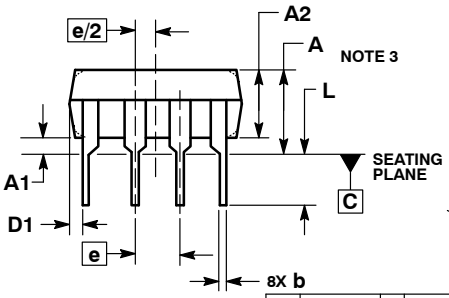
DATE 22 APR 2015



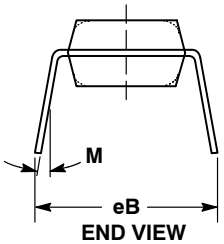
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



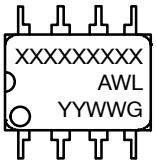
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

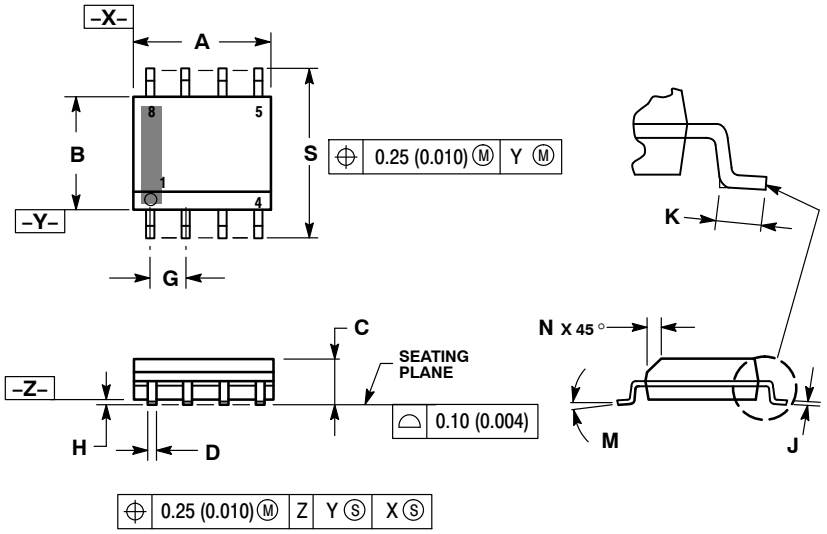
DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

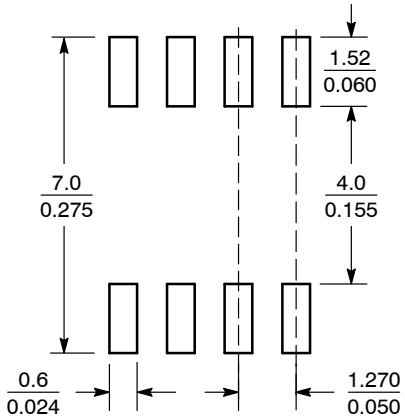
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

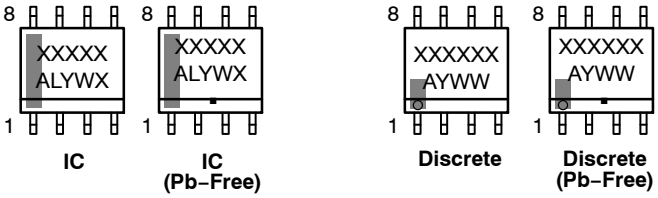
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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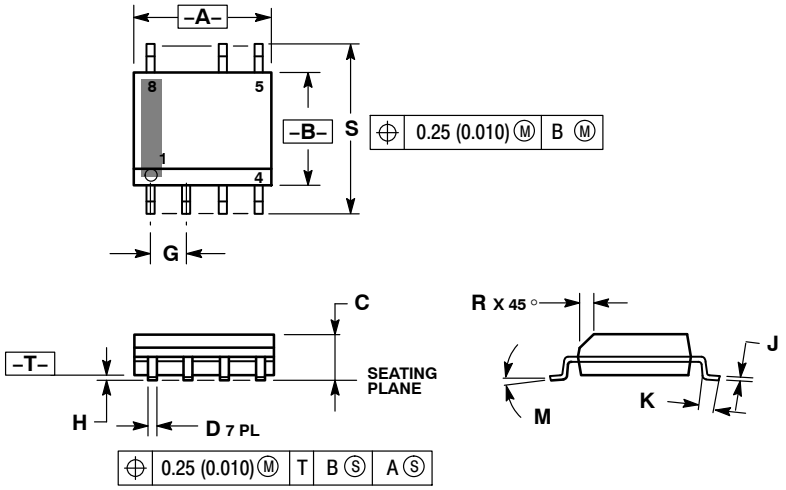
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

SOIC–7
CASE 751U–01
ISSUE E

DATE 20 OCT 2009

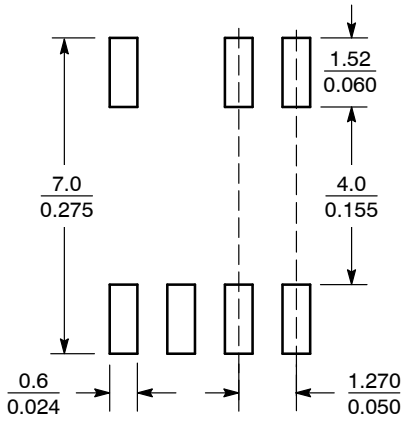
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

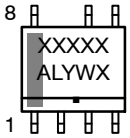
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

SOIC−7
CASE 751U−01
ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales