NCP1015

Self-Supplied Monolithic Switcher for Low Standby-Power Offline SMPS

The NCP1015 integrates a fixed−frequency current−mode controller and a 700 V voltage MOSFET. Housed in a PDIP−7 or SOT−223 package, the NCP1015 offers everything needed to build a rugged and low−cost power supply, including soft−start, frequency jittering, short−circuit protection, skip−cycle, a maximum peak current set−point and a Dynamic Self−Supply (no need for an auxiliary winding).

Unlike other monolithic solutions, the NCP1015 is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (65−100 kHz). When the current set−point falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at typically 0.25 of the maximum peak value, no acoustic noise takes place. As a result, standby power is reduced to the minimum without acoustic noise generation.

Short−circuit detection takes place when the feedback signal fades away e.g. un−true short−circuit or is broken optocoupler cases. Finally soft−start and frequency jittering further ease the designer task to quickly develop low−cost and robust offline power supplies.

For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to consume less than 100 mW at high line.

Features

- Built−in 700 V MOSFET with typical $R_{DS(on)}$ of 11 Ω
- Large Creepage Distance between High−voltage Pins
- Current−mode Fixed Frequency Operation: 65 kHz − 100 kHz
- Skip−cycle Operation at Low Peak Currents Only: No Acoustic Noise!
- Dynamic Self−Supply, No Need for an Auxiliary Winding
- Internal 1 ms Soft−start
- Auto−recovery Internal Output Short−circuit Protection
- Frequency Jittering for Better EMI Signature
- Below 100 mW Standby Power if Auxiliary Winding is Used
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient and AC Analysis
- This is a Pb−Free Device

Typical Applications

- Low Power ac−dc Adapters for Chargers
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

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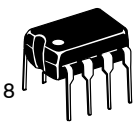
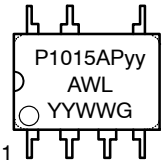
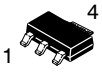
MARKING DIAGRAMS

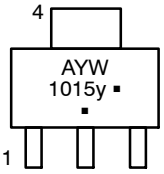


PDIP−7
CASE 626A
AP SUFFIX





SOT−223
CASE 318E
ST SUFFIX

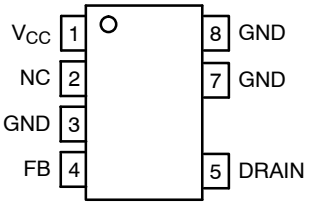


yy = 06 (65 kHz), 10 (100 kHz)
y = A (65 kHz), B (100 kHz)
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb−Free Package

(*Note: Microdot may be in either location)

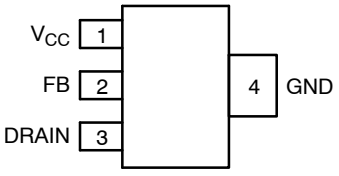
PIN CONNECTIONS

PDIP−7



(Top View)

SOT−223



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

Indicative Maximum Output Power from NCP1015

$R_{DS(on)}$ − I_p	230 Vac	100 − 250 Vac
11 Ω − 450 mA DSS	14 W	6.0 W
11 Ω − 450 mA Auxiliary Winding	19 W	8.0 W

1. Informative values only, with: T_{amb} = 50°C, circuit mounted on minimum copper area as recommended.

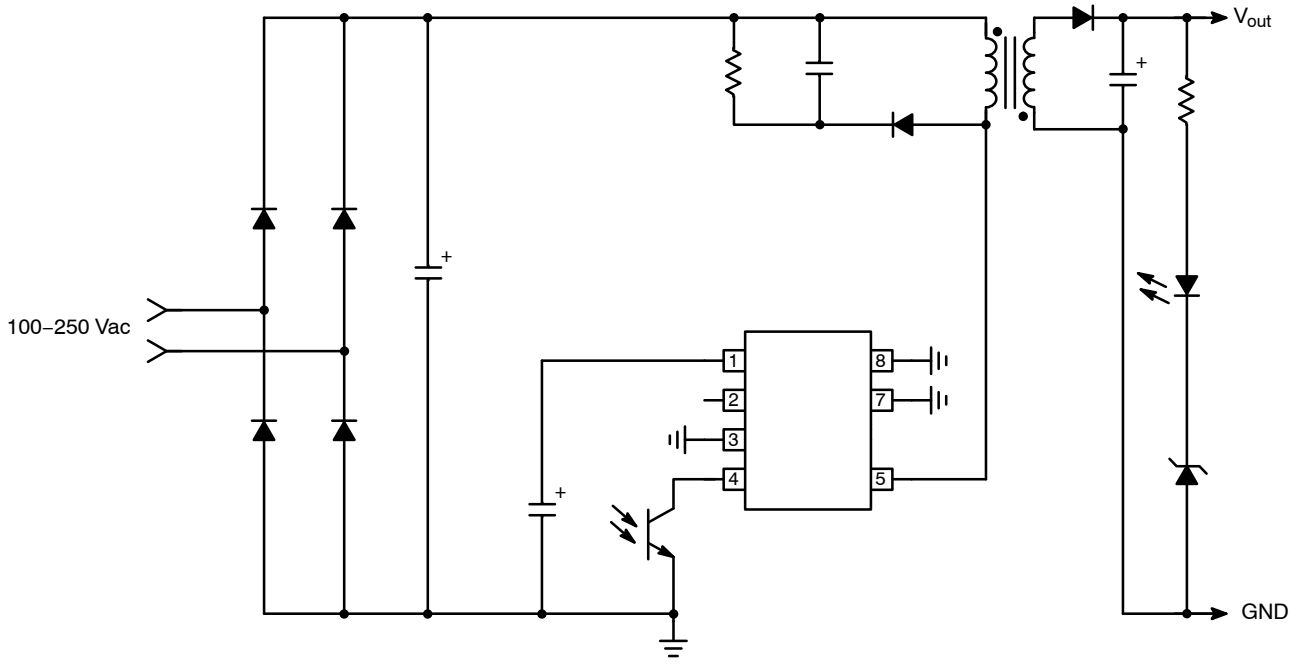


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin No.		Pin Name	Function	Description
SOT−223	PDIP−7			
1	1	V_{CC}	Powers the Internal Circuitry	This pin is connected to an external capacitor of typically 10 μF. The natural ripple superimposed on the V_{CC} participates to the frequency jittering. For improved standby performance, an auxiliary V_{CC} can be connected to Pin 1. The V_{CC} also includes an active shunt which serves as an opto fail−safe protection.
−	2	NC	−	−
−	3	GND	The IC Ground	−
2	4	FB	Feedback Signal Input	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	5	DRAIN	Drain Connection	The internal drain MOSFET connection.
−	−	−	−	−
−	7	GND	The IC Ground	−
4	8	GND	The IC Ground	−

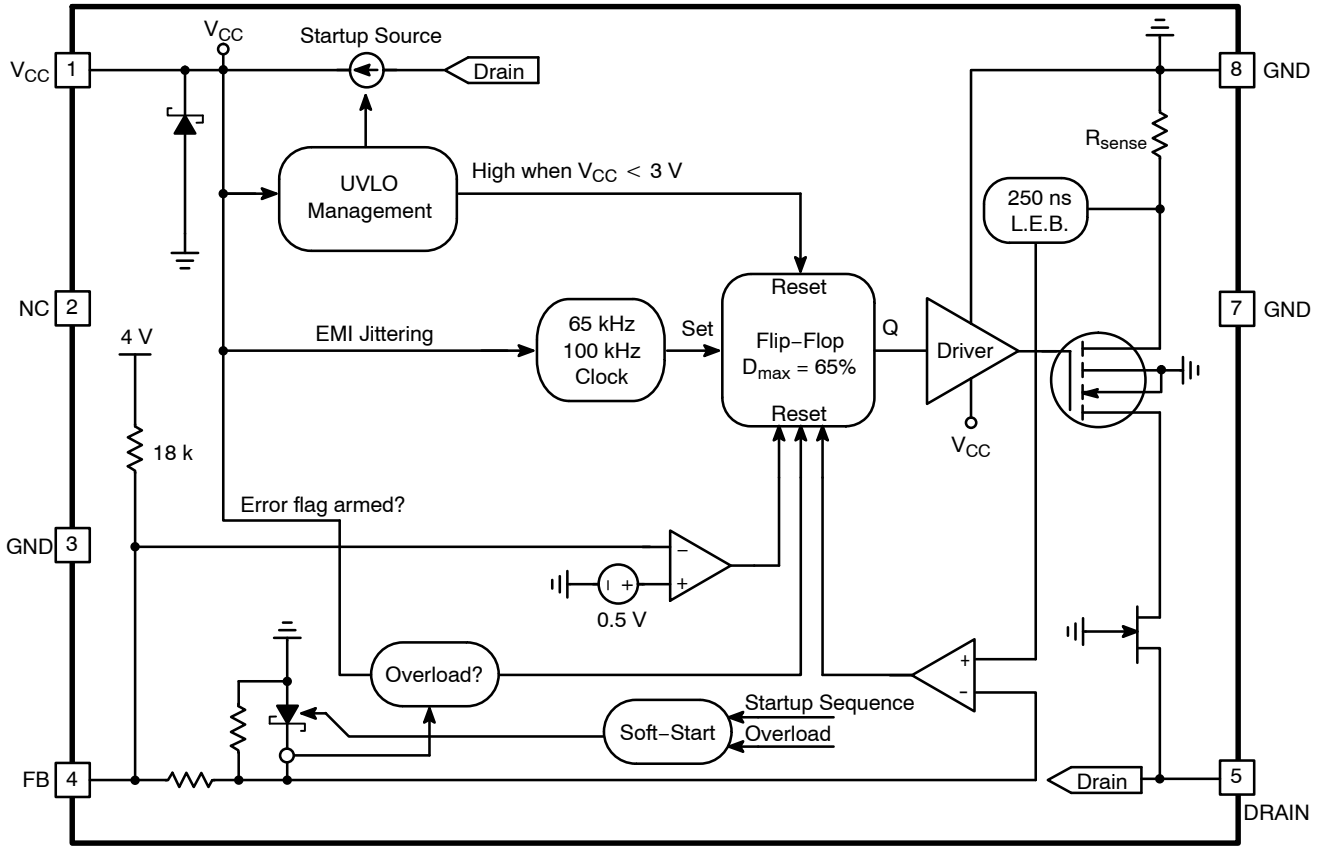


Figure 2. Simplified Internal Circuit Architecture

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	Power Supply voltage on all pins, except pin 5 (drain)	−0.3 to 10	V
Vds	Drain voltage	−0.3 to 700	V
Ids_{pk}	Drain peak current during transformer saturation	1	A
I_V_{CC}	Maximum current into pin 1	15	mA
	Thermal Characteristics		°C/W
	P Suffix, Case 626A		
$R_{\theta JL}$	Junction−to−Lead	9.0	
$R_{\theta JA}$	Junction−to−Air, 2.0 oz (70 μm) Printed Circuit Copper Clad		
	0.36 Sq. Inch (2.32 Sq. Cm)	77	
	1.0 Sq. Inch (6.45 Sq. Cm)	60	
	ST Suffix, Plastic Package Case 318E		
$R_{\theta JL}$	Junction−to−Lead	14	
$R_{\theta JA}$	Junction−to−Air, 2.0 oz (70 μm) Printed Circuit Copper Clad		
	0.36 Sq. Inch (2.32 Sq. Cm)	74	
	1.0 Sq. Inch (6.45 Sq. Cm)	55	
TJ_{MAX}	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model (HBM) (All pins except HV)	2	kV
	ESD Capability, Machine Model (MM)	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (For typical values T_J=25°C, for min/max values T_J=−40°Cto125°C, V_{CC}=8V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
$V_{CC(off)}$	V_{CC} increasing level at which the current source turns−off	1	7.9	8.5	9.1	V
$V_{CC(on)}$	V_{CC} decreasing level at which the current source turns−on	1	6.9	7.5	8.1	V
$V_{CCLATCH}$	Decreasing level at which the Latch−off phase Ends	1	4.4	4.7	5.1	V
ΔV_{CC}	Hysteresis between $V_{CC(off)}$	1	–	1.0	–	
ICC1	Internal IC consumption, MOSFET switching at 65 kHz	1	–	0.92	1.1	mA
ICC1	Internal IC consumption, MOSFET switching at 100 kHz	1	–	0.95	1.15	mA
V_{clamp}	Active zener voltage positive offset to $V_{CC(off)}$	1	140	200	300	mV
POWER SWITCH CIRCUIT						
$R_{DS(on)}$	Power Switch Circuit on−state resistance (Id = 50 mA) T_J = 25°C T_J = 125°C	 5 5	 – –	 11 –	 19 24	Ω
V_{dsb}	Power Switch Circuit & Startup breakdown voltage ($I_{DS(off)}$ = 100 μA, T_J = 25°C)	5	700	–	–	V
$I_{DS(off)}$	Power Switch & Startup breakdown voltage off−state leakage current T_J = −40°C (Vds = 650 V) T_J = 25°C (Vds = 700 V) T_J = 125°C (Vds = 700 V)	 5 5 5	 – – –	 70 50 30	 120 – –	μA
 t_{on} t_{off}	Switching characteristics (R_L = 50 Ω, Vds set for Ids = 0.7 x Ids_{lim}) Turn−on time (90% − 10%) Turn−off time (10% − 90%)	 5 5	 – –	 20 10	 – –	ns
INTERNAL START−UP CURRENT SOURCE						
IC1	High−voltage current source, V_{CC} = 8 V 0°C < T_J < 125°C −40°C < T_J < 125°C	1	5.0 5.0	8.0 8.0	10 11	mA
IC2	High−voltage current source, V_{CC} = 0	1	–	10	–	mA
CURRENT COMPARATOR T_J = 25°C (Note 2)						
I_{peak}	Maximum internal current set−point	5	405	450	495	mA
I_{Lskip}	Default internal current set−point for skip cycle operation, percentage $Ipeak_{max}$	–	–	25	–	%
t_{DEL}	Propagation delay from current detection to drain OFF state	–	–	125	–	ns
t_{LEB}	Leading Edge Blanking Duration	–	–	250	–	ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillation frequency, 65 kHz version, T_J = 25°C (Note 2)		59	65	71	kHz
f_{OSC}	Oscillation frequency, 100 kHz version, T_J = 25°C (Note 2)		90	100	110	kHz
f_{dither}	Frequency dithering compared to switching frequency (with active DSS)		–	±3.3	–	%
D_{max}	Maximum Duty−cycle		62	67	72	%
FEEDBACK SECTION						
R_{up}	Internal pull−up resistor	4	–	18	–	kΩ
t_{ss}	Internal soft−start (guaranteed by design)	–	–	1.0	–	ms
SKIP CYCLE GENERATION						
V_{skip}	Default skip mode level on FB pin	4		0.5		V
TEMPERATURE MANAGEMENT						
TSD	Temperature shutdown			150		°C
	Hysteresis in shutdown			50		°C

2. See characterization curves for temperature evolution

TYPICAL CHARACTERISTICS

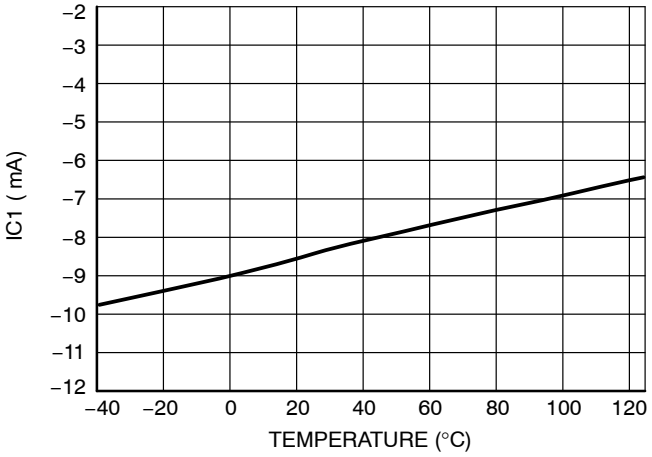


Figure 3. IC1 @ V_{CC} = 8.0 V, FB = 1.5 V vs. Temperature

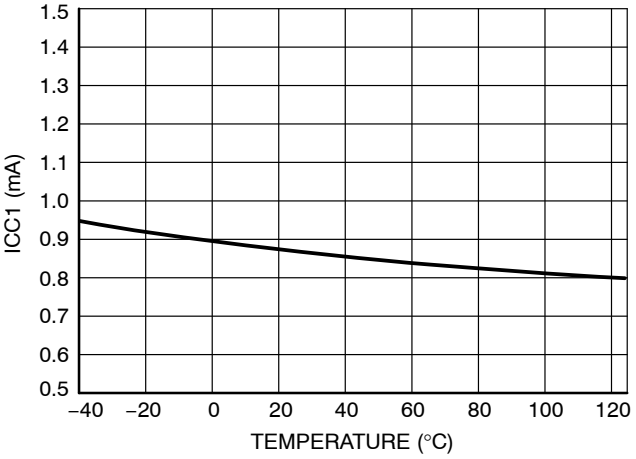


Figure 4. ICC1 @ V_{CC} = 8.0 V, FB = 1.5 V vs. Temperature

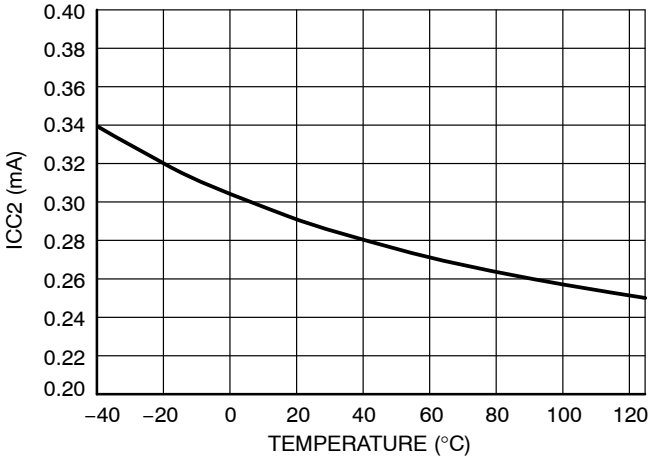


Figure 5. ICC2 @ V_{CC} = 6.0 V, FB = Open vs. Temperature

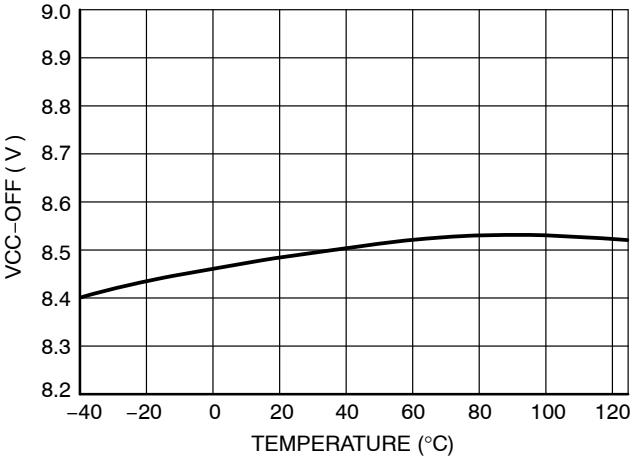


Figure 6. V_{CC} OFF, FB = 1.5 V vs. Temperature

TYPICAL CHARACTERISTICS

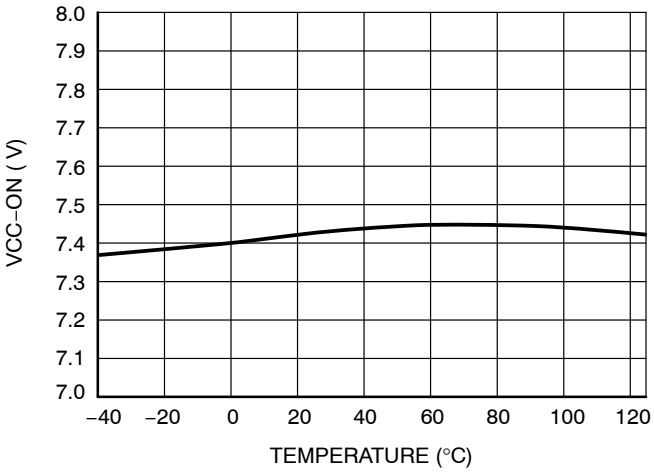


Figure 7. V_{CC} ON, FB = 3.5 V vs. Temperature

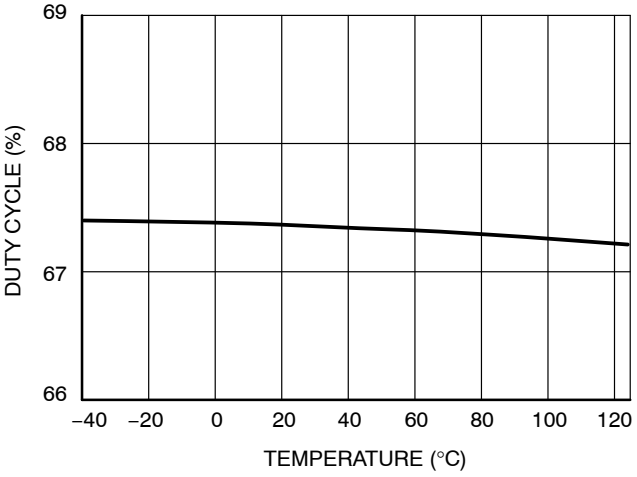


Figure 8. Duty Cycle vs. Temperature

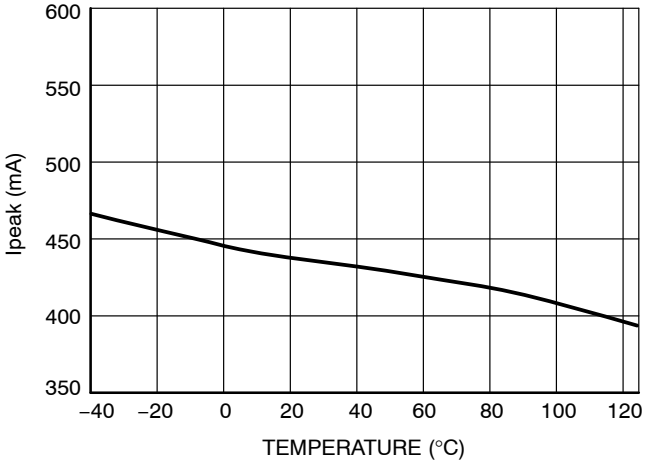


Figure 9. Ipeak−RR, V_{CC} = 8.0 V, FB = 3.5 V vs. Temperature

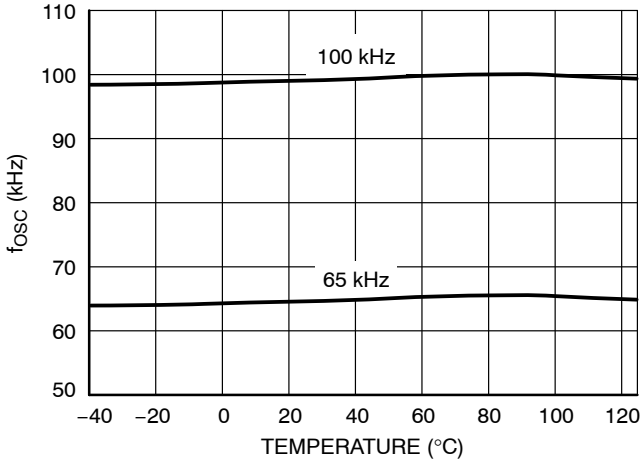


Figure 10. Frequency vs. Temperature

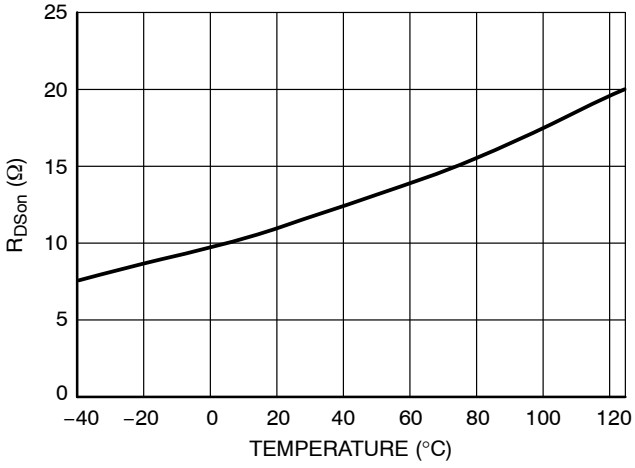


Figure 11. ON Resistance vs. Temperature

APPLICATION INFORMATION

Introduction

The NCP1015 offers a complete current−mode control solution (actually an enhanced NCP1200 controller section) together with a high−voltage power MOSFET in a monolithic structure. The component integrates everything needed to build a rugged and low−cost Switch−Mode Power Supply (SMPS) featuring low standby power. The quick selection table details the differences in operating frequency.

- No need for an auxiliary winding: ON Semiconductor Very High Voltage Integrated Circuit technology lets you supply the IC directly from the high−voltage dc rail. We call it Dynamic Self−Supply (DSS). This solution simplifies the transformer design and ensures a better control of the SMPS in difficult output conditions, e.g. constant current operations. However, for improved standby performance, an auxiliary winding can be connected to the V_{CC} pin to disable the DSS operation.
- Short−circuit protection: by permanently monitoring the feedback line activity, the IC is able to detect the presence short−circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation.
- Low standby−power: If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un−needed switching cycles, the NCP1015 drastically reduces the power wasted during light load conditions. An auxiliary winding can further help decreasing the standby power to extremely low levels by invalidating the DSS operation. Typical measurements show results below 80 mW @ 230 Vac for a typical 7 W universal power supply.
- No acoustic noise while operating: Instead of skipping cycles at high peak currents, the NCP1015 waits until the peak current demand falls below a fixed 0.25 of the maximum limit. As a result, cycle skipping can take place without having a singing transformer. You can thus select cheap magnetic components free of noise problems.
- SPICE model: a dedicated model to run transient cycle−by−cycle simulations is available but also an averaged version to help you closing the loop. Ready−to−use templates can be downloaded in OrCAD's PSpice, and INTUSOFT's IsSpice4 from ON Semiconductor web site, NCP1015 related section.

Dynamic Self−Supply

When the power supply is first powered from the mains outlet, the internal current source (typically 8 mA) is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the $V_{CC(off)}$ level (typically 8.5 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET. Figure 12 details the internal circuitry:

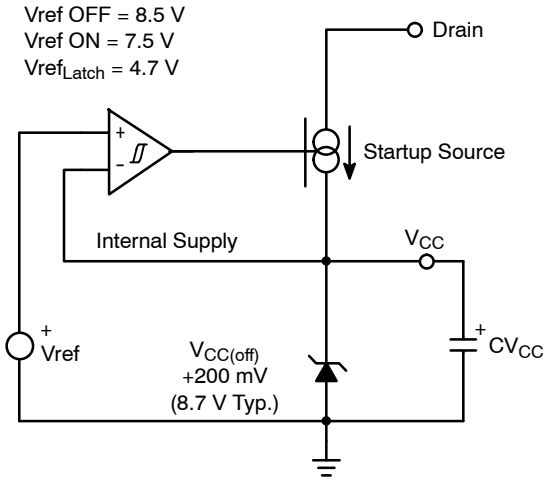


Figure 12. The Current Source Regulates V_{CC} by Introducing a Ripple

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When the DSS controller detects that V_{CC} has reached 7.5 V ($V_{CC(on)}$), it activates the internal current source to bring V_{CC} toward 8.5 V and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1 V ripple takes place on the V_{CC} pin whose average value equals ($V_{CC(off)}$ + $V_{CC(on)}$) / 2. Figure 13 shows a typical operation of the DSS.

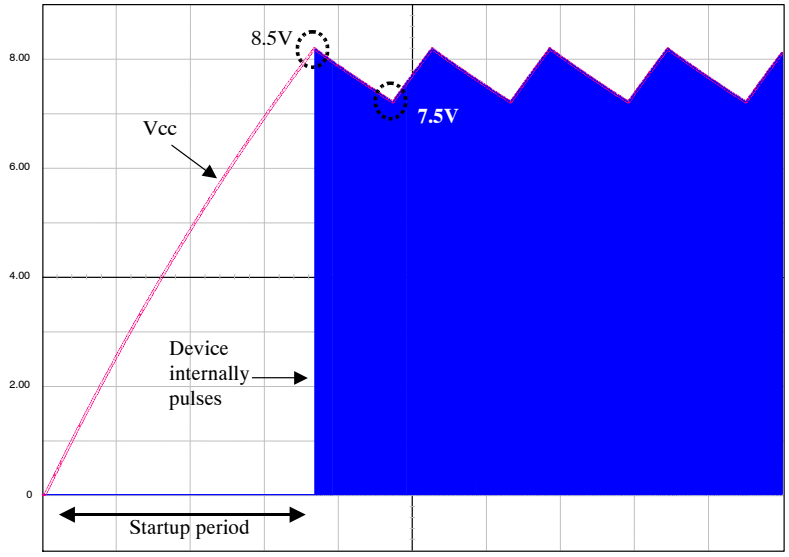


Figure 13. The Charge/Discharge Cycle over a 10 μF V_{CC} Capacitor

As one can see, the V_{CC} capacitor shall be dimensioned to offer an adequate startup time, i.e. ensure regulation is reached before V_{CC} crosses 7.5 V (otherwise the part enters the fault condition mode). If we know that ΔV = 1 V and ICC1 is 1.2 mA (for instance we selected a 11 Ω device switching at 65 kHz), then the V_{CC} capacitor can be calculated using:

$$C \geq \frac{ICC1 \cdot t_{startup}}{\Delta V} \qquad \text{(eq. 1)}$$

Let's suppose that the SMPS needs 10 ms to startup, then we will calculate C to offer a 15 ms period. As a result, C should be greater than 18 μF thus the selection of a 33 μF / 16 V capacitor is appropriate.

Short Circuit Protection

The internal protection circuitry involves a patented arrangement that permanently monitors the assertion of an internal error flag. This error flag is, in fact, a signal that instructs the controller that the internal maximum peak current limit is reached. This naturally occurs during the startup period (V_{out} is not stabilized to the target value) or when the optocoupler LED is no longer biased, e.g in a short−circuit condition or when the feedback network is broken. When the DSS normally operates, the logic checks for the presence of the error flag every time V_{CC} crosses $V_{CC(on)}$. If the error flag is low (peak limit not active) then the IC works normally. If the error signal is active, then the NCP1015 immediately stops the output pulses, reduces its internal current consumption and does not allow the startup source to activate: V_{CC} drops toward ground until it reaches the so−called latch−off level, where the current source activates again to attempt a new re−start. If the error has gone, the IC automatically resumes its operation. If the default is still there, the IC pulses during 8.5 V down to 7.5 V and enters a new latch−off phase. The resulting burst operation guarantees a low average power dissipation and lets the SMPS sustain a permanent short−circuit. Figure 14 presents the corresponding diagram:

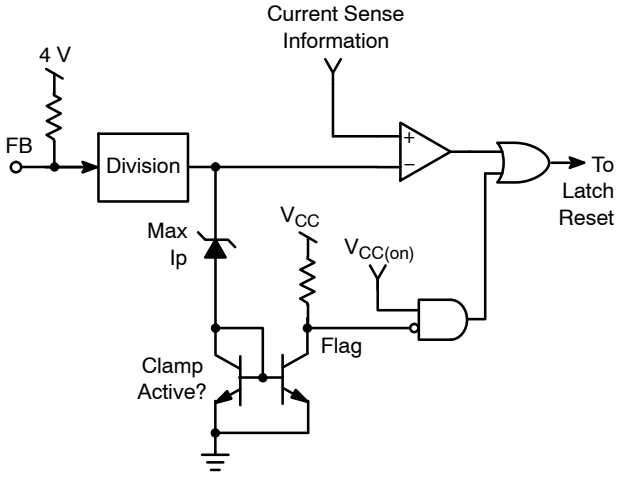


Figure 14. Simplified NCP1015 Short−Circuit Detection Circuitry

The protection burst duty−cycle can easily be computed through the various timing events as portrayed by Figure 15:

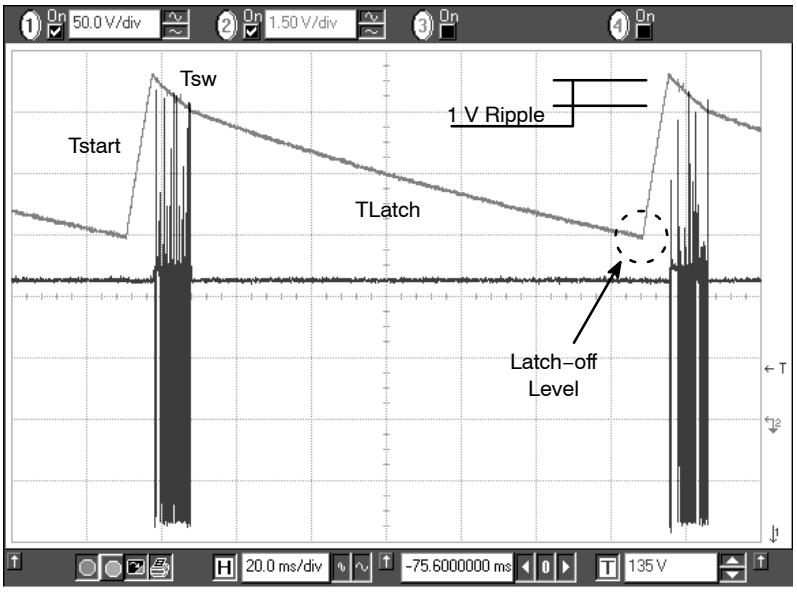


Figure 15. NCP1015 Facing a Fault Condition (V_{in} = 150 Vdc)

The rising slope from the latch−off level up to 8.5 V is expressed by:

$$P_{DSS} = V_{in} \cdot ICC1$$

$$t_{start} = \frac{\Delta V1 \cdot C}{IC1}$$

The time during which the IC actually pulses is given by:

$$t_{sw} = \frac{\Delta V2 \cdot C}{ICC1}$$

Finally, the latch−off time can be derived using the same formula topology:

$$t_{latch} = \frac{\Delta V3 \cdot C}{ICC2}$$

From these three definitions, the burst duty−cycle *D* can be computed:

$$D = \frac{t_{sw}}{t_{start} + t_{sw} + t_{latch}} \quad \text{(eq. 2)}$$

$$D = \frac{\Delta V2}{ICC1 \cdot \left(\frac{\Delta V2}{ICC1} + \frac{\Delta V1}{IC1} + \frac{\Delta V3}{ICC2}\right)} \quad \text{(eq. 3)}$$

Feeding the equation with values extracted from the parameter section gives a typical duty−cycle D of 13%, precluding any lethal thermal runaway while in a fault condition.

DSS Internal Dissipation

The Dynamic Self−Supplied pulls the energy out from the drain pin. In the Flyback−based converters, this drain level can easily go above 600 V peak and thus increase the stress on the DSS startup source. However, the drain voltage evolves with time and its period is small compared to that of the DSS. As a result, the averaged dissipation, excluding capacitive losses, can be derived by:

$$P_{DSS} = ICC1 \cdot < V_{DS(t)} > \quad \text{(eq. 4)}$$

Figure 16 shows a typical drain−ground wave−shape where leakage effects have been removed:

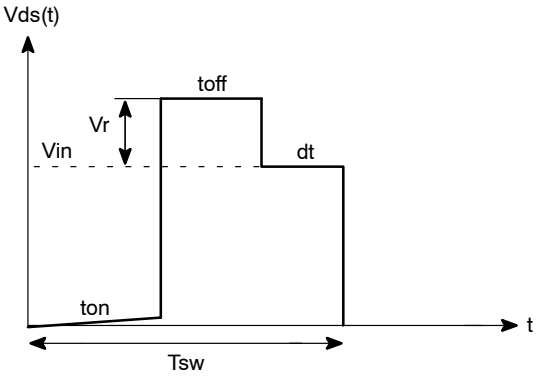


Figure 16. A Typical Drain−ground Waveshape where Leakage Effects are Not Accounted for

By looking at Figure 16 the average result can easily be derived by additive square area calculation:

$$< V_{DS(t)} > = V_{in} \cdot (1 - D) + V_r \cdot \frac{t_{off}}{t_{sw}} \quad \text{(eq. 5)}$$

By developing Equation 5 we obtain:

$$< V_{DS(t)} > = V_{in} - V_{in} \cdot \frac{t_{on}}{t_{sw}} + V_r \cdot \frac{t_{off}}{t_{sw}} \quad \text{(eq. 6)}$$

t_{off} can be expressed by:

$$t_{off} = I_p \cdot \frac{L_p}{V_r} \quad \text{(eq. 7)}$$

t_{on} can be evaluated by:

$$t_{on} = I_p \cdot \frac{L_p}{V_{in}} \quad \text{(eq. 8)}$$

Plugging Equation 7 and Equation 8 into Equation 6 leads to $<V_{ds(t)}> = V_{in}$ and thus:

$$P_{DSS} = V_{in} \cdot ICC1 \quad \text{(eq. 9)}$$

The worse case occurs at high line, when V_{in} equals 370 Vdc. With ICC1 = 1.2 mA (65 kHz version), we can expect a DSS dissipation around 440 mW. If you select a higher switching frequency version, the ICC1 increases and it is likely that the DSS consumption exceeds 500 mW. In that case, we recommend adding an auxiliary winding in order to offer more dissipation room to the power MOSFET.

Please read application note AND8125/D “Evaluating the power capability of the NCP101X members” to help selecting the right part / configuration for your application.

Lowering the Standby Power with an Auxiliary Winding

The DSS operation can bother the designer when a) its dissipation is too high b) extremely low standby power is a must. In both cases, one can connect an auxiliary winding to disable the self−supply. The current source then ensures the startup sequence only and stays in the off state as long as V_{CC} does not drop below $V_{CC(on)}$ or 7.5 V. Figure 17 shows that the insertion of a resistor (R_{limit}) between the auxiliary dc level and the V_{CC} pin is mandatory a) not to damage the internal 8.7 V zener diode during an overshoot for instance (absolute maximum current is 15 mA) b) to implement the fail−safe optocoupler protection as offered by the active clamp. Please note that there cannot be bad interaction between the clamping voltage of the internal zener and $V_{CC(off)}$ since this clamping voltage is actually built on top of $V_{CC(off)}$ with a fixed amount of offset (200 mV typical).

Self−supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (V_{nom}), this voltage can drop to below 10 V (V_{stby}) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re−fueling rate of the V_{CC} capacitor is not enough to keep a proper auxiliary voltage. Figure 18 shows a typical scope shot of a SMPS entering deep standby (output un−loaded). So care must be taken when calculating R_{limit} 1) to not excess the maximum pin current in normal operation but 2) not to drop too much voltage over R_{limit} when entering standby. Otherwise the DSS could reactivate and the standby performance would degrade. We are thus able to bound R_{limit} between two equations:

$$\frac{V_{nom} - V_{clamp}}{I_{trip}} \leq R_{lim} \leq \frac{V_{stby} - V_{CC(on)}}{ICC1} \quad \text{(eq. 10)}$$

Where:

V_{nom} is the auxiliary voltage at nominal load

V_{stdby} is the auxiliary voltage when standby is entered

I_{trip} is the current corresponding to the nominal operation. It thus must be selected to avoid false tripping in overshoot conditions.

ICC1 is the controller consumption. This number slightly decreases compared to ICC1 from the spec since the part in standby does almost not switch.

$V_{CC(on)}$ is the level above which V_{aux} must be maintained to keep the DSS in the OFF mode. It is good to shoot around 8 V in order to offer an adequate design margin, e.g. to not re−activate the startup source (which is not a problem in itself if low standby power does not matter)

Since R_{limit} shall not bother the controller in standby, e.g. keep V_{aux} to around 8 V (as selected above), we purposely select a V_{nom} well above this value. As explained before, experience shows that a 40% decrease can be seen on auxiliary windings from nominal operation down to standby mode. Let’s select a nominal auxiliary winding of 20 V to offer sufficient margin regarding 8 V when in standby (R_{limit} also drops voltage in standby). Plugging the values in Equation 10 gives the limits within which R_{limit} shall be selected:

$$\frac{20 - 8.7}{6.3\ m} \leq R_{limit} \leq \frac{12 - 8}{1.1\ m} \quad \text{(eq. 11)}$$

that is to say: 1.8 kΩ < R_{limit} < 3.6 kΩ.

If we are designing a power supply delivering 12 V, then the ratio auxiliary/power must be: 12 / 20 = 0.6. The I_{CC} current has to not exceed 6.4 mA. This will occur when V_{aux} grows−up to: 8.7 V + 1.8 k x (6.4 m + 1.1 m) = 22.2 V for the first boundary or 8.7 V + 3.6 k x (6.4 m +1.1 m) = 35.7 V for second boundary. On the power output, it will respectively give 22.6 x 0.6 = 13.3 V and 35.7 x 0.6 = 21.4 V. As one can see, tweaking the R_{limit} value will allow the selection of a given overvoltage output level. Theoretically predicting the auxiliary drop from nominal to standby is an almost impossible exercise since many parameters are involved, including the converter time constants. Fine tuning of R_{limit} thus requires a few iterations and experiments on a breadboard to check V_{aux} variations but also output voltage excursion in fault. Once properly adjusted, the fail−safe protection will preclude any lethal voltage runaways in case a problem would occur in the feedback loop.

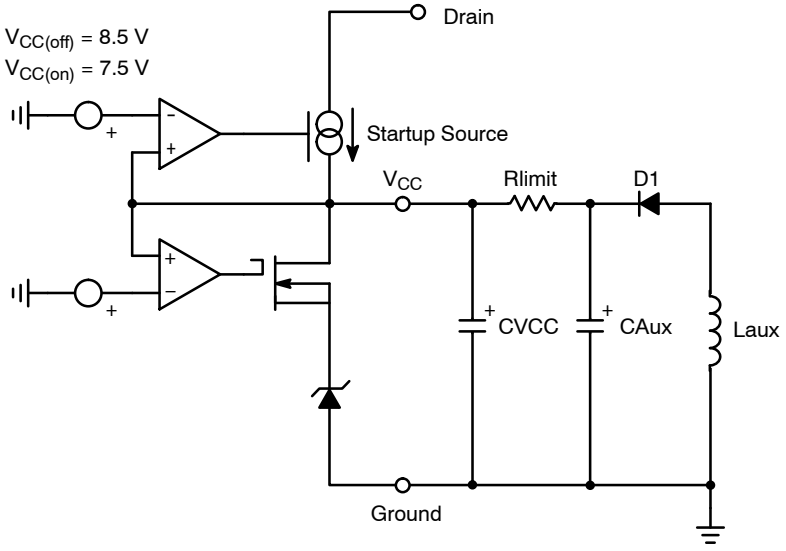


Figure 17. A Detailed View of the NCP1015 with Properly Connected Auxiliary Winding

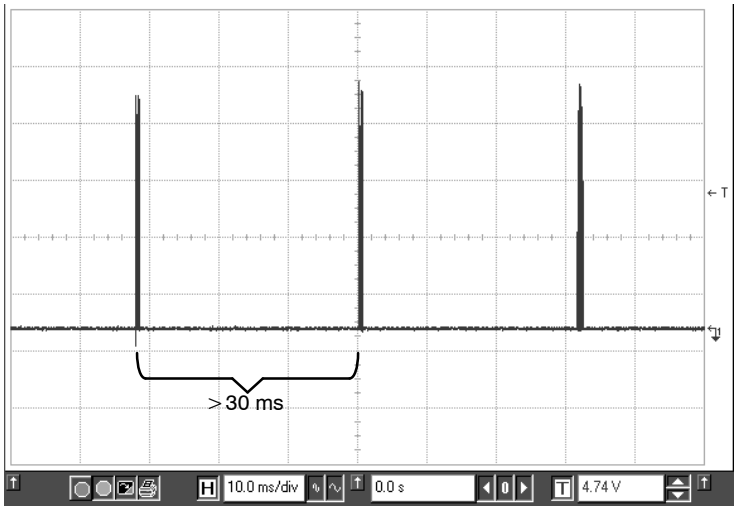


Figure 18. The Burst Frequency becomes So Low that it is Difficult to Keep an Adequate Level on the Auxiliary V_{CC}

Lowering the Standby Power with Skip−cycle

Skip cycle offers an efficient way to reduce the standby power by skipping unwanted cycles at light loads. However, the recurrent frequency in skip often enters the audible range and a high peak current obviously generates acoustic noise in the transformer. The noise takes its origins in the resonance of the transformer mechanical structure which is excited by the skipping pulses. A possible solution, successfully implemented in the NCP1200 series, also authorizes skip cycle but only when the power demand as dropped below a given level. At this time, the peak current is reduced and no noise can be heard. Figure 19 shows the peak current evolution of the NCP1015 entering standby:

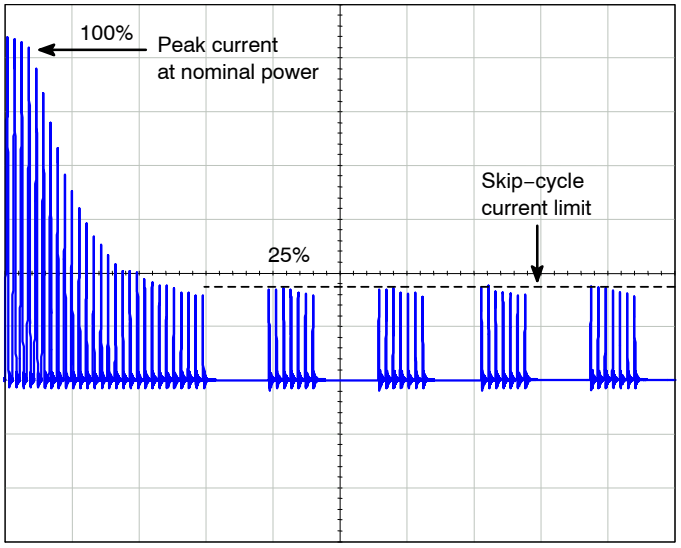


Figure 19. Low Peak Current Skip−Cycle Guarantees Noise−Free Operation

Full power operation involves the nominal switching frequency and thus avoids any noise when running.

Experiments carried on a 5 W universal mains board unveiled a standby power of 300 mW @ 230 Vac with the DSS activated and dropped to less than 100 mW when an auxiliary winding is connected.

Frequency Jittering for Improved EMI Signature

By sweeping the switching frequency around its nominal value, it spreads the energy content on adjacent frequencies rather than keeping it centered in one single ray. This offers the benefit to artificially reduce the measurement noise on a standard EMI receiver and pass the tests more easily. The EMI sweep is implemented by routing the V_{CC} ripple (induced by the DSS activity) to the internal oscillator. As a result, the switching frequency moves up and down to the DSS rhythm. Typical deviation is ±4% of the nominal frequency. With a 1 V peak−to−peak ripple, the frequency will equal 65 kHz in the middle of the ripple and will increase as V_{CC} rises or decrease as V_{CC} ramps down. Figure 20 shows the behavior we have adopted:

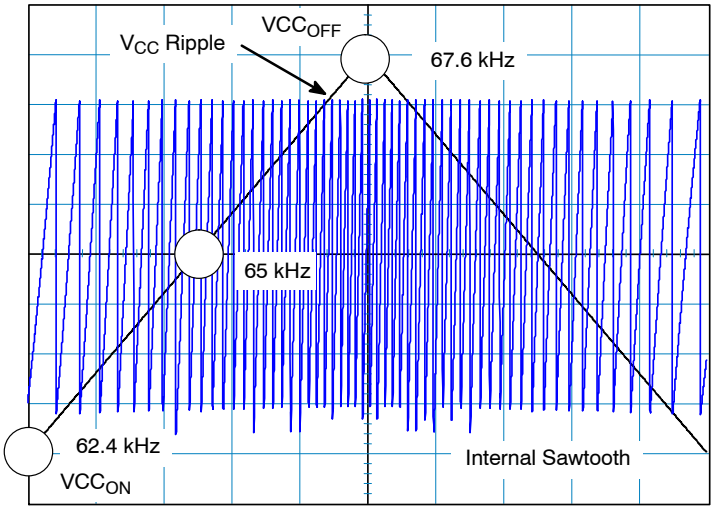


Figure 20. The V_{CC} Ripple Causes the Frequency Jittering on the Internal Oscillator Saw−tooth (65 kHz version)

Soft−Start

The NCP1015 features an internal 1 ms soft−start activated during the power on sequence (P_{ON}). As soon as V_{CC} reaches $V_{CC(off)}$, the peak current is gradually increased from nearly zero up to the maximum internal clamping level (e.g. 350 mA). This situation lasts 1 ms and further to that time period, the peak current limit is blocked to the maximum until the supply enters regulation. The soft−start is also activated during the over current burst (OCP) sequence. Every re−start attempt is followed by a soft−start activation. Generally speaking, the soft−start will be activated when V_{CC} ramps up either from zero (fresh power−on sequence) or 4.5 V, the latch−off voltage occurring during OCP. Figure 21 shows the soft−start behavior. The time scales are purposely shifted to offer a better zoom portion.

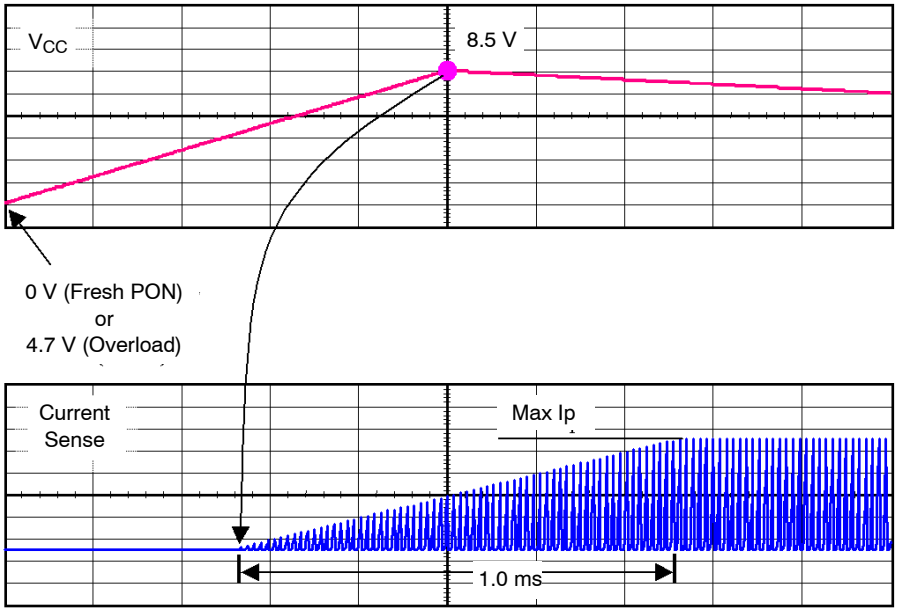


Figure 21. Soft−Start is Activated During a Start−up Sequence or an OCP Condition

Non−latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its re−start once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the internal skip level (V_{skip}), the output pulses are disabled. As soon as FB is relaxed, the IC resumes its operation. Figure 22 shows the application example:

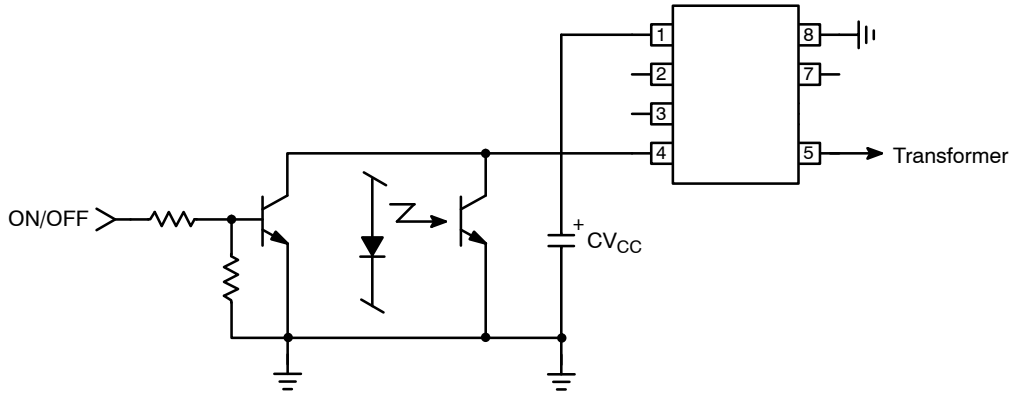


Figure 22. A Non−latching Shutdown where Pulses are Stopped as long as the NPN is Biased

Full Latching Shutdown

Other applications require a full latching shutdown, e.g. when an abnormal situation is detected (over temp or overvoltage). This feature can easily be implemented through two external transistors wired as a discrete SCR. When the OVP level exceeds the zener breakdown voltage, the NPN biases the PNP and fires the equivalent SCR, permanently bringing down the FB pin. The switching pulses are disabled until the user un−plugs the power supply.

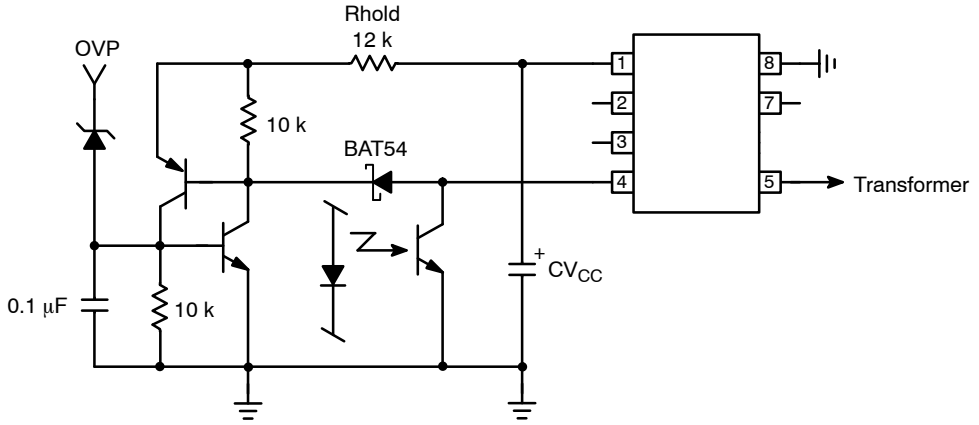


Figure 23. Two Bipolar Transistors Ensures a Total Latch−off of the SMPS in Presence of an OVP

R_{hold} ensures that the SCR stays on when fired. The bias current flowing through R_{hold} should be small enough to let the V_{CC} ramp up (8.5 V) and down (7.5 V) when the SCR is fired. The NPN base can also receive a signal from a temperature sensor. Typical bipolar can be MMBT2222 and MMBT2907 for the discrete latch. The NST3946 features two bipolar NPN + PNP in the same package and could also be used.

Power Dissipation and Heatsinking

The power dissipation of NCP1015 consists of the dissipation DSS current−source (when active) and the dissipation of MOSFET. Thus $P_{tot} = P_{DSS} + P_{MOSFET}$. When the PDIP7 package is surrounded by copper, it becomes possible to drop its thermal resistance junction−to−ambient, $R_{\theta JA}$ down to 75°C/W and thus dissipate more power. The maximum power the device can thus evacuate is:

$$P_{max} = \frac{T_{J(max)} - T_{AMB(max)}}{R_{\theta JA}} \qquad \text{(eq. 12)}$$

which gives around 1 W for an ambient of 50°C. The losses inherent to the MOSFET $R_{DS(on)}$ can be evaluated using the following formula:

$$P_{mos} = \frac{1}{3} \cdot I_p^{\,2} \cdot D \cdot R_{DS(on)} \qquad \text{(eq. 13)}$$

where I_p is the worse case peak current (at the lowest line input), D is the converter operating duty−cycle and $R_{DS(on)}$ the MOSFET resistance for T_J = 100°C. This formula is only valid for Discontinuous Conduction Mode (DCM) operation where the turn−on losses are null (the primary current is zero when you re−start the MOSFET). Figure 24 gives a possible layout to help dropping the thermal resistance. When measured on a 35 μm (1 oz.) copper thickness PCB, we obtained a thermal resistance of 75°C/W:

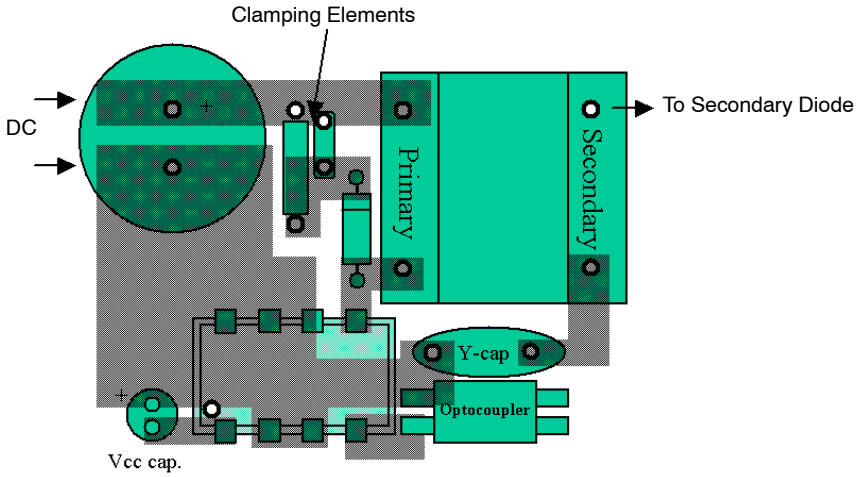


Figure 24. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction−to−Ambient

Design Procedure

The design of a SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices:

1. In any case, the lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown by Figure 25.

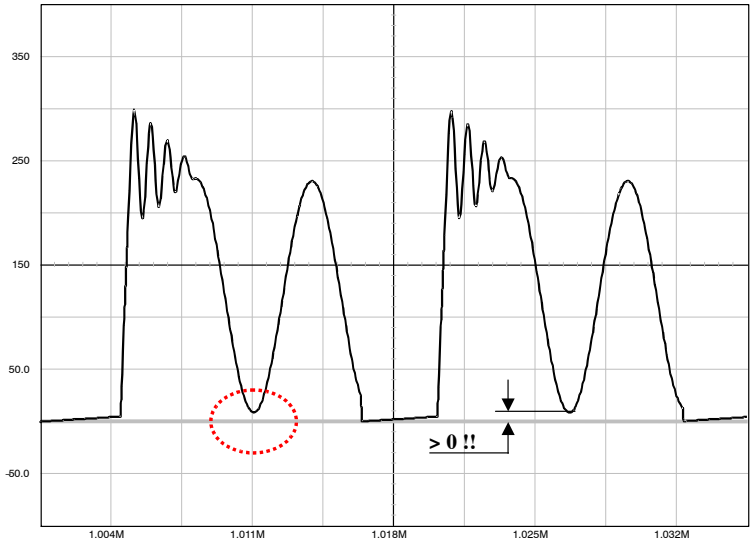


Figure 25. The Drain−Source Wave Shall Always be Positive . . .

As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

$$N \cdot (V_{out} + V_f) < V_{IN(min)} \quad \text{(eq. 14)}$$

For instance, if you operate from a 120 V dc rail and you deliver 12 V, we can select a reflected voltage of 100 VDC maximum: 120 − 100 > 0. Therefore, the turn ratio Np : Ns must be smaller than 100 / (12 + 1) = 7.7 or Np : Ns < 7.7. We will see later on how it affects the calculation.

2. Current−mode architecture is, by definition, sensitive to subharmonic oscillations. Subharmonic oscillations only occur when the SMPS is operating in Continuous Conduction Mode (CCM) together with a duty−cycle greater than 50%. As a result, we recommend operating the device in DCM only, whatever duty−cycle it implies (max. = 65%).
3. Lateral Mosfets have a poorly doped body−diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since:

$$V_{DRAIN(max)} = V_{in} + N \cdot (V_{out} + V_f) + I_p \cdot \sqrt{\frac{L_f}{C_{tot}}} \quad \text{(eq. 15)}$$

where L_f is the leakage inductance, C_{tot} the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source), N the Np : Ns turn ratio, V_{out} the output voltage, V_f the secondary diode forward drop and finally, I_p the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the V_{out} target is almost reached and I_p is still pushed to the maximum.

Taking into account all previous remarks, it becomes possible to calculate the maximum power that can be transferred at low line:

When the switch closes, V_{in} is applied across the primary inductance L_p until the current reaches the level imposed by the feedback loop. The duration of this event is called the ON time and can be defined by:

$$t_{on} = \frac{L_p \cdot I_p}{V_{in}} \quad \text{(eq. 16)}$$

At the switch opening, the primary energy is transferred to the secondary and the flyback voltage appears across L_p, reseting the transformer core with a slope of:

$$\frac{N \cdot (V_{out} + V_f)}{L_p} \cdot t_{off}$$

the t_{off} time is thus:

$$t_{off} = \frac{L_p \cdot I_p}{N \cdot (V_{out} + V_f)} \quad \text{(eq. 17)}$$

If one wants to keep DCM only, but still need to pass the maximum power, we will not allow a dead−time after the core is reset, but rather immediately re−start. The switching time t_{sw} can be expressed by:

$$t_{sw} = t_{off} + t_{on} = L_p \cdot I_p \cdot \left(\frac{1}{V_{in}} + \frac{1}{N \cdot (V_{out} + V_f)} \right) \quad \text{(eq. 18)}$$

The Flyback transfer formula dictates that:

$$\frac{P_{out}}{\eta} = \frac{1}{2} \cdot L_p \cdot I_p^2 \cdot f_{sw} \quad \text{(eq. 19)}$$

which, by extracting I_p and plugging into Equation 19 leads to:

$$t_{sw} = L_p \sqrt{\frac{2 \cdot P_{out}}{\eta \cdot f_{sw} \cdot L_p}} \cdot \left(\frac{1}{V_{in}} + \frac{1}{N \cdot (V_{out} + V_f)} \right) \quad \text{(eq. 20)}$$

Extracting L_p from Equation 20 gives:

$$L_{Pcritical} = \frac{(V_{in} \cdot V_r)^2 \cdot \eta}{2 \cdot f_{sw} \cdot [P_{out} \cdot (V_r^2 + 2 \cdot V_r \cdot V_{in} + V_{in}^2)]} \quad \text{(eq. 21)}$$

with $V_r = N \cdot (V_{out} + V_f)$ and η the efficiency.

If L_p critical gives the inductance value above which DCM operation is lost, there is another expression we can write to connect L_p, the primary peak current bounded by the NCP1015 and the maximum duty−cycle that needs to stay below 50%:

$$L_{P(max)} = \frac{D_{max} \cdot V_{IN(min)} \cdot t_{sw}}{I_{P(max)}} \quad \text{(eq. 22)}$$

where $V_{IN(min)}$ corresponds to the lowest bulk voltage, hence the longest ton duration or largest duty−cycle. $I_{P(max)}$ is the available peak current from the considered part, e.g. 450 mA typical for the NCP1015 (however, the minimum value of this parameter shall be considered for reliable evaluation). Combining Equations 21 and 22 gives the maximum theoretical power you can pass respecting the peak current capability of the NCP1015, the maximum duty−cycle and the discontinuous mode operation:

$$P_{max} = t_{sw}^2 \cdot V_{IN(min)}^2 \cdot V_r^2 \cdot \eta \cdot \frac{f_{sw}}{(2L_{P(max)}V_r^2 + 4L_{P(max)}V_rV_{IN(min)} + V_{IN(min)}^2)} \quad \text{(eq. 23)}$$

From Equation 22 we obtain the operating duty−cycle D:

$$D = \frac{I_p \cdot L_p}{V_{in} \cdot t_{sw}} \quad \text{(eq. 24)}$$

This lets us calculate the RMS current circulating in the MOSFET:

$$I_{D(rms)} = I_p \cdot \sqrt{\frac{D}{3}} \quad \text{(eq. 25)}$$

From this equation, we obtain the average dissipation in the MOSFET:

$$P_{avg} = \frac{1}{3} \cdot I_p^2 \cdot D \cdot R_{DS(on)} \quad \text{(eq. 26)}$$

to which switching losses shall be added.

If we stick to Equation 23, compute Lp and follow the above calculations, we will discover that a power supply built with the NCP1015 and operating from a 100 Vac line minimum will not be able to deliver more than 7 W continuous, regardless of the selected switching frequency (however the transformer core size will go down as f_{sw} is increased). This number grows up significantly when operated from single European mains (18 W).

For more different flyback converters then are the below examples we recommend use following support:

1) Application note AND8125/D “Evaluating the power capability of the NCP101X members”

2) Application note AND8134/D “Designing Converters with the NCP101X members.”

3) Application note AND8142/D “A 6W/12W Universal mains adapter with NCP101X series”.

4) The PSpice or Orcad simulation models

Example 1.: A 12 V 7.0 W SMPS Operating on a Large Mains with NCP1015:

V_{in} = 100 Vac ÷ 250 Vac or 140 Vdc ÷ 350 Vdc once rectified, assuming a low bulk ripple

Efficiency = 80%

V_{out} = 12 V, I_{out} = 580 mA

f_{sw} = 65 kHz

$I_{P(max)}$ = 450 mA − 10% = 405 mA

Applying the above equations leads to :

Selected maximum reflected voltage = 120 V

with V_{out} = 12 V, secondary drop = 0.5 V → Np : Ns = 1 : 0.1

L_p critical = 3.9 mH

I_p = 250 mA

D_{max} = 0.39

$I_{DRAIN(rms)}$ = 90 mA

P_{MOSFET} = 202 mW at $R_{DS(on)}$ = 25 Ω (T_J > 100°C)

P_{DSS} = 1.2 mA x 350 V = 420 mW, if DSS is used

Secondary diode voltage stress = (350 x 0.1) + 12 = 47 V (e.g. a MBRS360T3, 3 A / 60 V would fit)

Example 2.: A 12 V 16 W SMPS Operating on Narrow European Mains with NCP1015:

V_{in} = 230 Vac ± 15%, or 276 Vdc ÷ 370 Vdc

Efficiency = 80%

V_{out} = 12 V, I_{out} = 1.25 A

f_{sw} = 65 kHz

$I_{P(max)}$ = 450 mA − 10% = 405 mA

Applying the equations leads to :

Selected maximum reflected voltage = 250 V

with V_{out} = 12 V, secondary drop = 0.5 V → Np : Ns = 1:0.05

L_p = 7,2 mH

I_p = 0.27 mA

D_{max} = 0.41

$I_{DRAIN(rms)}$ = 100 mA

P_{MOSFET} = 250 mW at $R_{DS(on)}$ = 25 Ω (T_J > 100°C)

P_{DSS} = 1.2 mA x 370 V = 444 mW, if DSS is used below an ambient of 50°C.

Secondary diode voltage stress = (370 x 0.05) + 12 = 30.5 V (e.g. a MBRS340T3, 3 A / 40 V)

Please note that these calculations assume a flat DC rail whereas a 10 ms ripple naturally affects the final voltage available on the transformer end. Once the Bulk capacitor has been selected, one should check that the resulting ripple (min V_{bulk}?) is still compatible with the above calculations. As an example, to benefit from the largest operating range, a 7 W board was built with a 47 μF bulk capacitor which ensured discontinuous operation even in the ripple minimum waves.

MOSFET Protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BVdss which is 700 V. Figures 26A, B, and C present possible implementations:

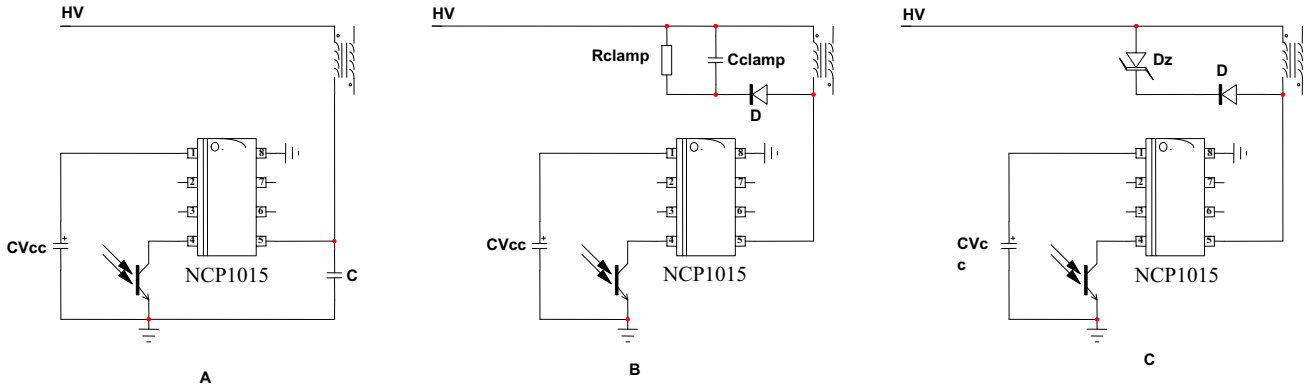


Figure 26. Different Options to Clamp the Leakage Spike

Figure 26A: The simple capacitor limits the voltage according to Equation 15. This option is only valid for low power applications, e.g. below 5 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with Equation 15. Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses.

Figure 26B: The most standard circuitry called the RCD network. You calculate R_{clamp} and C_{clamp} using the following formulas:

$$R_{clamp} = \frac{2 \cdot V_{clamp} \cdot (V_{clamp} - (V_{out} + V_f\,sec) \cdot N)}{L_{leak} \cdot I_p{}^2 \cdot f_{sw}} \quad \text{(eq. 27)}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot f_{sw} \cdot R_{clamp}} \quad \text{(eq. 28)}$$

V_{clamp} is usually selected 50−80 V above the reflected value N x (V_{out} + V_f). The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when I_p and V_{in} are maximum and V_{out} is close to reach the steady−state value.

Figure 26C: This option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

Typical Application Examples

A 6.5 W NCP1015−based Flyback converter. (For evaluation a universal NCP1012 demo−board can be used)

Figure 27 shows a converter originally built with a NCP1012 which can be easily used for evaluation of NCP1015 device delivering 6.5 W from a universal volts input range. The board uses the Dynamic Self−Supply and a simplified zener−type feedback. This configuration was selected for cost reasons and a more precise circuitry can be used, e.g. based on a TL431:

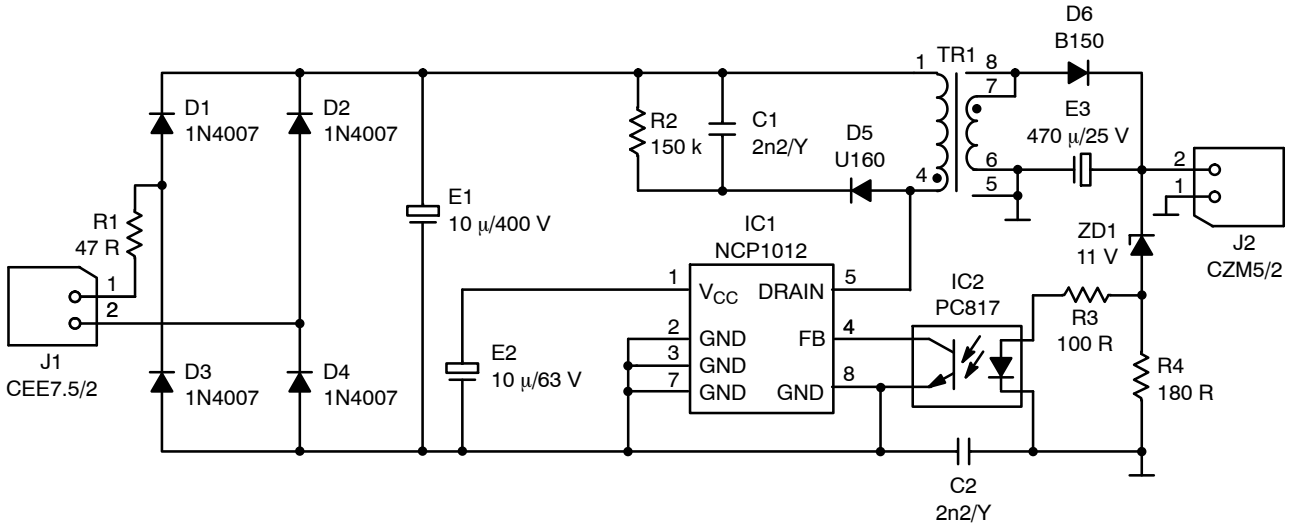


Figure 27. A NCP1012−based Flyback Converter Delivering 6.5 W

The converter built according to Figure 28 layouts, gave the following results:

- Efficiency at V_{in} = 100 Vac and P_{out} = 6.5 W = 75.7%
- Efficiency at V_{in} = 230 Vac and P_{out} = 6.5 W = 76.5%

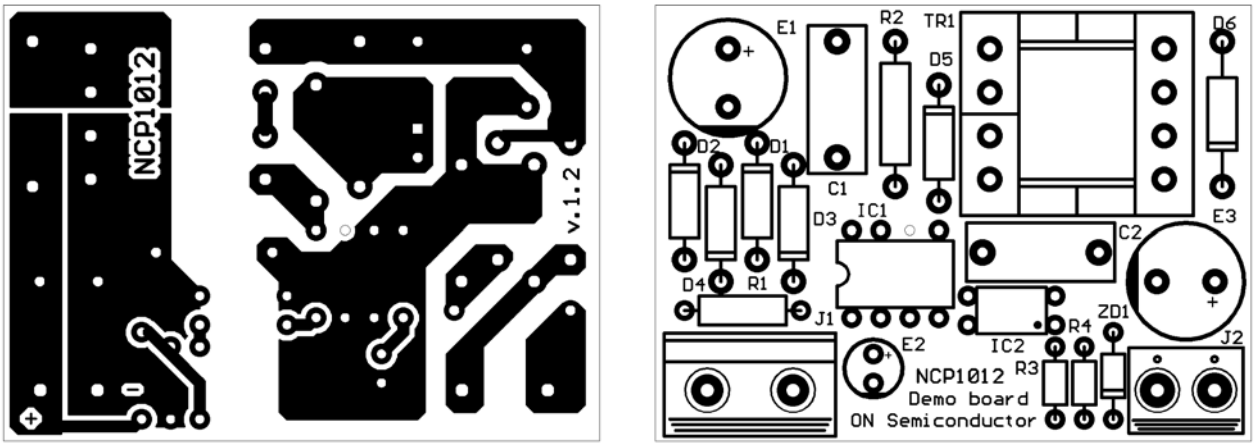


Figure 28. The NCP1012−based PCB Layout and its Associated Component Placement

A 7.0 W NCP1015−based Flyback Converter Featuring Low Standby Power

Figure 29 shows another typical application showing a NCP1015−65 kHz operating in a 7 W converter up to 70°C of ambient temperature. We can grow−up the output power since an auxiliary winding is used, the DSS is disabled, and thus offering more room for the MOSFET. In this application, the feedback is made via a TLV431 whose low bias current (100 μA min) helps to lower the no−load standby power.

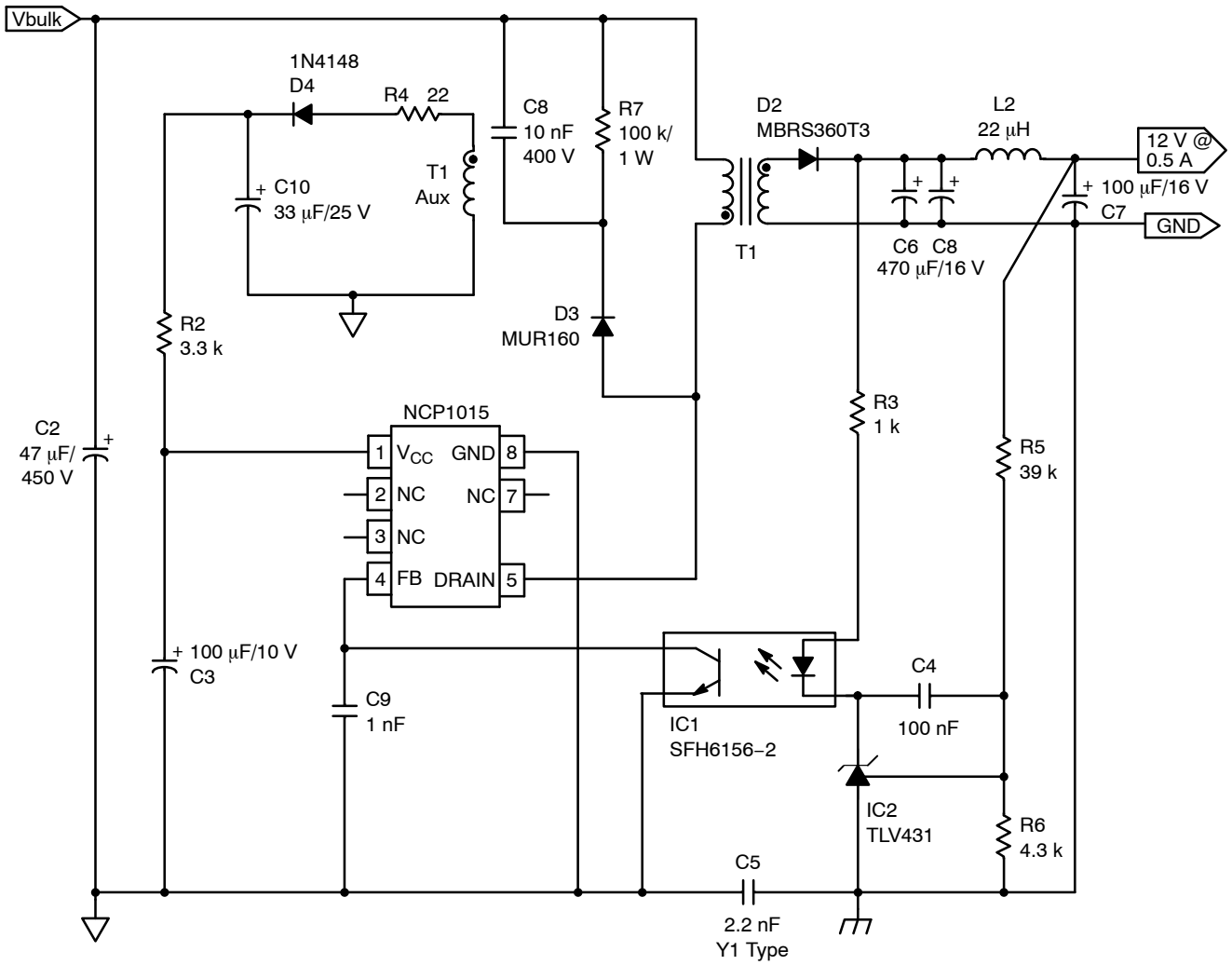


Figure 29. A Typical Converter Delivering 5 W from a Universal Mains

Measurements have been taken from a demonstration board implementing Figure 12 12's sketch and the following results were achieved, with either the auxiliary winding in place or through the Dynamic Self−Supply:

V_{in} = 230 Vac, auxiliary winding, P_{out} = 0, P_{in} = 60 mW

V_{in} = 100 Vac, auxiliary winding, P_{out} = 0, P_{in} = 42 mW

V_{in} = 230 Vac, Dynamic Self−Supply, P_{out} = 0, P_{in} = 300 mW

V_{in} = 100 Vac, Dynamic Self−Supply, P_{out} = 0, P_{in} = 130 mW

P_{out} = 7 W, η = 81% @ 230 Vac, with aux winding

P_{out} = 7 W, η = 81.3% @ 100 Vac, with aux winding

For a quick evaluation of Figure 29 application example, the following transformers are available from Coilcraft:

A9619−C, L_p = 3 mH, Np : Ns = 1: 0.1, 7 W application on universal mains, including auxiliary winding, NCP1015−65 kHz

A0032−A, L_p = 6 mH, Np : Ns = 1: 0.055, 10 W application on European mains, DSS operation only, NCP1015−65 kHz

Coilcraft
1102 Silver Lake Road
CARY, IL 60013
Email: info@coilcraft.com
Tel. : 847−639−6400
Fax.: 847−639−1469

ORDERING INFORMATION

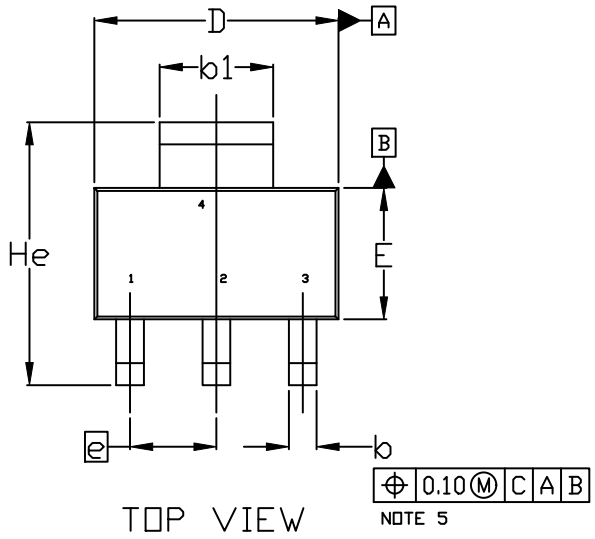
Device Order Number	Frequency (kHz)	Package Type	Shipping†	R_{DSon} (Ω)	Ipk (mA)
NCP1015AP065G	65	PDIP−7 (Pb−Free)	50 Units / Rail	11	450
NCP1015AP100G	100	PDIP−7 (Pb−Free)		11	450
NCP1015ST65T3G	65	SOT−223 (Pb−Free)	4000 / Tape & Reel	11	450
NCP1015ST100T3G	100	SOT−223 (Pb−Free)		11	450

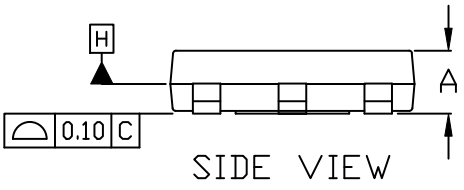
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

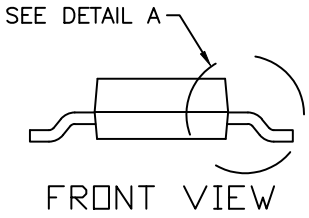
SCALE 1:1

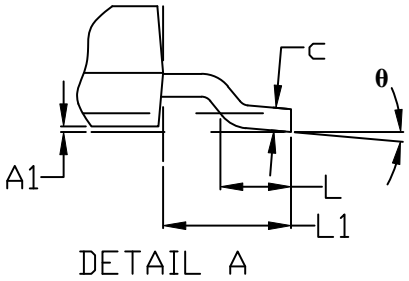
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



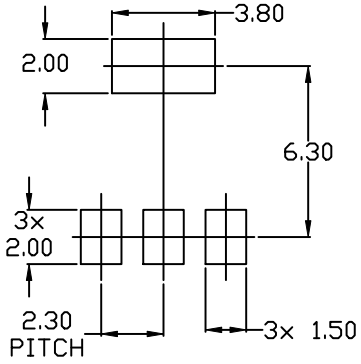






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

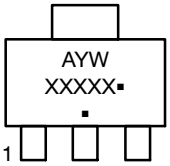
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

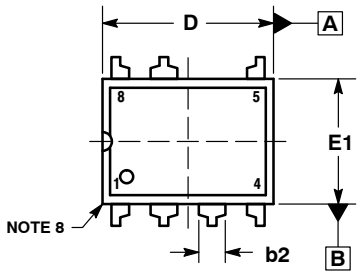
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2

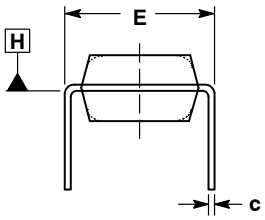
PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C

DATE 22 APR 2015

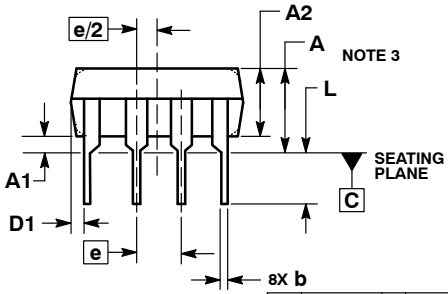
SCALE 1:1



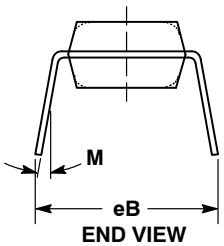
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

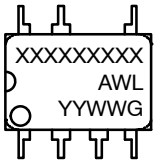


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON11774D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**PDIP−7 (PDIP−8 LESS PIN 6)**		**PAGE 1 OF 1**

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