NCL30170

Direct AC Drive LED Driver for Power Factor Correction and Precise Constant Current Regulation

The NCL30170 is a linear regulating constant current LED controller in smart lighting and phase−cut dimming application. The controller manages multiple series LED current in ON Semiconductor's proprietary auto−commutation topology with high CC regulation accuracy and superior performance in PF and THD.

The device provides wide analog dimming range with linear dimming curve and low current consumption in the standby mode. In phase−cut dimming application, input current shape modulation provides both good PF and excellent dimmer compatibility. Self−biasing high−voltage regulator supplies stable IC bias voltage with fast startup time. The NCL30170 has several protections such as thermal shutdown, input over voltage protection, sensing resistor short protection and LED over current limit for high system reliability.

Features

- Accurate CC Regulation by Closed Loop Control
- High PF and Low THD: 0.99 PF and less than 10% THD
- Wide Analog Dimming down to 5%
- Input Voltage and Current Modulation for High Phase−cut Dimmer Compatibility
- Low System BOM
- High Voltage Startup
- Flexible Selection of the Number of LED Channels
- Wide Range Power Design in 5 ~ 300 W with Single Controller
- Robust Protection Features
  - Input Over Voltage Protection
  - Sensing Resistor Short Protection
  - Thermal Shutdown
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- LED Lighting System

ON Semiconductor®

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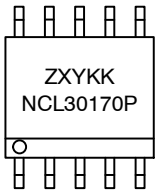
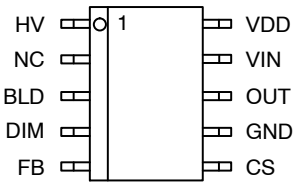
SOIC10
R2 SUFFIX
CASE 751EE

MARKING DIAGRAM



NCL30170 = Specific Device Code
Z = Plant Code
X = 1 Digit Year Code
Y = 1 Digit Week Code
KK = 2 Digit Lot Traceability Code
P = Product Option
(A = HVDIM, B = LVDIM)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 12 of this data sheet.

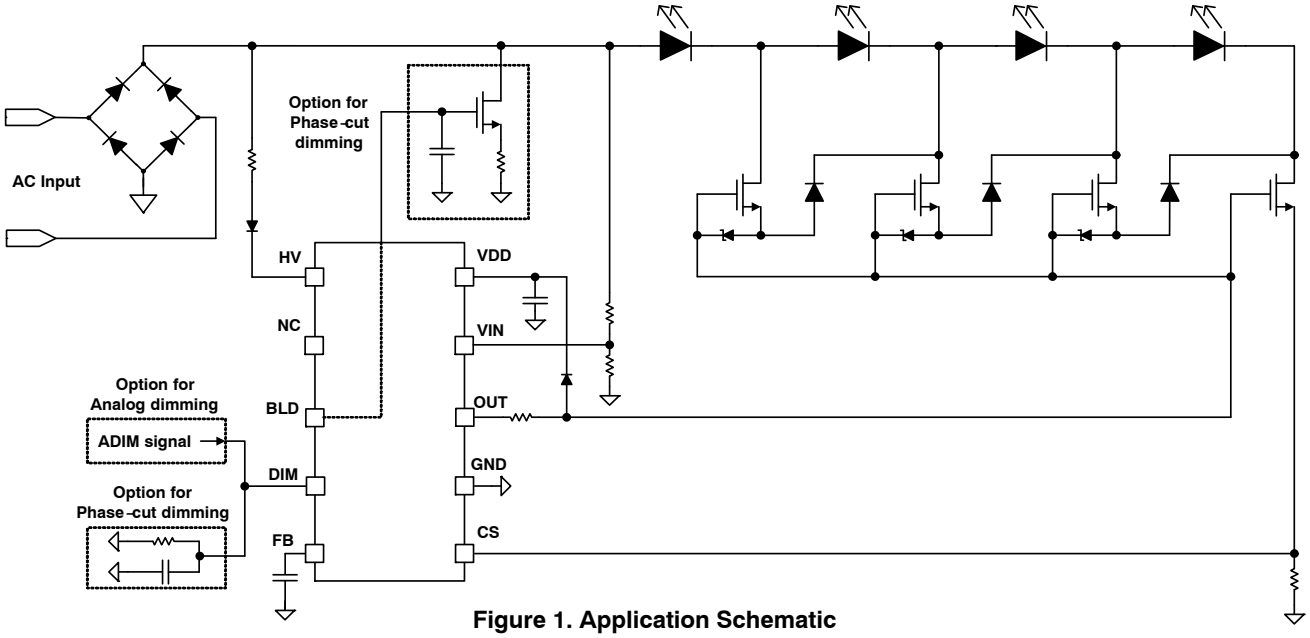


Figure 1. Application Schematic

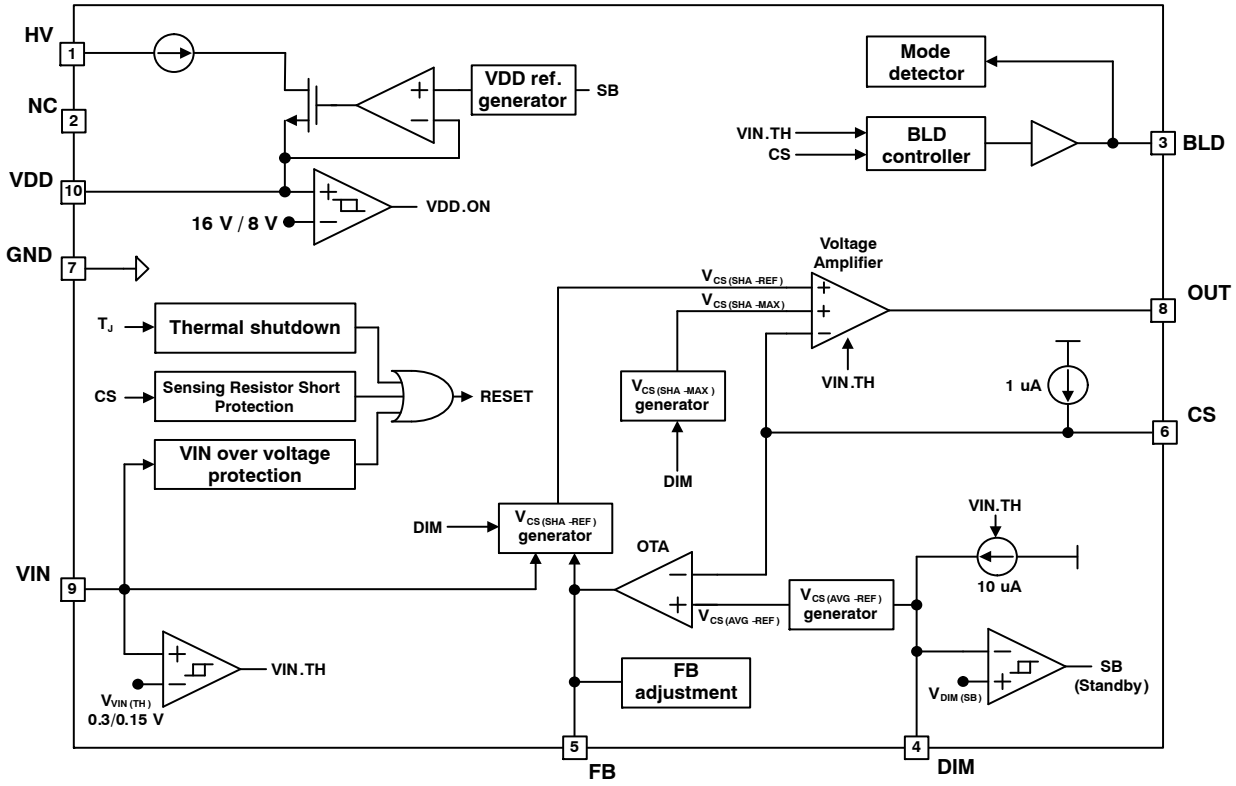


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	HV	High Voltage Startup	This pin is connected to the rectified input voltage for fast startup and self biasing.
2	NC	No Connection	
3	BLD	Bleeding Control	This pin controls the external bleeding MOSFET for phase−cut dimming.
4	DIM	Dimming Input	Analog dimming signal is provided to this pin. In phase−cut dimming, this pin is connected to a resistor and a capacitor in parallel to obtain phase angle information.
5	FB	Feedback	This pin is connected to the compensation network.
6	CS	Current Sense	This pin monitors LED current.
7	GND	Ground.	The controller ground.
8	OUT	Output Drive	This pin is connected to drive external regulator switch.
9	VIN	Input Voltage Detection	This pin is connected to the resistive divider to detect input voltage.
10	VDD	Power Supply	This pin voltage is regulated by internal self biasing HV supply.

Table 2. NCL30170 VERSION

Part Number	Description
NCL30170ADR2G	Option A: HVDIM version has analog DIM voltage control in 0 ~ 3 V.
NCL30170BDR2G	Option B: LVDIM version has analog DIM voltage control in 0 ~ 1.5 V.

Table 3. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
HV Pin Voltage Range	$V_{HV(MAX)}$	560	V
VDD, BLD, OUT, VIN Pin Voltage Range	$V_{MV(MAX)}$	−0.3 to 26	V
FB, DIM, CS Pin Voltage Range	$V_{LV(MAX)}$	−0.3 to 6	V
CS Pin Negative Pulse Voltage at I_{LV} < 0.2 A and t_{PULSE} < 5 μs	$V_{LV(PULSE)}$	−1.5	V
Maximum Power Dissipation (T_A < 50°C)	$P_{D(MAX)}$	663	mW
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Junction−to−Ambient Thermal Impedance	$R_{\theta JA}$	158	°C/W
Junction−to−Case Thermal Impedance	$R_{\theta JC}$	39	°C/W
ESD Capability, Human Body Model (Note 1)	ESDHBM	1.5	kV
ESD Capability, Charged Device Model (Note 1)	ESDCDM	1.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS V_{DD} = 20 V and T_J = −40 ~ 125°C unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VDD SECTION						
VDD Regulation Voltage	V_{HV} = 80 V	$V_{DD(REG)}$	19.5	20	20.5	V
VDD Regulation High Voltage at Standby	V_{HV} = 80 V , V_{DIM} = 0 V	$V_{DD(SB-H)}$	9.5	10	10.5	V
VDD Regulation Low Voltage at Standby	V_{HV} = 80 V , V_{DIM} = 0 V	$V_{DD(SB-L)}$	9.0	9.5	10.0	V
IC Turn−On Threshold Voltage		$V_{DD(ON)}$	15	16	17	V
IC Turn−Off Threshold Voltage		$V_{DD(OFF)}$	7	8	9	V
Startup HV Current	V_{HV} = 80 V, V_{DD} = $V_{DD(ON)}$ − 1.6 V	$I_{DD(ST-HV)}$	1.35			mA
Startup Current	V_{HV} = 80 V, V_{DD} = $V_{DD(ON)}$ − 1.6 V	$I_{DD(ST)}$		90	200	μA
Operating Current	V_{HV} = 80 V	$I_{DD(OP)}$		0.8	1.2	mA
Standby Current	V_{HV} = 80 V, T_J = 25°C	$I_{DD(SB)}$			250	μA
DIM SECTION						
DIM Sourcing Current	V_{DIM} = 3.5 V	I_{DIM}	9	10	11	μA
DIM Voltage for 99% $V_{CS(AVG-REF)}$ at HVDIM	A version	$V_{DIM(MAX-EFF-HV)}$	2.91	2.97	3.03	V
DIM Voltage for 99% $V_{CS(AVG-REF)}$ at LVDIM	B version	$V_{DIM(MAX-EFF-LV)}$	1.428	1.488	1.548	V
Standby Enabling DIM Voltage at HVDIM	A version	$V_{DIM(SB-ENA-HV)}$	0.15	0.2	0.25	V
Standby Disabling DIM Voltage at HVDIM	A version	$V_{DIM(SB-DIS-HV)}$	0.25	0.3	0.35	V
Standby Enabling DIM Voltage at LVDIM	B version	$V_{DIM(SB-ENA-LV)}$	0.05	0.1	0.15	V
Standby Disabling DIM Voltage at LVDIM	B version	$V_{DIM(SB-DIS-LV)}$	0.15	0.2	0.25	V
Standby Delay Time		$t_{SB(DELAY)}$		10		ms
CS SECTION						
CS Average Regulation Voltage at HVDIM (Test in closed loop CC regulation)	A version V_{DIM} = 3.1 V V_{DIM} = 3.1 V (Note 2) V_{DIM} = 1.0 V V_{DIM} = 1.0 V (Note 2) V_{DIM} = 0.3 V (T_J = 25°C) V_{DIM} = 0.3 V (T_J = 25°C) (Note 2)	$V_{CS(AVG-REG-HV)}$	 1.432 1.455 0.253 0.265 0.025 0.043	 1.500 1.500 0.300 0.300 0.050 0.050	 1.568 1.545 0.347 0.335 0.075 0.057	V
CS Average Regulation Voltage at LVDIM (Test in closed loop CC regulation)	B version V_{DIM} = 1.6 V V_{DIM} = 1.6 V (Note 2) V_{DIM} = 1.0 V V_{DIM} = 1.0 V (Note 2) V_{DIM} = 0.2 V V_{DIM} = 0.2 V (T_J = 25°C) (Note 2)	$V_{CS(AVG-REG-LV)}$	 1.432 1.455 0.805 0.825 0.025 0.043	 1.500 1.500 0.875 0.875 0.050 0.050	 1.568 1.545 0.945 0.925 0.075 0.057	V
Temperature Coefficient of CS Regulation	V_{DIM} = 0.3 V A Ver. Design guaranteed	$TC_{VCS(AVG-REG)}$	−180		+180	μV/°C
CS Source Current		$I_{CS(SOURCE)}$	0.7	1.0	1.3	μA
FB SECTION						
FB OTA Sink Current	V_{CS} = 2.5 V	$I_{FB(SINK)}$	26	34	47	μA
FB OTA Source Current	V_{CS} = 0.5 V	$I_{FB(SOURCE)}$	26	34	47	μA
FB OTA Transconductance		$g_{M(FB)}$	26	34	47	μmho
FB OTA High Voltage	V_{DIM} = 3.3 V, V_{CS} = 0.5 V	$V_{FB(HIGH)}$	4.7			V

2. Drift after IC reliability test (HTOL, HOSL, TMCL, HAST) is not included.
3. If over−temperature protection is activated, the power system enters Protection Mode and output is disabled. Device operation above the maximum junction temperature is not guaranteed.

Table 5. ELECTRICAL CHARACTERISTICS V_{DD} = 20 V and T_J = −40 ~ 125°C unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
FB SECTION						
FB OTA Low Voltage	V_{DIM} = 3.3 V, V_{CS} = 2.5 V	$V_{FB(LOW)}$			0.1	V
FB Clamping Voltage at PCDIM		$V_{FB(CLP-PC)}$	1.7	1.8	1.9	V
VIN SECTION						
VIN−TH High Threshold		$V_{VIN(TH-H)}$	0.25	0.30	0.35	V
VIN−TH Low Threshold		$V_{VIN(TH-L)}$	0.10	0.15	0.20	V
OUT SECTION						
OUT Voltage High		$V_{OUT(H)}$	19			V
OUT Voltage Low		$V_{OUT(L)}$			1	V
Voltage Amplifier Input Offset		$V_{OUT(OFFSET)}$			10	mV
Voltage Amplifier Open Loop Gain	Design guaranteed	$A_{VA(OPEN)}$		100		dB
Voltage Amplifier Bandwidth	Design guaranteed	$f_{VA(BW)}$		190		kHz
BLD SECTION						
BLD Reset Time		$t_{BLD(RST)}$	56	80	104	μs
Phase Cut DIM Mode Monitoring Time		$t_{BLD(PCDIM)}$	3.5	5.0	6.8	μs
Phase Cut DIM Mode Monitoring Voltage		$V_{BLD(PCDIM)}$	2.75	3.25	3.75	V
Internal BLD Resistance		R_{BLD}	85	110	135	kΩ
BLD Enabling CS Voltage		$V_{CS(BLD)}$	150	200	250	mV
PROTECTION SECTION						
Thermal Shut Down Temperature	Design guaranteed (Note 3)	T_{SD}	145	160	175	°C
Thermal Shut Down Hysteresis	Design guaranteed	$T_{SD(HYS)}$		30		°C
Input Over Voltage Protection Threshold		$V_{VIN(OVP)}$	3.5	4.0	4.5	V
Sensing Resistor Short Current		I_{SRSP}	30		90	mA
Sensing Resistor Short Voltage		V_{SRSP}	60	100	140	mV

2. Drift after IC reliability test (HTOL, HOSL, TMCL, HAST) is not included.
3. If over−temperature protection is activated, the power system enters Protection Mode and output is disabled. Device operation above the maximum junction temperature is not guaranteed.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

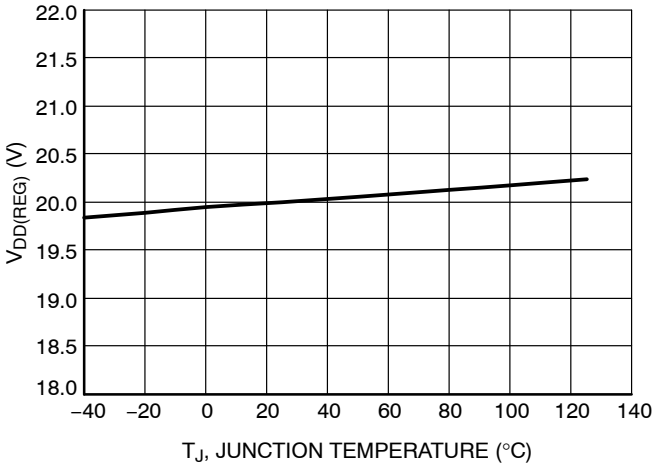


Figure 3. $V_{DD(REG)}$ vs. Temperature

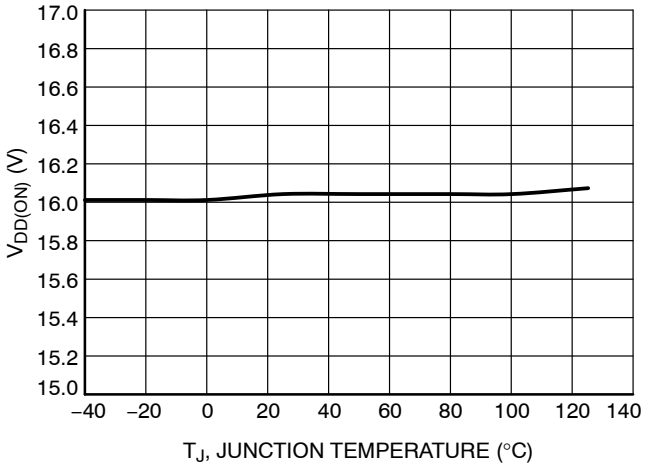


Figure 4. $V_{DD(ON)}$ vs. Temperature

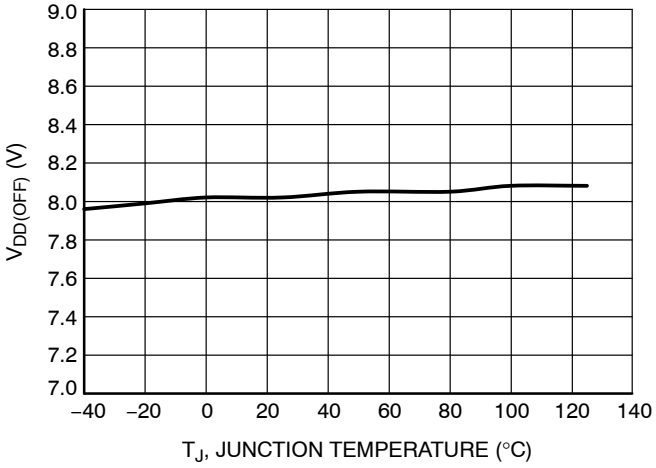


Figure 5. $V_{DD(OFF)}$ vs. Temperature

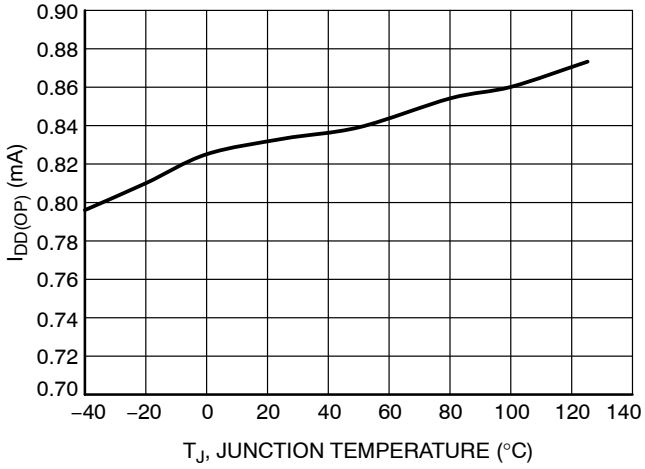


Figure 6. $I_{DD(OP)}$ vs. Temperature

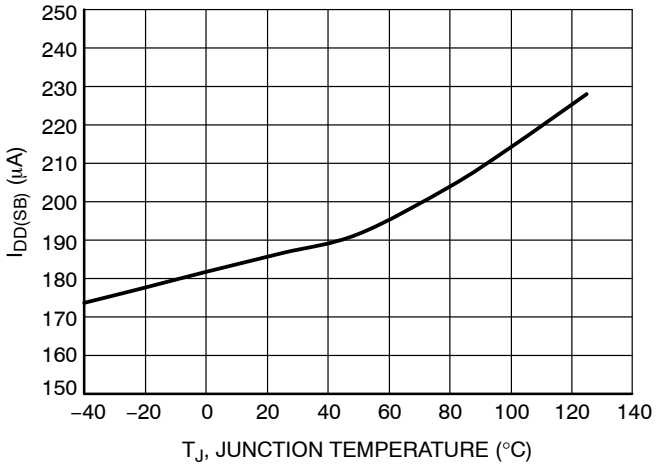


Figure 7. $I_{DD(SB)}$ vs. Temperature

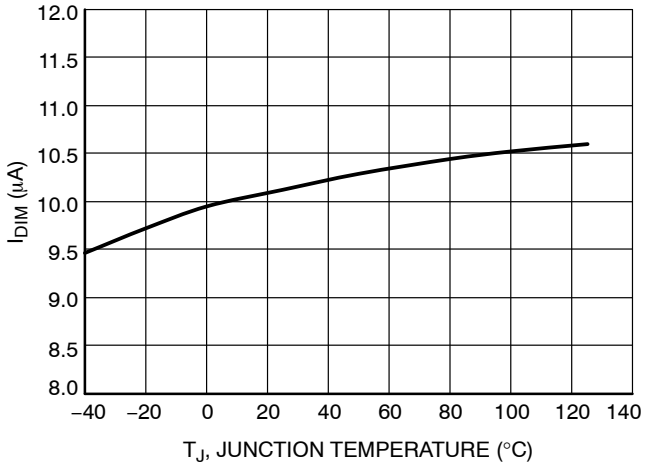


Figure 8. I_{DIM} vs. Temperature

APPLICATION INFORMATION

General

NCL30170 provides accurate LED current regulation with good PF and THD in ON Semiconductor's proprietary auto−commutation topology. The number of LED current regulation channels is flexibly selected with single controller. By selecting different values of external resistor and capacitor at DIM pin, either analog dimming or phase−cut dimming is easily implemented. Self−biasing HV supply shortens startup time with no external components and standby power consumption is minimized by reducing the operating current.

ON Semiconductor's Auto Commutation Topology

By adding cost effective HV diode between series switch connection, auto commutation in each LED channels is easily implemented in ON Semiconductor's proprietary topology. User can choose the number of LED channels based on the trade−off of system BOM and efficiency.

Power Factor Correction

Different from stepped input current in conventional parallel topology, NCL30170 in new parallel topology provides excellent sinusoidal input current shape with 0.99 PF and less than 10% THD.

Constant Current Regulation

Averaged input current is precisely regulated by closed loop control which minimizes CC tolerance in mains line variation.

Analog Dimming

NCL30170 features wide analog dimming down to 5%. The dimming curve is linear and IC to IC tolerance is small by high resolution trimming in max and min VDIM conditions.

Low Standby Power

When DIM pin voltage is close to 0 V, standby mode is entered and most of the internal biasing blocks are turned off to minimize standby power. Also, VDD regulation voltage is dropped from 20 V to 10 V and internal HV supply headroom loss will be almost zero if there is external supply voltage (around 15 V) connection through diode to VDD pin.

Phase−cut Dimming

As phase angle is reduced, input current is smoothly changed to flat shape from sinusoidal shape. In the low phase angle range, the flattened input current is maintained higher than TRIAC holding current. When input voltage is less than first LED channel voltage and CS voltage is close to 0 V, BLD pin controls external bleeding MOSFET so that input voltage softly reaches to 0 V and maintains close to 0 V during phase−cut condition. The input current shape and bleeding current control performs high dimmer compatibility.

High Voltage Startup

Internal HV startup fastens startup time less than 0.2 sec with no external components.

Input Over Voltage Protection

When VIN pin voltage is higher than 4 V, OUT pin voltage is pulled down and external linear regulator switches are protected from thermal stress by large headroom loss.

Thermal Shut Down

Protection is triggered when the internal junction temperature reaches to 150°C and normal startup begins once the temperature comes down to 120°C.

Sensing Resistor Short Protection

Short circuit of a sensing resistor makes severe over current at LED loads by losing close loop regulation. At startup, CS pin short is monitored by sourcing large current into external sensing resistor and protection is triggered if CS pin voltage is lower than SRSP threshold voltage.

Direct AC Driver Topology

NCL30170 controls multiple LED channels in new Direct AC Drive parallel topology. In the configuration, HV blocking diodes are connected between SW(n) source and SW(n+1) drain. As input voltage increases, the HV diodes are turned off one by one in auto commutation of the ambient switches. Therefore, one main amplifier controls all the channel current with one reference. The amplifier CS shaping reference, $V_{CS(SHA-REF)}$, is sinusoidal so that the input current is optimally sinusoidal with 0.99 PF and less than 10% THD compared to the conventional parallel topology which hardly meets THD in class C due to the stepped input current. 24 V zener diodes are added at gate to source node of each switch except for the last channel switch so that gate to source voltage is maintained under maximum voltage rating specified in the external switch datasheet.

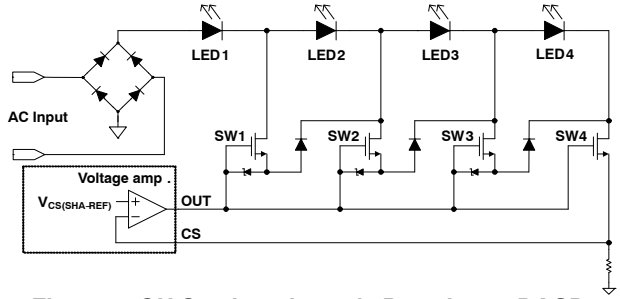


Figure 9. ON Semiconductor's Proprietary DACD Topology

Current Regulation and Power Factor Correction

An LED current is constantly regulated in the closed feedback loop. The LED current is detected through CS pin and CS voltage is compared with $V_{CS(AVG-REF)}$ reference by internal OTA which generates FB voltage in a narrow bandwidth due to an external large compensation capacitor, C_{FB}. In the closed loop, averaged CS voltage is accurately regulated same as $V_{CS(AVG-REF)}$ thanks to a minimized input voltage offset of OTA which is obtained by high resolution trimming done in mass production.

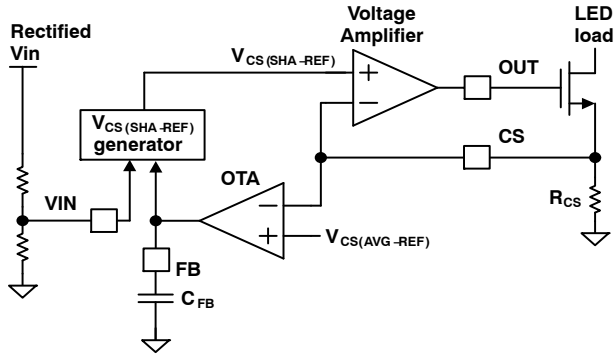


Figure 10. LED Current Regulation

An input current in the driver flows through CS sensing resistor, R_{CS}. Therefore, sinusoidal CS voltage shape in a half line period makes sinusoidal input current with ideal power factor correction. In order to obtain the excellent PF and THD, CS voltage shape is controlled by a voltage amplifier and the voltage amplifier reference, $V_{CS(SHA-REF)}$, is set by VIN and FB signals. VIN voltage comes from a resistive divider detecting a rectified Vin. $V_{CS(SHA-REF)}$ generator outputs $V_{CS(SHA-REF)}$ which is a sum of VIN voltage and a voltage offset controlled by the FB voltage. As line voltage increases, FB voltage is reduced to keep the same CS average voltage by OTA and $V_{CS(SHA-REF)}$ voltage offset is reduced accordingly.

Mode Detection

NCL30170 provides two dimming modes, ADIM (Analog Dimming Mode) and PCDIM (Phase−Cut Dimming Mode). The dimming mode is set before current regulation starts and NCL30170 operates differently in each dimming mode for the optimized dimming control.

BLD voltage is pulled up to VDD during UVLO state and pulled down for 80 us once VDD is higher than VDD.ON threshold. After 80 us $t_{BLD(RST)}$, BLD pin is pulled up by internal 110 kΩ R_{BLD} for 5 us $t_{BLD(PCDIM)}$. If BLD voltage is less than 3.25 V $V_{BLD(PCDIM)}$ threshold in the end of $t_{BLD(PCDIM)}$ by a large capacitor over 500 pF in an external bleeding circuit for PCDIM, dimming mode is set by PCDIM. If not, operation begins in ADIM mode. In order to set ADIM mode, BLD pin is open or connected to a filtering capacitor less than 50 pF.

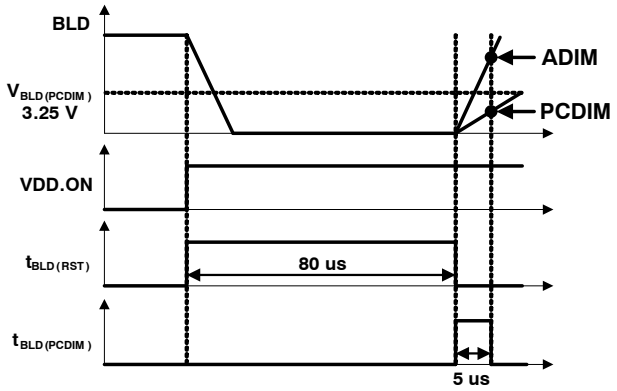


Figure 11. Mode Detection

Analog Dimming

Analog dimming is controlled by DC DIM voltage supplied from external dimming control signal. For a resistor controlled analog dimming, a variable resistor is connected to DIM pin in which 10 uA DIM internal current source and the variable resistor sets the DIM voltage.

As DIM voltage is reduced, $V_{CS(AVG-REF)}$ is reduced accordingly. As $V_{CS(AVG-REF)}$ decreases, FB voltage is also reduced and $V_{CS(SHA-REF)}$ has more negative offset voltage from VIN pin voltage.

When dimming signal is generated by an MCU, maximum dimming voltage is dependent on Vcc (3.3 V or 1.6 V) of the selected MCU. Therefore, two versions of NCL30170 are provided as shown in Figure 12. In A version, DIM range is up to 3 V and standby is enabled when

DIM voltage is lower than 0.2/0.3 V. B version provides dimming range in 0 ~ 1.5 V DIM voltage with 0.1/0.2 V standby threshold voltage, $V_{DIM(SB)}$. In both options, $V_{CS(AVG-REF)}$ is in between 50 mV and 1.5 V so that min LED brightness is less than 5% of maximum light output.

When DIM voltage is lower than $V_{DIM(SB)}$ for 10 ms $t_{SB(DELAY)}$, standby mode is entered and IC operating current drops less than 300 μA.

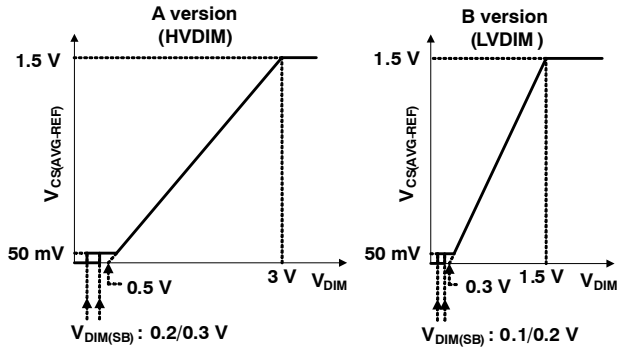


Figure 12. Analog Dimming Curve

Phase−Cut Dimming

In PCDIM mode, DIM current source is enabled and disabled by VIN.TH signal which is set by hysteretic comparator detecting VIN pin voltage. A time constant of external R_{DIM} and C_{DIM} is around 100 ms so that DIM voltage is almost constant over a half line period. Therefore, DIM voltage level is proportional to the phase angle set by the phase−cut dimmer.

When VDIM is higher than 3 V, $V_{CS(AVG-REF)}$ is constantly set to 1.5 V and constant light output is obtained in the VDIM range. Also, $V_{CS(SHA-REF)}$ is set to sinusoidal shape dominantly determined by VIN voltage for high PF. As VDIM decreases lower than 3 V, light output is reduced and $V_{CS(SHA-REF)}$ gradually changes from sinusoidal shape to flat shape to perform wide phase−cut dimming range and maintain TRIAC holding current by ON Semiconductor's proprietary active PCDIM control.

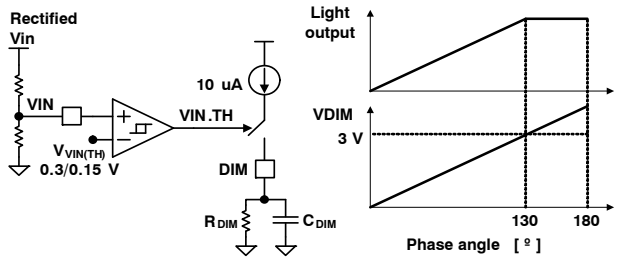


Figure 13. PCDIM Operation

BLD pin drives external bleeding MOSFET to stabilize phase−cut dimmer during TRIAC turn−off time. At input voltage leading edge, inrush current could come through LED current regulation path and damage LED loads and external regulation switches. Therefore, voltage amplifier output is pulled down during the leading edge and softly rises after several tens of usec to normally regulate LED current.

VDD Supply

NCL30170 has internal HV JFET switch to supply VDD current for fast startup and self biasing with no external VDD supply circuitry. Once VDD reaches to 16 V, VDD.ON flag is high and internal operation begins and VDD is regulated at 20 V. After VDD drops lower than 8 V, all operating blocks are shutdown. Blocking diode, D_{HV}, is connected to HV pin to protect reverse current when HV voltage is lower than VDD voltage.

Once SB (Stand By) flag signal is high as DIM pin voltage is lower than $V_{DIM(SB)}$, IC minimizes operating current less than 300 μA by disabling most of the functional blocks.

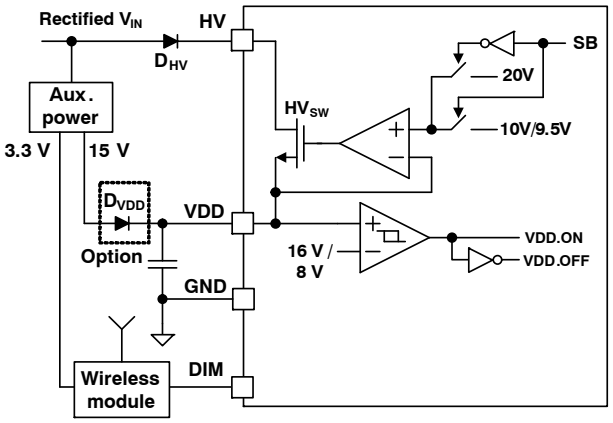


Figure 14. VDD Supply

In standby mode, VDD regulation voltage drops from 20 V down to 10 V/9.5 V by a hysteretic regulation. In wireless smart dimming application, auxiliary power supply is generally added to provide wireless module operating current. If aux. power could provide another output voltage around 15 V, this voltage can be utilized to supply NCL30170 VDD current through a diode (D_{VDD} in Figure 14) during standby condition in which 300 μA IC standby current is provided from efficient aux. power output, not internal HV regulator.

Protection

NCL30170 provides robust protections such as input over voltage, sensing resistor short and over temperature protections for system reliability.

When input voltage increases out of system input spec, external regulation switches take large amount of headroom loss and those switches can end up with severe damage. In order to protect the input over voltage condition, OUT and FB are pulled down when VIN voltage is higher than 4 V $V_{VIN(OVP)}$. This protection is disabled at PCDIM mode to prevent abnormal triggering caused by a leading edge input voltage spike.

When sensing resistor is short circuited, voltage amplifier is out of regulation and OUT pin voltage is pulled up with high power consumption in the external regulation switches. So, at the beginning of $t_{BLD(RST)}$, 30 mA I_{SRSP} flows into the external CS sensing resistor and SRSP protection is triggered if CS voltage is not higher than 60 mV V_{SRSP} for

5 μs. Once sensing resistor short protection is triggered, internal timer counts 40 ms and detects CS voltage again with I_{SRSP} and startup begins if CS voltage is higher than V_{SRSP} threshold.

NCL30170 has thermal shutdown protection by detecting internal junction temperature. When the temperature is over 160°C, protection is triggered and VDD is regulated at 20 V. If the junction temperature drops lower than 130°C, startup sequence with mode detection normally begins.

DESIGN GUIDANCE

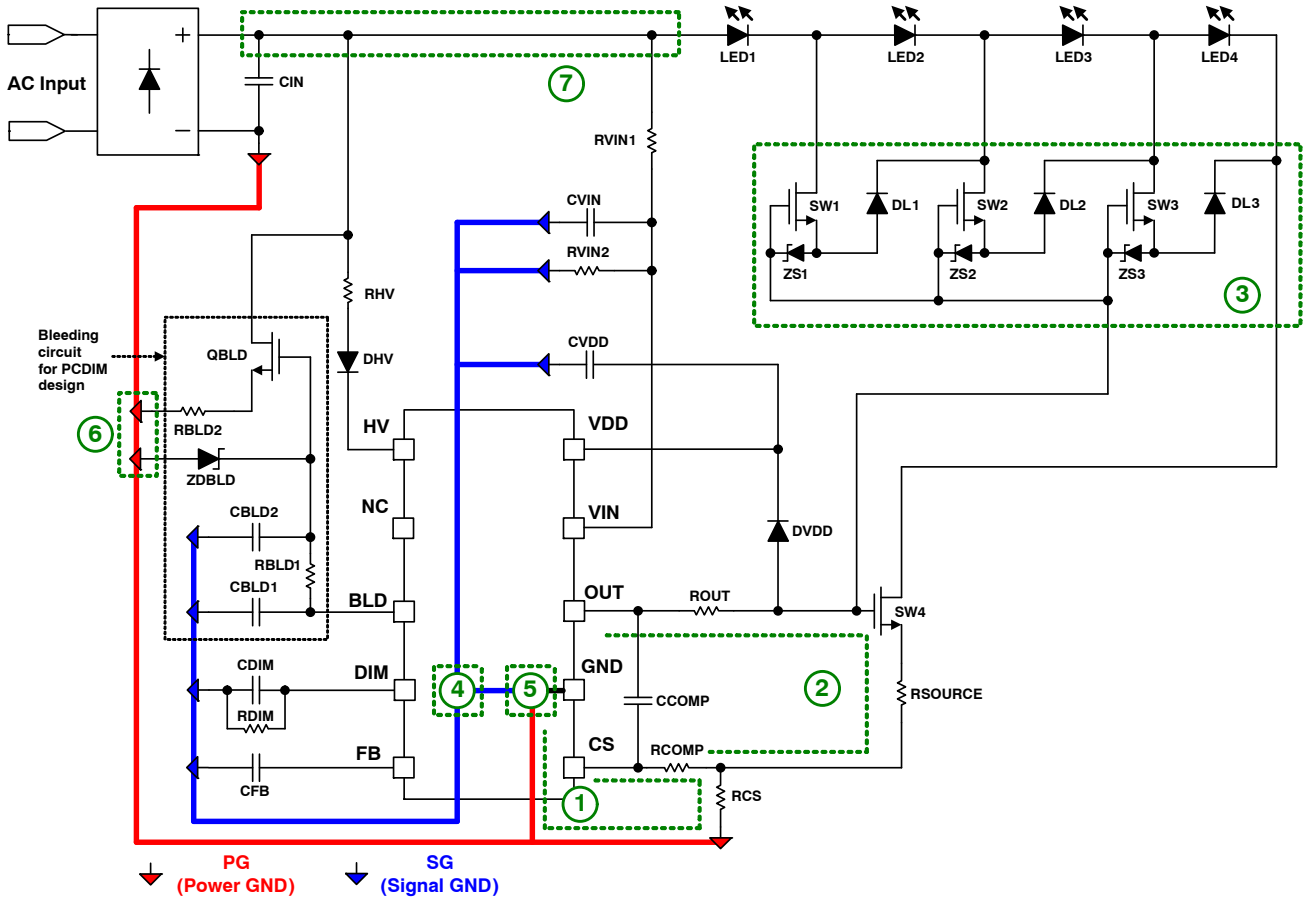


Figure 15. System Layout

Noise Immune Layout Guidance

1. CS – RCS – GND distance should be short.
2. OUT – SW4 (Switch in the last channel) – CS distance should be short.
3. It would be better to have SW1 ~ 3 and DL1 ~ 3 close to SW4. But, those switches shouldn't be very close due to thermal dissipation.
4. GND of control circuit (CBLD, CDIM, RDIM, CFB, CVIN, RVIN and CVDD) is closely connected near IC GND pin.
5. SG and PG are connected near IC GND pin.
6. RBLD2 and ZDBLD are connected to PG.
7. RVIN1 is connected to rectified input voltage node behind CIN, not between the bridge diode and CIN.

EMI Improvement

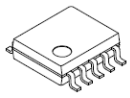
1. RCOMP and CCOMP can be optionally added to reduce regulation loop speed.
2. RSOURCE between SW4 and RCS can be optionally added to reduce input current glitch near input voltage zero cross.

ORDERING INFORMATION

Device	Package	Shipping
NCL30170ADR2G	10 Lead SOIC, JDEC MS−012, 150” Narrow Body	Tape and Reel
NCL30170BDR2G	10 Lead SOIC, JDEC MS−012, 150” Narrow Body	Tape and Reel

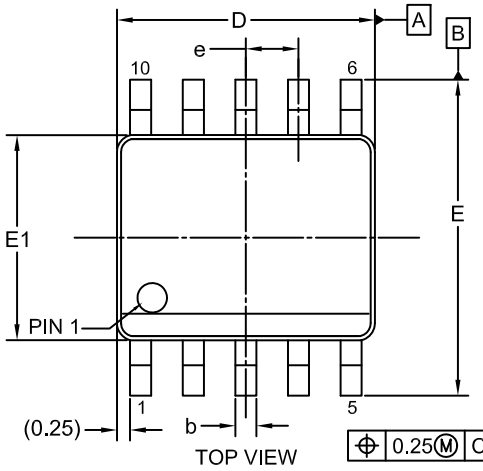
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

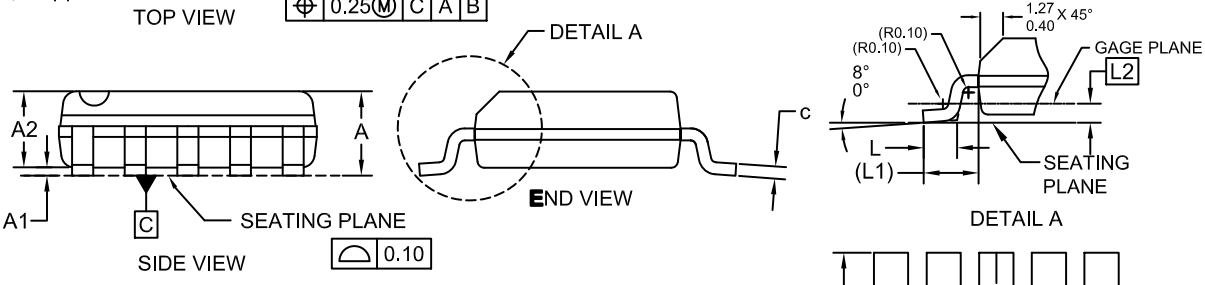


SOIC10, 4.9x6.0, 1.0P
CASE 751EE
ISSUE A

DATE 28 MAY 2019



DIM	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.50
b	0.30	0.40	0.45
c	0.10	0.20	0.25
D	4.80	4.90	5.00
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.00 BSC		
L	0.40	0.65	1.27
L1	1.04 Reference only		
L2	0.36 BSC		

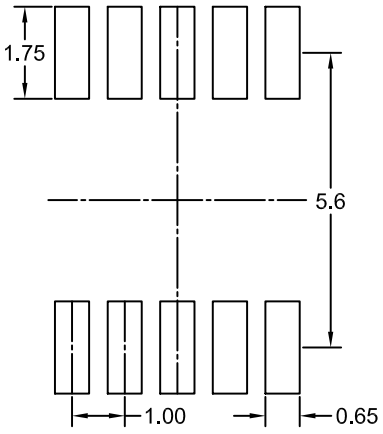


NOTES:
A. THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MS-012.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
E. LAND PATTERN STANDARD : SOIC127P600X175.10M

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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