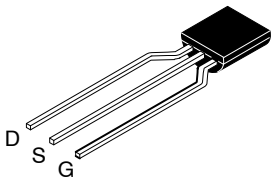
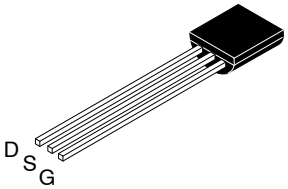
N-Channel Switch

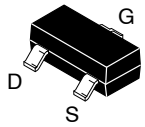
J111, J112, J113, MMBFJ111, MMBFJ112, MMBFJ113



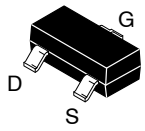
TO−92 3 4.83x4.76 LEADFORMED
CASE 135AR



TO−92 3 4.825x4.76
CASE 135AN



SOT−23 (TO−236)
CASE 318−08



SOT−23
CASE 318BM

Features

- This Device is Designed for Low Level Analog Switching, Sample and Hold Circuits and Chopper Stabilized Amplifiers
- Sourced from Process 51
- Source & Drain are Interchangeable
- These are Pb−Free Devices

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted) (Note 1, 2)

Symbol	Parameter	Value	Unit
V_{DG}	Drain−Gate Voltage	35	V
V_{GS}	Gate−Source Voltage	−35	V
I_{GF}	Forward Gate Current	50	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

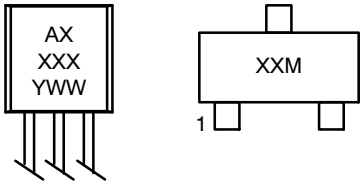
1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady−state limits. ON Semiconductor should be consulted on applications involving pulsed or low−duty−cycle operations.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Max		Unit
		J111 / J112 / J113 (Note 3)	**MMBFJ111 / MMBFJ112 / MMBFJ113** (Note 4)	
P_D	Total Device Dissipation	625	350	mW
	Derate Above 25°C	5.0	2.8	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	125	–	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	200	357	°C/W

3. PCB size: FR−4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.
4. Device mounted on FR−4 PCB 36 mm x 18 mm x 1.5 mm; mounting pad for the collector lead minimum 6 cm^2.

MARKING DIAGRAMS



XXXX, XX = Specific Device Code
A = Assembly Plant Code
Y = Year
WW = Work Week
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Max	Unit
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate−Source Breakdown Voltage	I_G = −1.0 μA, V_{DS} = 0		−35	–	V
I_{GSS}	Gate Reverse Current	V_{GS} = −15 V, V_{DS} = 0		–	−1.0	nA
$V_{GS}(off)$	Gate−Source Cut−Off Voltage	V_{DS} = 5 V, I_D = 1.0 μA	*111*	−3.0	−10.0	V
			112	−1.0	−5.0	
			113	−0.5	−3.0	
$I_D(off)$	Drain Cutoff Leakage Current	V_{DS} = 5.0 V, V_{GS} = −10 V		–	1.0	nA
ON CHARACTERISTICS						
I_{DSS}	Zero−Gate Voltage Drain Current (Note 5)	V_{DS} = 15 V, V_{GS} = 0	*111*	20	–	mA
			112	5.0	–	
			113	2.0	–	
$r_{DS}(on)$	Drain−Source On Resistance	$V_{DS} \leq$ 0.1 V, V_{GS} = 0	*111*	–	30	Ω
			112	–	50	
			113	–	100	
SMALL SIGNAL CHARACTERISTICS						
$C_{dg}(on)$ $C_{sg}(on)$	Drain−Gate &Source−Gate On Capacitance	V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz		–	28	pF
$C_{dg}(off)$	Drain−Gate Off Capacitance	V_{DS} = 0, V_{GS} = −10 V, f = 1.0 MHz		–	5.0	pF
$C_{sg}(off)$	Source−Gate Off Capacitance	V_{DS} = 0, V_{GS} = −10 V, f = 1.0 MHz		–	5.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse test: pulse width ≤300 μs, duty cycle ≤2%.

TYPICAL PERFORMANCE CHARACTERISTICS

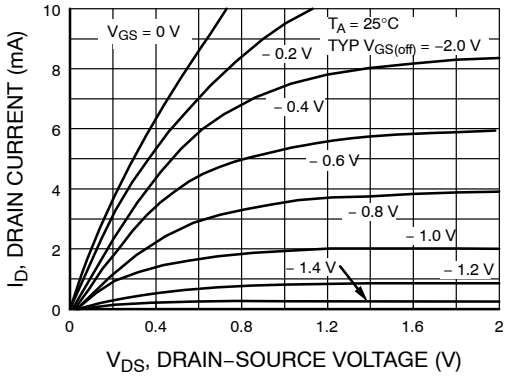


Figure 1. Common Drain−Source

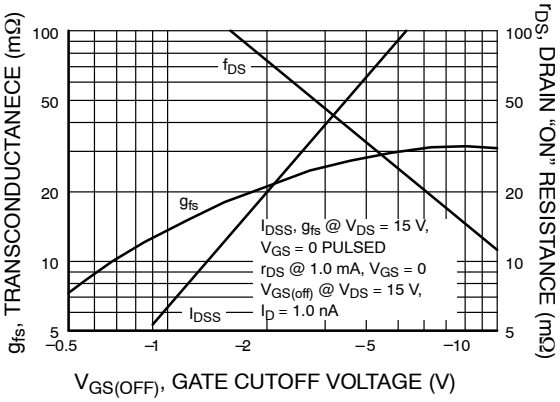


Figure 2. Parameter Interactions

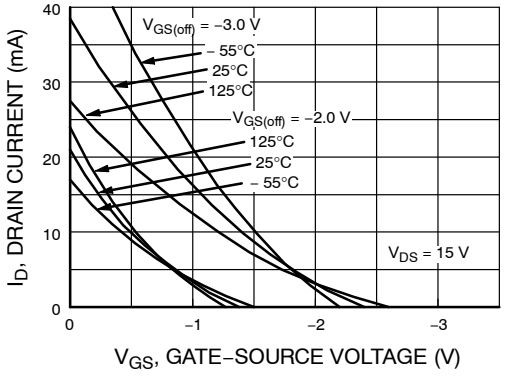


Figure 3. Transfer Characteristics

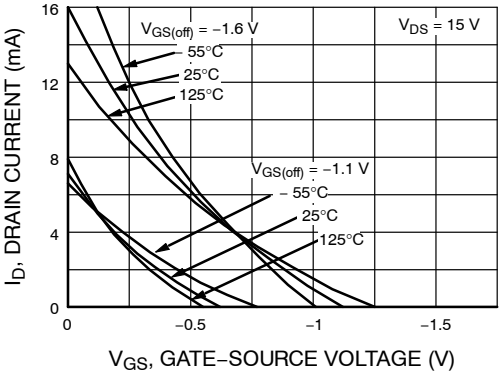


Figure 4. Transfer Characteristics

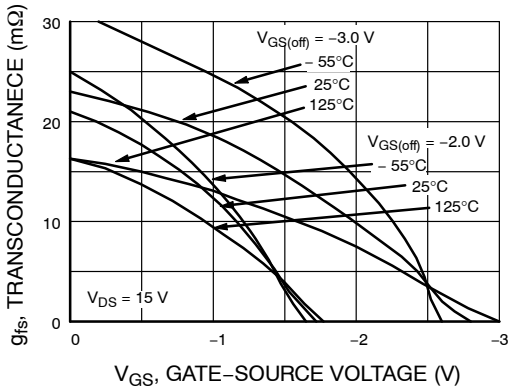


Figure 5. Transfer Characteristics

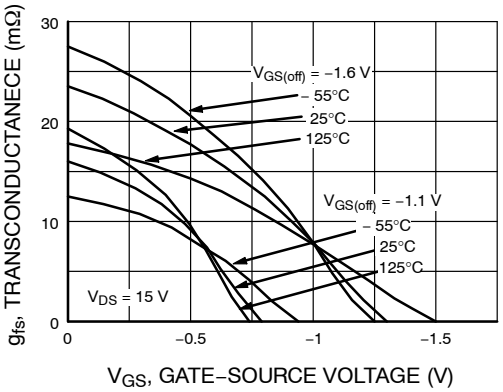


Figure 6. Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

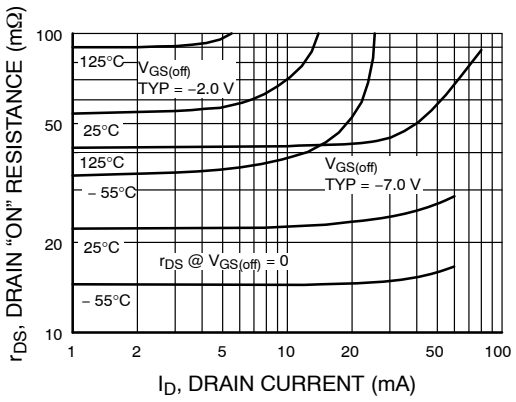


Figure 7. On Resistance vs. Drain Current

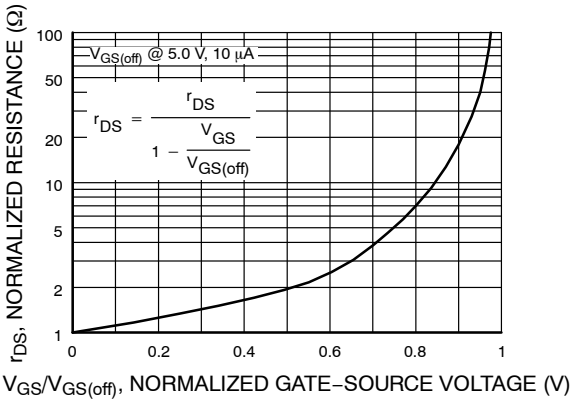


Figure 8. Normalized Drain Resistance vs. Bias Voltage

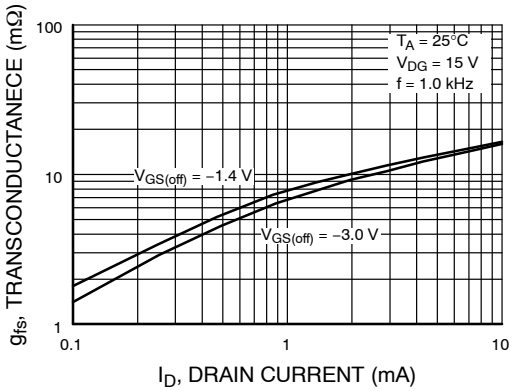


Figure 9. Transconductance vs. Drain Current

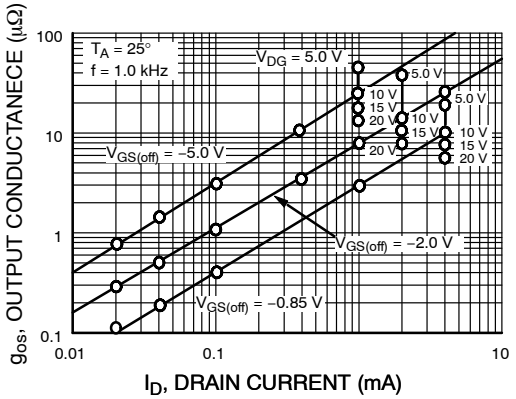


Figure 10. Output Conductance vs. Drain Current

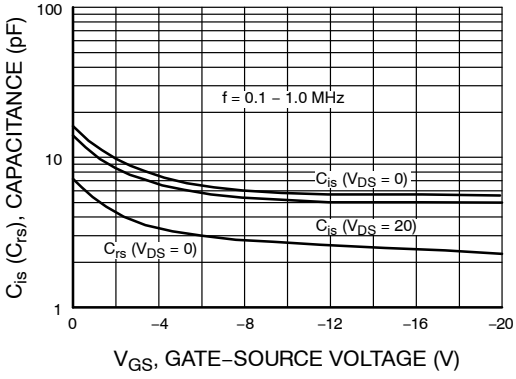


Figure 11. Capacitance vs. Voltage

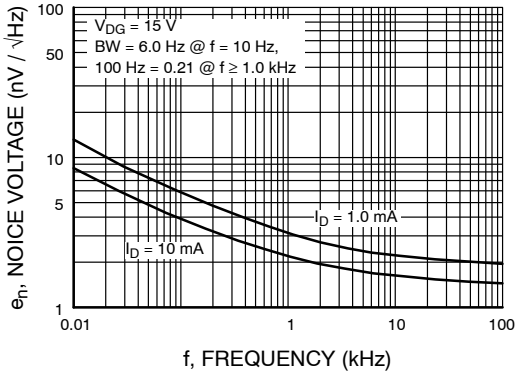


Figure 12. Noise Voltage vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

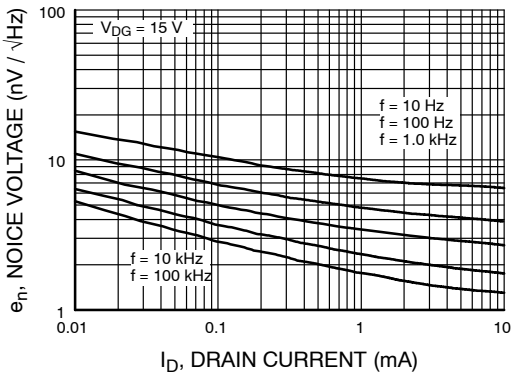


Figure 13. Noise Voltage vs. Current

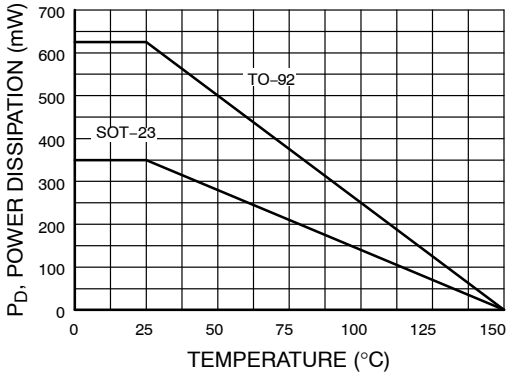


Figure 14. Power Dissipation vs. Ambient Temperature

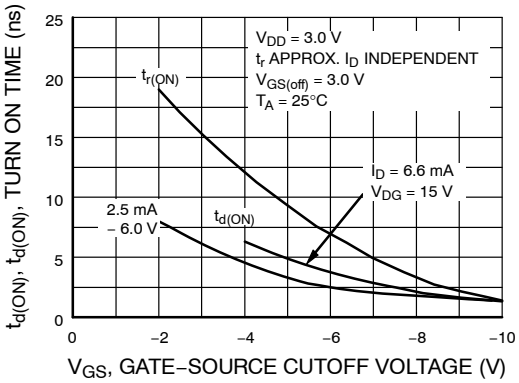


Figure 15. Switching Turn−On Time vs. Gate−Source Voltage

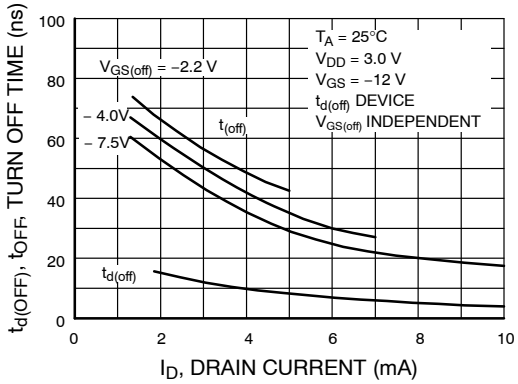


Figure 16. Switching Turn−Off Time vs. Drain Current

ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping†
J111	AJ 111 YWW	TO−92 3L (Pb−Free)	10000 Units / Bulk
J111−D26Z	AJ 111 YWW	TO−92 3L (Pb−Free)	2000 / Tape & Reel
J111−D74Z	AJ 111 YWW	TO−92 3L (Pb−Free)	2000 / Ammo
J112	AJ 112 YWW	TO−92 3L (Pb−Free)	10000 Units / Bulk
J112−D26Z	AJ 112 YWW	TO−92 3L (Pb−Free)	2000 / Tape & Reel
J112−D27Z	AJ 112 YWW	TO−92 3L (Pb−Free)	2000 / Tape & Reel
J112−D74Z	AJ 112 YWW	TO−92 3L (Pb−Free)	2000 / Ammo
J113	AJ 113 YWW	TO−92 3L (Pb−Free)	10000 Units / Bulk
J113−D74Z	AJ 113 YWW	TO−92 3L (Pb−Free)	2000 / Ammo
MMBFJ111	6P	SOT−23 3L (Pb−Free)	3000 / Tape & Reel
MMBFJ112	6R	SOT−23 3L (Pb−Free)	3000 / Tape & Reel
MMBFJ113	6S	SOT−23 3L (Pb−Free)	3000 / Tape & Reel

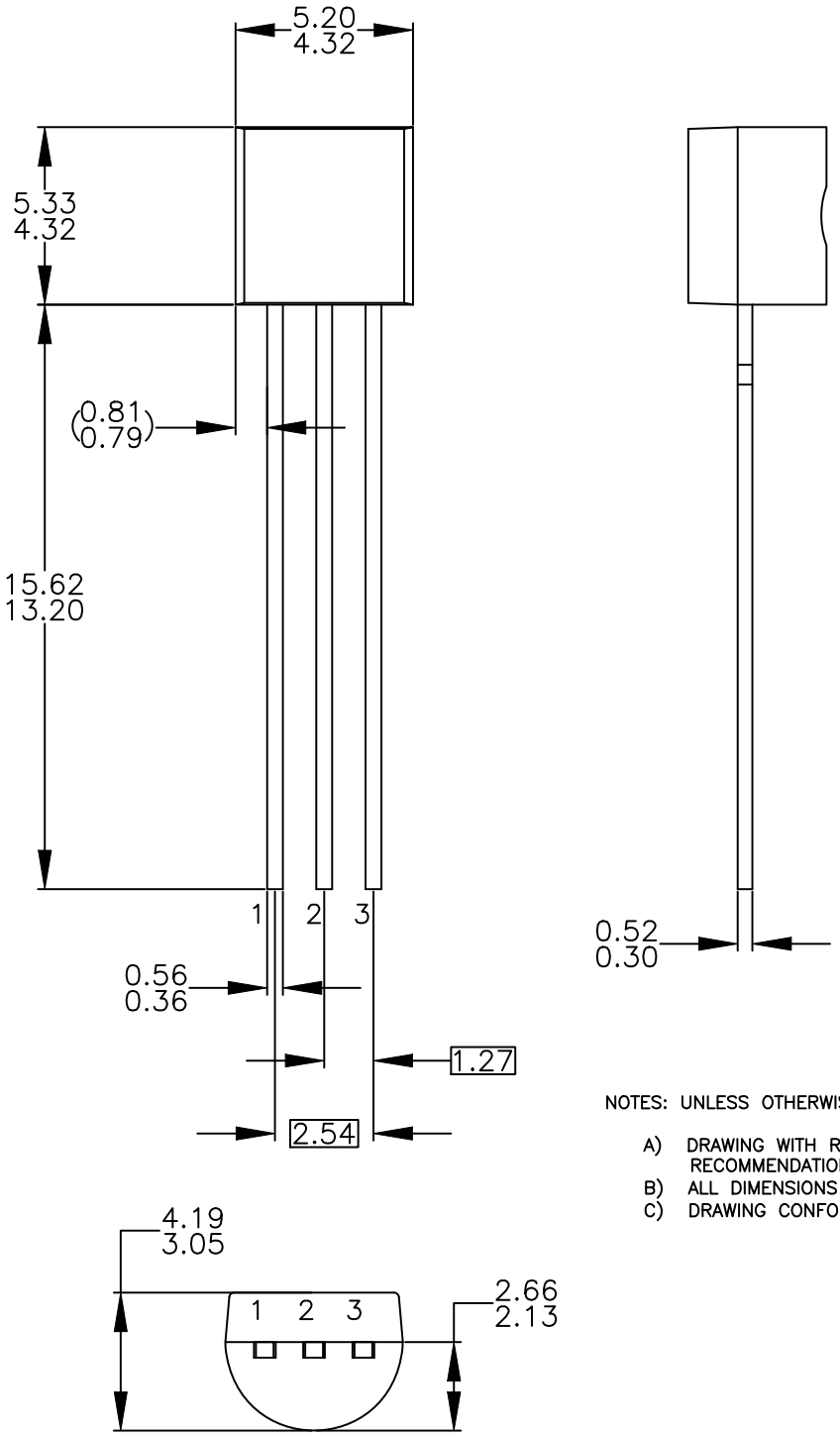
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−92 3 4.825x4.76
CASE 135AN
ISSUE O

DATE 31 JUL 2016



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO−92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M−2009.

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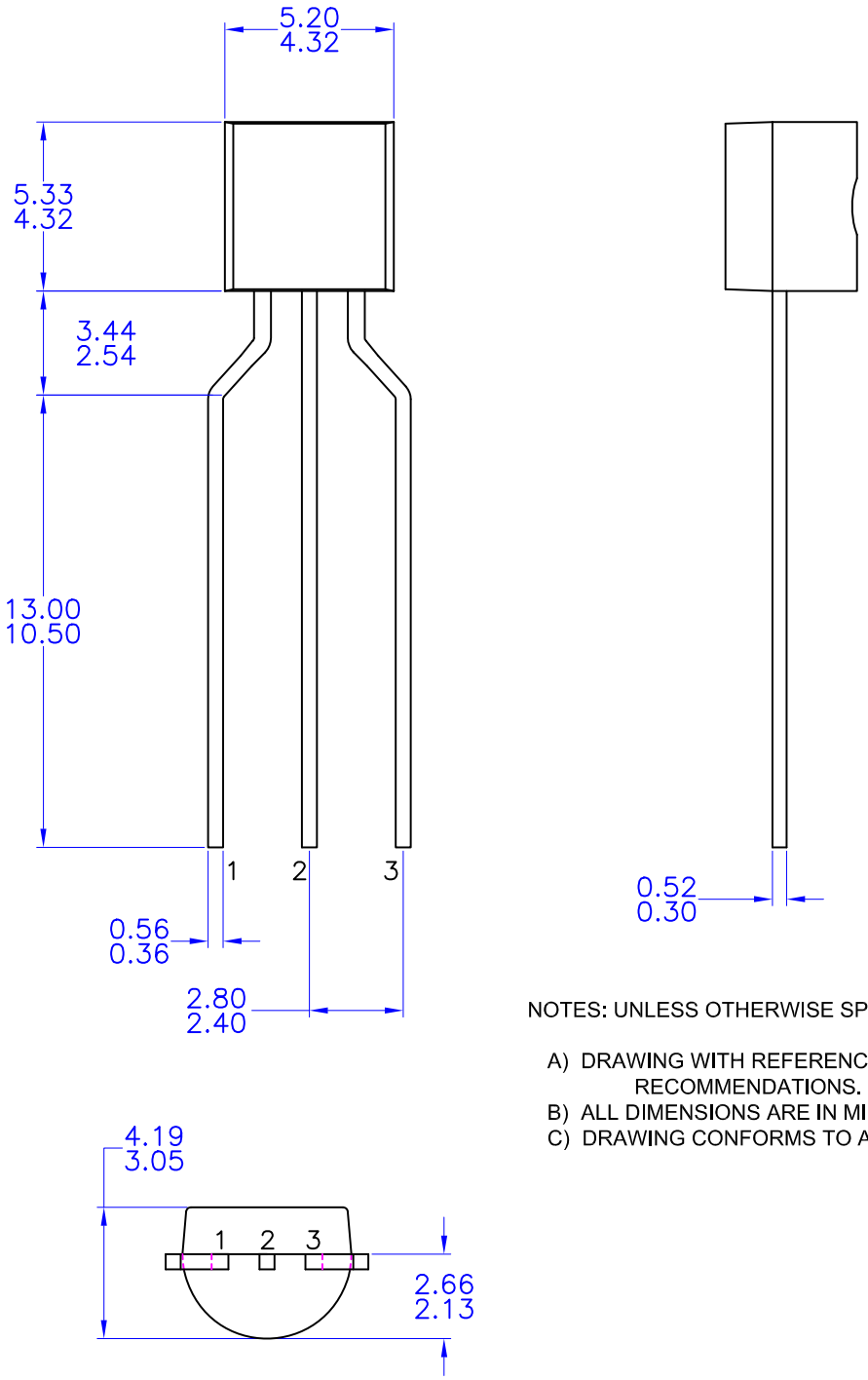
DESCRIPTION:	**TO−92 3 4.825X4.76**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−92 3 4.83x4.76 LEADFORMED
CASE 135AR
ISSUE O

DATE 30 SEP 2016



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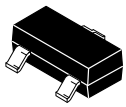
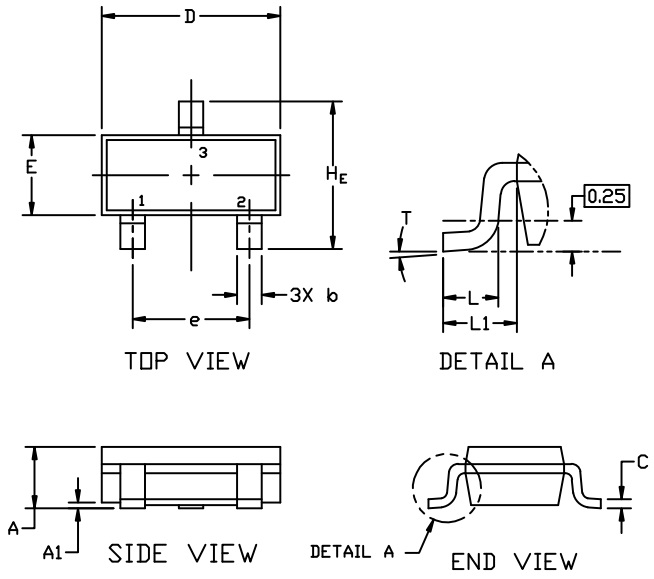
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

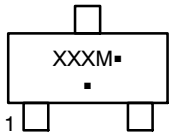


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

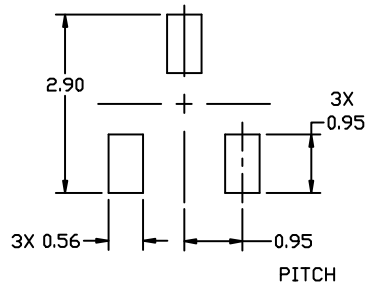
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales