

SET-TOP CLOCK SOURCE

MK2761A

Description

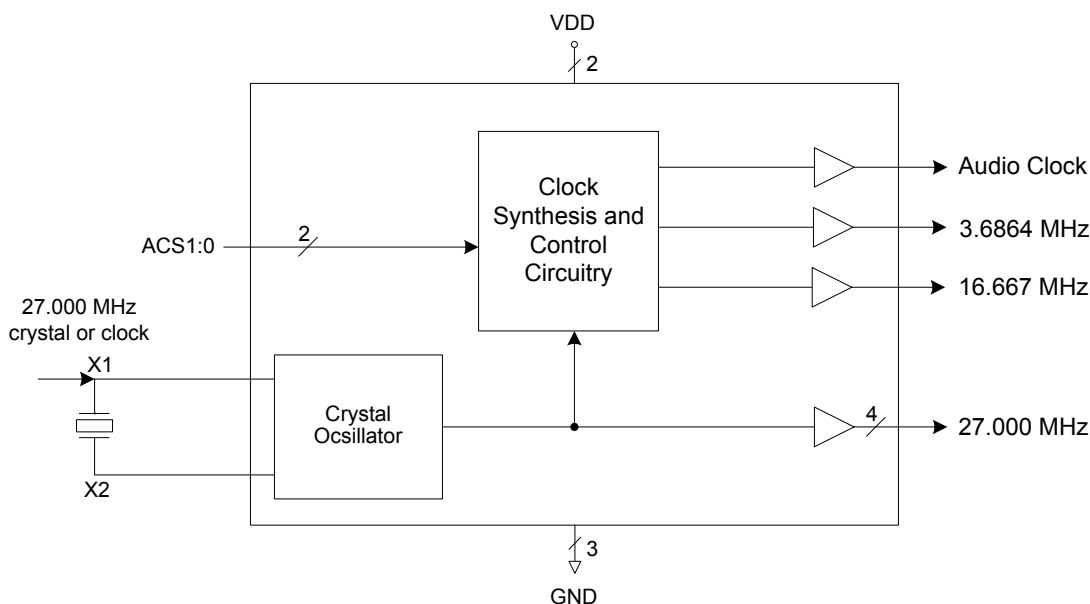
The MK2761A is a low-cost, low-jitter, high-performance clock synthesizer for set-top box applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 27 MHz crystal or clock input to produce multiple output clocks including the processor clock, the UART clock, a selectable audio clock, and four low skew copies of the 27 MHz. The audio clocks are frequency-locked to the 27 MHz using our patented zero ppm error techniques. This allows audio and video to track exactly, thereby eliminating the need for large buffer memory.

IDT manufactures a large variety of Set-top Box and multimedia clock synthesizers for all applications. Consult IDT to eliminate crystals and oscillators from your board.

Features

- Packaged in a 16-pin narrow (150 mil) SOIC
- Pb (lead) free package
- Selectable audio sampling frequencies support 32, 44.1, and 48 kHz in most DACs
- 27 MHz crystal or clock input
- Processor frequency of 16.67 MHz
- Fixed clocks of 27 and 3.6864 MHz
- Zero ppm in audio clocks exactly track video frequency
- 25 mA output drive capability at TTL levels
- Advanced, low-power, sub-micron CMOS process
- Operating voltage of 5.0 V $\pm 10\%$

Block Diagram



Pin Assignment

| | | | | | |
|-----------|--------------------------|---|----|--------------------------|--------|
| ACS1 | <input type="checkbox"/> | 1 | 16 | <input type="checkbox"/> | ACS0 |
| X2 | <input type="checkbox"/> | 2 | 15 | <input type="checkbox"/> | 27 MHz |
| X1/ICLK | <input type="checkbox"/> | 3 | 14 | <input type="checkbox"/> | 27 MHz |
| VDD | <input type="checkbox"/> | 4 | 13 | <input type="checkbox"/> | VDD |
| GND | <input type="checkbox"/> | 5 | 12 | <input type="checkbox"/> | GND |
| 16.67 MHz | <input type="checkbox"/> | 6 | 11 | <input type="checkbox"/> | 27 MHz |
| 3.68 MHz | <input type="checkbox"/> | 7 | 10 | <input type="checkbox"/> | 27 MHz |
| ACLK | <input type="checkbox"/> | 8 | 9 | <input type="checkbox"/> | GND |

16-pin (150 mil) SOIC

Audio Clock (MHz) Decoding Table

| ACS1 | ACS0 | ACLK |
|------|------|---------|
| 0 | 0 | 8.192 |
| 0 | 1 | 11.2896 |
| 1 | 0 | 12.288 |
| 1 | 1 | 5.6448 |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | ACS1 | Input | Audio clock Select 1. Selects ACLK on pin 8. See table above. |
| 2 | X2 | XO | Crystal connection. Connect to 27 MHz crystal. Leave unconnected for clock input. |
| 3 | X1/ICLK | XI | Crystal connection. Connect to 27 MHz crystal or to a 27 MHz input clock. |
| 4 | VDD | Power | Connect to +5 V. |
| 5 | GND | Power | Connect to ground. |
| 6 | 16.67M | Output | 16.667 MHz processor clock output. |
| 7 | 3.68M | Output | 3.6864 MHz clock output. |
| 8 | ACLK | Output | Audio clock output. Determined by status of ACS1, ACS0. See table above |
| 9 | GND | Power | Connect to ground. |
| 10 | 27M | Output | 27 MHz buffered reference clock output. Duty cycle matches input clock. |
| 11 | 27M | Output | 27 MHz buffered reference clock output. Duty cycle matches input clock. |
| 12 | GND | Power | Connect to ground. |
| 13 | VDD | Power | Connect to +5 V. |
| 14 | 27M | Output | 27 MHz buffered reference clock output. Duty cycle matches input clock. |
| 15 | 27M | Output | 27 MHz buffered reference clock output. Duty cycle matches input clock. |
| 16 | ACS0 | Input | Audio clock Select 0. Selects audio clock on pin 8. See table above. |

External Components

The MK2761A requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1μF should be connected between VDD and GND, as close to the MK2761A as possible. A series termination resistor of 33Ω may be used for each clock output. If a clock input is not used, the 27 MHz crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant, 50 ppm or better. Crystal capacitors should be connected from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation, where CL is the crystal load capacitance: Crystal caps (pF) = (CL-4) x 2. So, for a crystal with 16 pF load capacitance, the crystal caps should be 24 pF each.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2761A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +4.5 | | +5.5 | V |

DC Electrical Characteristics

VDD = 5.0 V \pm 10% (unless otherwise noted), Temp 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|-----------------|--------------------------|---------|-----------|------|-------|
| Operating Voltage | VDD | | 4.5 | | 5.5 | V |
| Input High Voltage | V _{IH} | X1/ICLK pin only | 3.5 | 2.5 | | V |
| Input Low Voltage | V _{IL} | X1/ICLK pin only | | 2.5 | 1.5 | V |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | | | 0.4 | V |
| Output High Voltage, CMOS level | V _{OH} | I _{OH} = -8 mA | VDD-0.4 | | | V |
| Operating Supply Current | IDD | No load, Note 1 | | 65 | | mA |
| Short Circuit Current | I _{OS} | Each output | | \pm 100 | | mA |
| Input Capacitance | C _{IN} | | | 7 | | pF |
| Frequency Error, ACLK | | | | | 0 | ppm |

Note 1: With ACLK clock at 12.28 MHz.

AC Electrical Characteristics

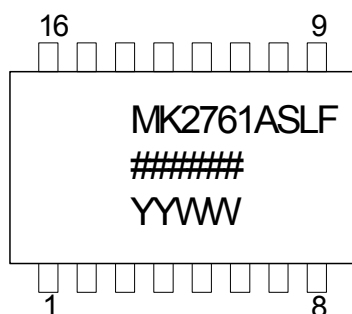
VDD = 5.0 V \pm 10% (unless otherwise noted), Temp 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------|-----------------------|------|-----------|------|-------|
| Input Frequency | | | | 27 | | MHz |
| Output Clock Rise Time | t _{OR} | 0.8 to 2.0 V | | | 1.5 | ns |
| Output Clock Fall Time | t _{OF} | 2.0 to 0.8 V | | | 1.5 | ns |
| Output Clock Duty Cycle | | At 1.4 V | 40 | | 60 | % |
| Absolute Jitter, short term | | Variation from mean | | \pm 250 | | ps |
| Skew of 27 MHz Outputs | | Rising edges at 1.4 V | -500 | 0 | 500 | ps |

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 120 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 115 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 105 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 58 | | °C/W |

Marking Diagram (MK2761ASLF)

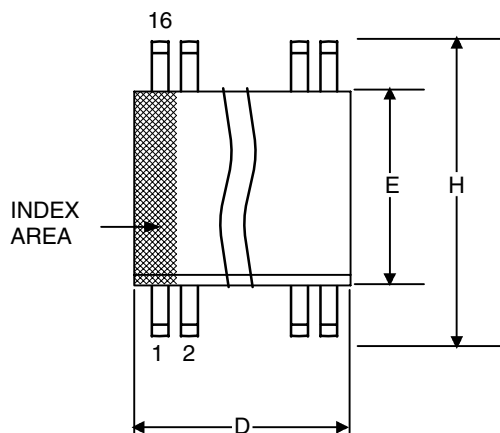


Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "LF" denotes Pb (lead) free package.
4. Bottom marking: (origin). Origin = country of origin if not USA.

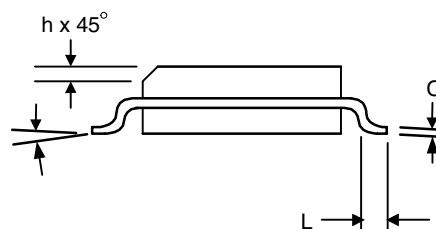
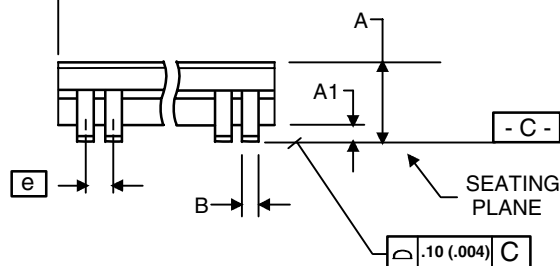
Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



| | Millimeters | | Inches* | |
|----------|-------------|-------|-------------|-------|
| Symbol | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | 9.80 | 10.00 | .3859 | .3937 |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|-------------|-------------|
| MK2761ASLF | see page 5 | Tubes | 16-pin SOIC | 0 to +70° C |
| MK2761ASLFTR | | Tape and Reel | 16-pin SOIC | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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