



## Pin Assignment

X1	□ 1	20	□ X2
VDD	□ 2	19	□ GND
VDD	□ 3	18	□ ISEL
VDD	□ 4	17	□ ICLK1
VIN	□ 5	16	□ ICLK2
GND	□ 6	15	□ SEL0
GND	□ 7	14	□ CLK
GND	□ 8	13	□ NC
CHGP	□ 9	12	□ SEL1
ISET	□ 10	11	□ SEL2

20 pin 300 mil SOIC

## Output Clock Selection Table

Input	SEL2	SEL1	SEL0	Output Clock (MHz)	Crystal Used (MHz)
8 kHz	0	0	0	1.544	24.704
8 kHz	0	0	1	2.048	24.576
8 kHz	0	1	0	16.384	16.384
8 kHz	0	1	1	17.664	17.664
8 kHz	M	0	0	18.528	18.528
8 kHz	M	0	1	20.00	20.00
8 kHz	M	1	0	25.00	25.00
8 kHz	M	1	1	25.92	25.92
8 kHz	1	0	0	19.44	19.44
8 kHz	1	0	1	20.48	20.48
8 kHz	1	1	0	24.704	24.704
8 kHz	1	1	1	24.576	24.576

Note: For SEL input pin programming:

0 = GND, 1 = VDD, M = Floating

## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	-	Crystal Input. Connect this pin to the specified crystal.
2	VDD	Power	Power Supply. Connect to +3.3V.
3	VDD	Power	Power Supply. Connect to +3.3V.
4	VDD	Power	Power Supply. Connect to +3.3V.
5	VIN	Input	VCXO Control Voltage Input. Connect this pin to CHGP pin and the external loop filter as shown in this data sheet.
6	GND	Power	Connect to ground
7	GND	Power	Connect to ground
8	GND	Power	Connect to ground
9	CHGP	Output	Charge Pump Output. Connect this pin to the external loop filter and to pin VIN.
10	ISET	-	Charge pump current setting node, connection for setting resistor.
11	SEL2	Input	Output Frequency Selection Pin 2. Determines output frequency as per table above. Internally biased to VDD/2.
12	SEL1	Input	Output Frequency Selection Pin 1. Determines output frequency as per table above. Internal pull-up.
13	NC	Input	No Internal Connection.
14	CLK	Output	Clock Output
15	SEL0	Input	Output Frequency Selection Pin 0. Determines output frequency as per table above. Internal pull-up.
16	ICLK2	Input	Input Clock Connection 2. Connect an input reference clock to this pin. If unused, connect to ground.
17	ICLK1	Input	Input Clock Connection 1. Connect an input reference clock to this pin. If unused, connect to ground.
18	ISEL	Input	Input Selection. Used to select which reference input clock is active. Low input level selects ICLK1, high input level selects ICLK2. Internal pull-up.
19	GND	Power	Connect to ground.
20	X2	-	Crystal Output. Connect this pin to the specified crystal.

## Functional Description

The MK2059-01 is a clock generator IC that generates an output clock directly from an internal VCXO circuit which works in conjunction with an external quartz crystal. The VCXO is controlled by an internal PLL (Phase Locked Loop) circuit, enabling the device to perform clock regeneration from an input reference clock. The MK2059-01 is configured to provide a MHz communications reference clock output from an 8kHz input clock. There are 12 selectable output frequencies. Please refer to the Output Clock Selection Table on Page 2.

Most typical PLL clock devices use an internal VCO (Voltage Controlled Oscillator) for output clock generation. By using a VCXO with an external crystal, the MK2059-01 is able to generate a low jitter, low phase-noise output clock within a low bandwidth PLL. This serves to provide input clock jitter attenuation and enables stable operation with a low frequency reference clock.

The VCXO circuit requires an external pullable crystal for operation. External loop filter components enable a PLL configuration with low loop bandwidth.

## Application Information

### Output Frequency Configuration

The MK2059-01 is configured to generate a set of output frequencies from an 8kHz input clock. Please refer to the Output Clock Selection Table on Page 2. Input bits SEL2:0 are set according to this table, as is the external crystal frequency. Please refer to the Quartz Crystal section on this page regarding external crystal requirements.

### Input Mux

The Input Mux serves to select between two alternate input reference clocks. Upon reselection of the input clock, clock glitches on the output clock will not be generated due to the “fly-wheel” effect of the VCXO (the quartz crystal is a high-Q tuned circuit). When the input clocks are not phase aligned, the phase of the output clock will change to reflect the phase of newly selected input at a controlled phase slope (rate of phase change) as influenced by the PLL loop characteristics.

## Quartz Crystal

It is important that the correct type of quartz crystal is used with the MK2059-01. Failure to do so may result in reduced frequency pullability range, inability of the loop to lock, or excessive output phase jitter.

The MK2059-01 operates by phase-locking the VCXO circuit to the input signal of the selected ICLK input. The VCXO consists of the external crystal and the integrated VCXO oscillator circuit. To achieve the best performance and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the PCB Layout Recommendations section must be followed.

The frequency of oscillation of a quartz crystal is determined by its cut and by the external load capacitance. The MK2059-01 incorporates variable load capacitors on-chip which “pull”, or change, the frequency of the crystal. The crystals specified for use with the MK2059-01 are designed to have zero frequency error when the total of on-chip + stray capacitance is 14pF. To achieve this, the layout should use short traces between the MK2059-01 and the crystal.

A complete description of the recommended crystal parameters is shown in application note MAN05.

A list of qualified crystal devices that meet these requirements can be found on the IDT web site.

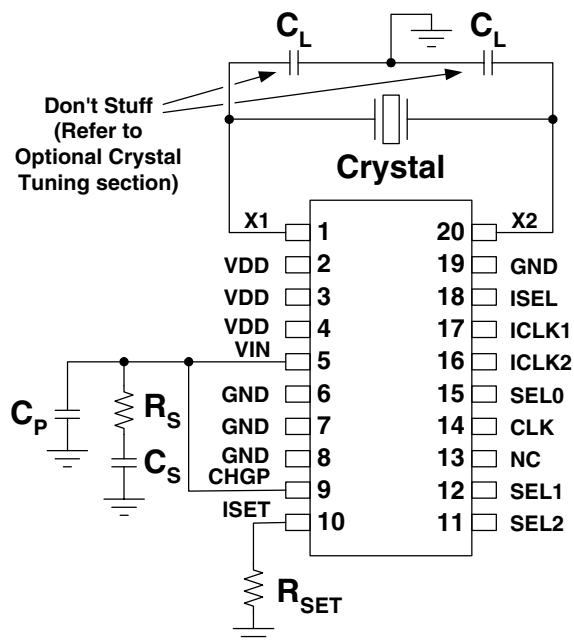
### PLL Loop Filter Components

All analog PLL circuits use a loop filter to establish operating stability. The MK2059-01 uses external loop filter components for the following reasons:

- 1) Larger loop filter capacitor values can be used, allowing a lower loop bandwidth. This enables the use of lower input clock reference frequencies and also input clock jitter attenuation capabilities. Larger loop filter capacitors also allow higher loop damping factors when less passband peaking is desired.
- 2) The loop filter values can be user selected to optimize loop response characteristics for a given application.

Referencing the External Component Schematic on this page, the external loop filter is made up of components  $R_S$ ,  $C_S$  and  $C_P$ .  $R_{SET}$  establishes PLL charge pump current and therefore influences loop filter characteristics. Tools for determining loop filter component values are on the IDT web site.

## External Component Schematic



## Recommended Loop Filter Values Vs. Output Frequency Range Selection

SEL2	SEL1	SEL0	Crystal Multiplier (N)	R <sub>SET</sub>	R <sub>S</sub>	C <sub>S</sub>	C <sub>P</sub>	Loop Bandwidth (-3dB point)	Damping Factor
0	0	0	3088	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	18 Hz	1.4
0	0	1	3072	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	19 Hz	1.4
0	1	0	2048	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	27 Hz	1.7
0	1	1	2208	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	26 Hz	1.7
M	0	0	2316	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	24 Hz	1.6
M	0	1	2500	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	22 Hz	1.6
M	1	0	3125	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	18 Hz	1.4
M	1	1	3240	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	17 Hz	1.4
1	0	0	2430	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	23 Hz	1.6
1	0	1	2560	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	22 Hz	1.6
1	1	0	3088	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	18 Hz	1.4
1	1	1	3072	120 kΩ	1.0 MΩ	0.1 μF	4.7 nF	19 Hz	1.4

Note: For SEL input pin programming: 0 = GND, 1 = VDD, M = Floating

A “normalized” PLL loop bandwidth may be calculated as follows:

$$NBW = \frac{R_S \times I_{CP} \times 575}{N}$$

The “normalized” bandwidth equation above does not take into account the effects of damping factor or the second pole. However, it does provide a useful approximation of filter performance.

The loop damping factor is calculated as follows:

$$\text{Damping Factor} = R_S \times \sqrt{\frac{625 \times I_{CP} \times C_S}{N}}$$

Where:

- $R_Z$  = Value of resistor in loop filter (Ohms)
- $I_{CP}$  = Charge pump current (amps)  
(refer to Charge Pump Current Table, below)
- $N$  = Crystal multiplier shown in the above table
- $C_1$  = Value of capacitor  $C_1$  in loop filter (Farads)

As a general rule, the following relationship should be maintained between components  $C_1$  and  $C_2$  in the loop filter:

$$C_P = \frac{C_S}{20}$$

### Charge Pump Current Table

$R_{SET}$	Charge Pump Current ( $I_{CP}$ )
1.4 M $\Omega$	10 $\mu$ A
680 k $\Omega$	20 $\mu$ A
540 k $\Omega$	25 $\mu$ A
120 k $\Omega$	100 $\mu$ A

Special considerations must be made in choosing loop components  $C_S$  and  $C_P$ . These recommendations can be found on the IDT web site.

### Series Termination Resistor

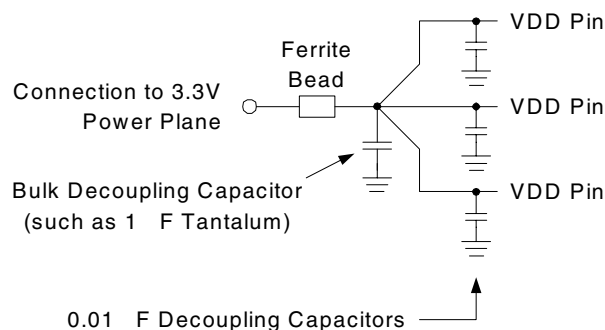
Clock output traces over one inch should use series termination. To series terminate a 50 $\Omega$  trace (a commonly used trace impedance), place a 33 $\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 $\Omega$ . (The optional series termination resistor is not shown in the External Component Schematic.)

### Decoupling Capacitors

As with any high performance mixed-signal IC, the MK2059-01 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01 $\mu$ F must be connected between each VDD and the PCB ground plane. To further guard against interfering system supply noise, the MK2059-01 should use one common connection to the PCB power plane as shown in the diagram on the next page. The ferrite bead and bulk capacitor help reduce lower frequency noise in the supply that can lead to output clock phase modulation.

### Recommended Power Supply Connection for Optimal Device Performance



## Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground, shown as  $C_L$  in the External Component Schematic. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no via's) between the crystal and device.

In most cases the load capacitors will not be required. They should not be stuffed on the prototype evaluation board as the indiscriminate use of these trim capacitors will typically cause more crystal centering error than their absence. If the need for the load capacitors is later determined, the values will fall within the 1-4 pF range. The need for, and value of, these trim capacitors can only be determined at prototype evaluation. Please refer to [application note MAN05](#) for the procedure to determine the capacitor values.

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please also refer to the Recommended PCB Layout drawing on Page 7.

1) Each 0.01  $\mu$ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No via's should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The loop filter components must also be placed close to the CHGP and VIN pins.  $C_P$  should be closest to the device. Coupling of noise from other system signal traces should be minimized by keeping traces short and away from active signal traces. Use of vias should be avoided.

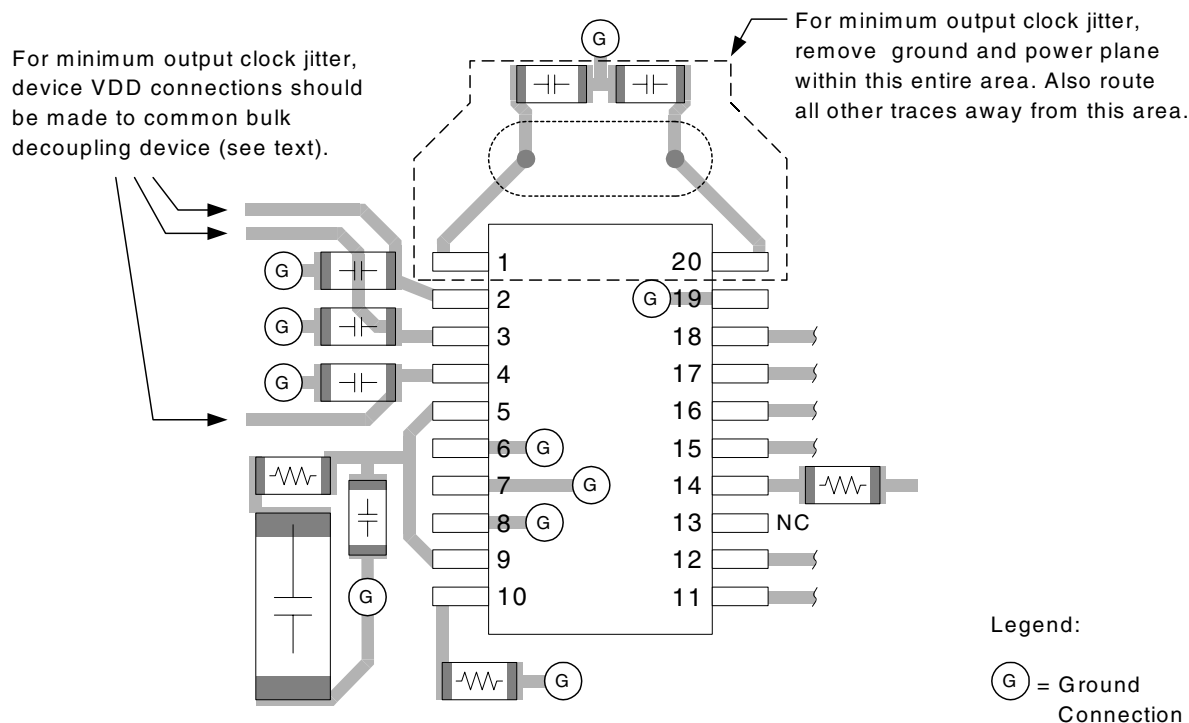
3) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

4) To minimize EMI the 33  $\Omega$  series termination resistor, if needed, should be placed close to the clock output.

5) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK2059-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

The IDT Applications Note MAN05 may also be referenced for additional suggestions on layout of the crystal section.

## Recommended PCB Layout



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2059-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	175° C
Soldering Temperature	260° C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

## DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V  $\pm$ 5%, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Supply Current	IDD	Clock outputs unloaded, VDD = 3.3V		10	15	mA
Input High Voltage, SEL2	V <sub>IH</sub>		VDD-0.5			V
Input Low Voltage, SEL2	V <sub>IL</sub>				0.5	V
Input High Voltage, ISEL, SEL1:0	V <sub>IH</sub>		2			V
Input Low Voltage, ISEL, SEL1:0	V <sub>IL</sub>				0.8	V
Input High Voltage, ICLK1, 2	V <sub>IH</sub>		VDD/2+1			V
Input Low Voltage, ICLK1, 2	V <sub>IL</sub>				VDD/2-1	V
Input High Current	I <sub>IH</sub>	V <sub>IH</sub> = VDD	-10		+10	μA
Input Low Current	I <sub>IL</sub>	V <sub>IL</sub> = 0	-10		+10	μA
Input Capacitance, except X1	C <sub>IN</sub>			7		pF
Output High Voltage (CMOS Level)	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	VDD-0.4			V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA			0.4	V
Short Circuit Current	I <sub>OS</sub>			±50		mA
VIN, VCXO Control Voltage	V <sub>XC</sub>		0		VDD	V
Nominal Output Impedance	Z <sub>OUT</sub>			20		Ω



## AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V  $\pm$ 5%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VCXO Crystal Pull Range	$f_{XP}$	Using Recommended Crystal	-115		+115	ppm
VCXO Crystal Nominal Frequency	$f_X$		13.5		27	MHz
Input Jitter Tolerance	$t_{ji}$	In reference to input clock period			0.4	UI
Input pulse width (1)	$t_{pi}$		10			ns
Output Frequency Error	$F_{OUT}$	ICLK = 0 ppm error	0	0	0	ppm
Output Duty Cycle (% high time)	$t_{OD}$	Measured at VDD/2, $C_L=15pF$	40		60	%
Output Rise Time	$t_{OR}$	0.8 to 2.0V, $C_L=15pF$			1.5	ns
Output Fall Time	$t_{OF}$	2.0 to 0.8V, $C_L=15pF$			1.5	ns
Skew, Input to Output Clock Note 2	$t_{IO}$	All output clock selections except 1.544 and 2.048 MHz	-5		+5	ns
Cycle Jitter (short term jitter)	$t_{ja}$			150		ps p-p
Timing Jitter, Filtered 500Hz-1.3MHz (OC-3)	$t_{jf}$	Referenced to Mitel/Zarlink MT9045, Note 3		227		ps p-p
Timing Jitter, Filtered 65kHz-1.3MHz (OC-3)	$t_{jf}$	Referenced to Mitel/Zarlink MT9045, Note 3		170		ps p-p

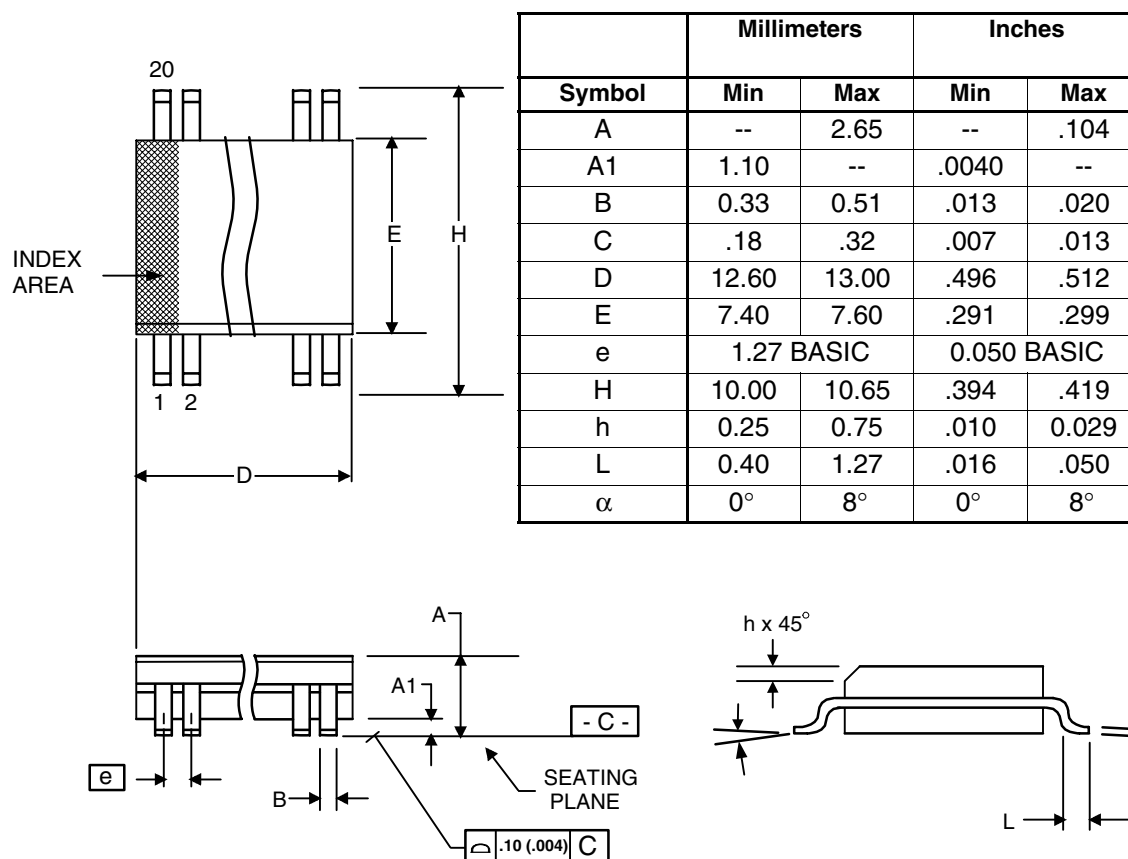
Note 1: Minimum high or low time of input clock.

Note 2: For the 1.544MHz and 2.048MHz output selections, the input to output clock skew is not controlled nor predictable and will change between power up cycles. Because it is dependent on the phase relationship between the output and feedback divider states following power up, the input to output clock skew will remain stable during a given power up cycle. If controlled input to output skew is desired for this output clock frequency please refer to the MK2049 or MK2069 products.

Note 3: Input reference is the 8 kHz output from a Mitel/Zarlink MT9045 device in freerun mode (SEL2:0 = 100, 19.44 MHz external crystal).

## Package Outline and Package Dimensions (20 pin SOIC, 300 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK2059-01SILF	MK2059-01SILF	Tubes	20 pin SOIC	-40 to +85° C
MK2059-01SILFTR	MK2059-01SILF	Tape and Reel	20 pin SOIC	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.