

MJE521

Plastic Medium-Power NPN Silicon Transistor

These devices are designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

Features

- DC Current Gain – $h_{FE} = 40$ (Min) @ $I_C = 1.0$ Adc
- Complementary to PNP MJE371
- Pb-Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0	Adc
Base Current – Continuous	I_B	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40 0.32	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	θ_{JC}	3.12	$^\circ\text{C/W}$

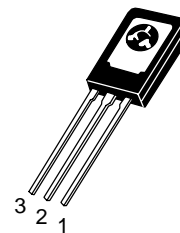
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



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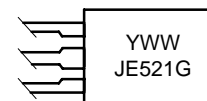
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**4 AMPERES
POWER TRANSISTORS
NPN SILICON
40 VOLTS, 40 WATTS**



TO-225
CASE 77
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week
JE521 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE521	TO-225	500 Units/Box
MJE521G	TO-225 (Pb-Free)	500 Units/Box

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MJE521

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 1) ($I_C = 100\text{ mA}_{dc}$, $I_B = 0$)	$V_{CEO(sus)}$	40	–	Vdc
Collector–Base Cutoff Current ($V_{CB} = 30\text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	100	μA_{dc}
Emitter–Base Cutoff Current ($V_{EB} = 4.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	100	μA_{dc}
ON CHARACTERISTICS				
DC Current Gain (Note 1) ($I_C = 1.0\text{ A}_{dc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	40	–	–

1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

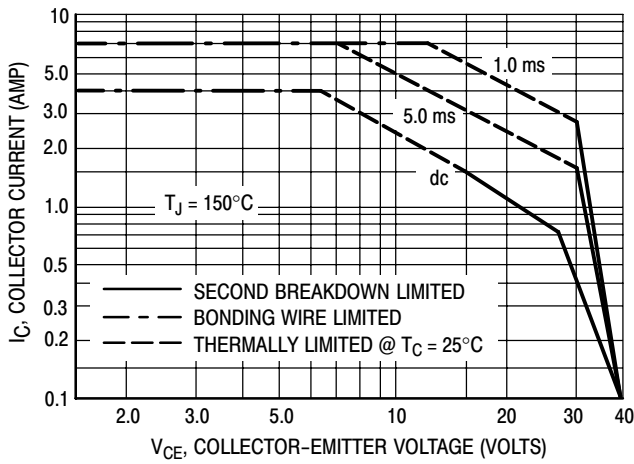


Figure 1. Active-Region Safe Operating Area

The data of Figure 1 based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $(T_{Jpk}) \leq 150^{\circ}\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

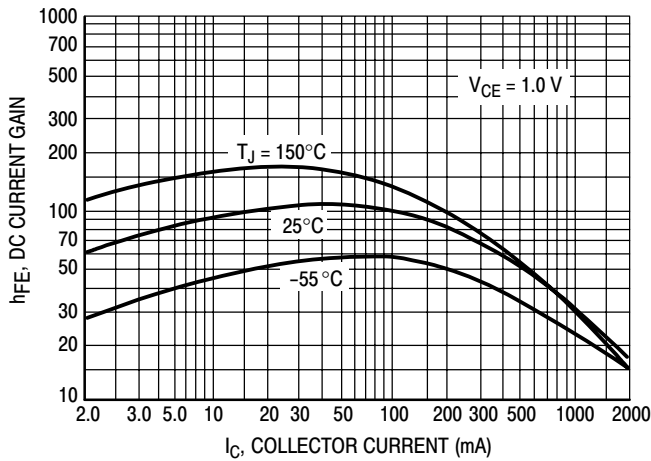


Figure 2. DC Current Gain

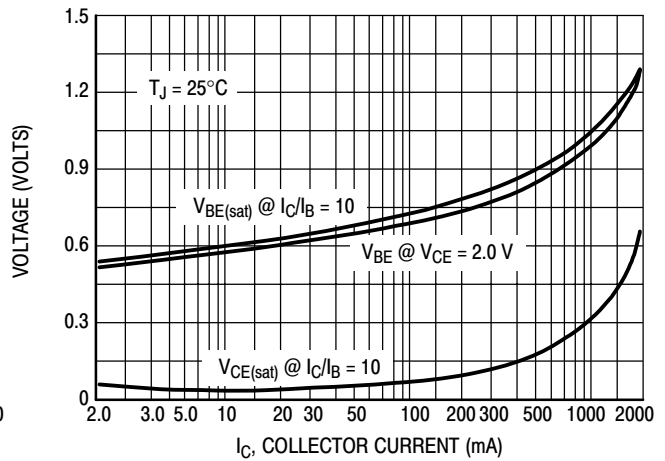


Figure 3. "On" Voltage

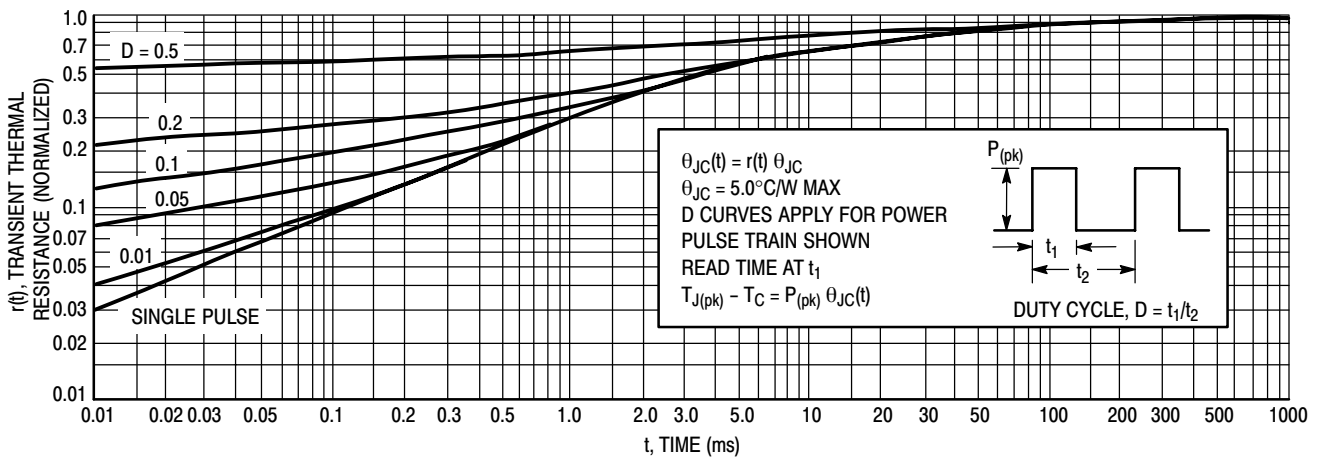


Figure 4. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

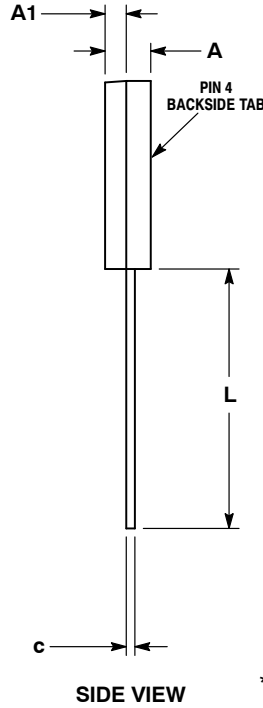
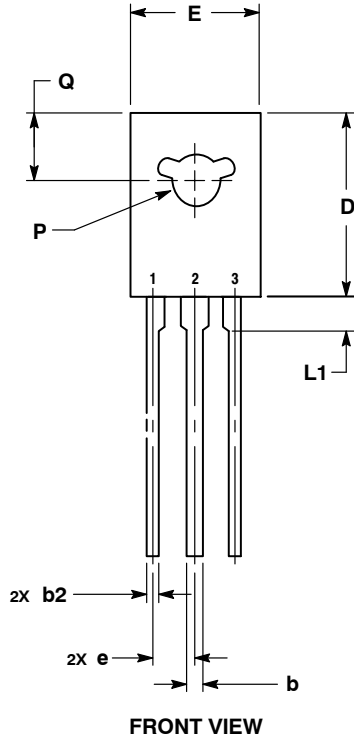
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TO-225
CASE 77-09
ISSUE AD

DATE 25 MAR 2015

SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

DIM	MILLIMETERS	
	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

GENERIC MARKING DIAGRAM*



- Y = Year
- WW = Work Week
- XXXXX = Device Code
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

- | | | | | |
|---|---|---|---|---|
| <p>STYLE 1:
PIN 1. EMITTER
2., 4. COLLECTOR
3. BASE</p> | <p>STYLE 2:
PIN 1. CATHODE
2., 4. ANODE
3. GATE</p> | <p>STYLE 3:
PIN 1. BASE
2., 4. COLLECTOR
3. EMITTER</p> | <p>STYLE 4:
PIN 1. ANODE 1
2., 4. ANODE 2
3. GATE</p> | <p>STYLE 5:
PIN 1. MT 1
2., 4. MT 2
3. GATE</p> |
| <p>STYLE 6:
PIN 1. CATHODE
2., 4. GATE
3. ANODE</p> | <p>STYLE 7:
PIN 1. MT 1
2., 4. GATE
3. MT 2</p> | <p>STYLE 8:
PIN 1. SOURCE
2., 4. GATE
3. DRAIN</p> | <p>STYLE 9:
PIN 1. GATE
2., 4. DRAIN
3. SOURCE</p> | <p>STYLE 10:
PIN 1. SOURCE
2., 4. DRAIN
3. GATE</p> |

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