Phase-Frequency Detector

MCH12140, MCK12140

Description

The MCH/K12140 is a phase frequency−detector intended for phase−locked loop applications which require a minimum amount of phase and frequency difference at lock. When used in conjunction with high performance VCO such as the MC100EL1648, a high bandwidth PLL can be realized. The device is functionally compatible with the MC12040 phase−frequency detector with the maximum frequency extending to 800 MHz.

When the Reference (R) and VCO (V) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO. See AND8040 for further information. The device is packaged in a small outline, surface mount 8−lead SOIC package. There are two versions of the device to provide I/O compatibility to the two existing ECL standards. The MCH12140 is compatible with MECL™ 10H logic levels while the MCK12140 is compatible to 100 K ECL logic levels. This device can also be used in +5.0 V systems. See AND8020 for termination information

Features

- 800 MHz Typical Bandwidth
- Small Outline 8-Lead SOIC Package
- 75 kΩ Internal Input Pulldown Resistors
- >1000 V ESD Protection
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

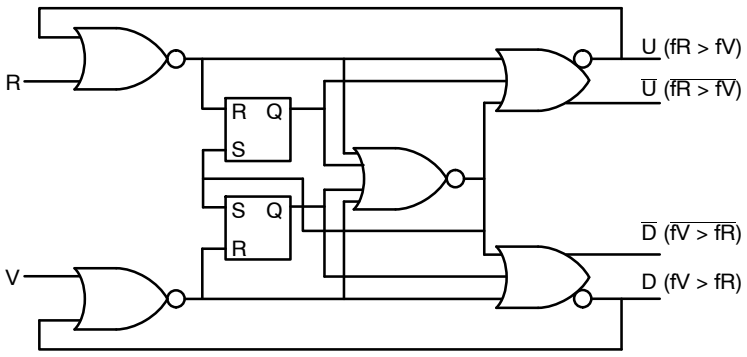


Figure 1. Logic Diagram

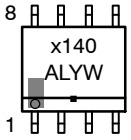
For proper operation, the input edge rate of the R and V inputs should be less than 5.0 ns.

ON Semiconductor®

www.onsemi.com

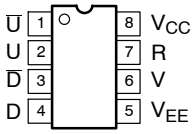
SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



x	= H or K
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
MCH12140DG	SOIC−8 (Pb−Free)	98 Units / Tube
MCK12140DG	SOIC−8 (Pb−Free)	98 Units / Tube
MCK12140DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 1. TRUTH TABLE*

Input		Output				Input		Output			
R	V	U	D	U	D	R	V	U	D	U	D
0	0	X	X	X	X	1	1	0	0	1	1
0	1	X	X	X	X	1	0	0	0	1	1
1	1	X	X	X	X	1	1	0	1	1	0
0	1	X	X	X	X	1	0	0	1	1	0
1	1	1	0	0	1	1	1	0	1	1	0
0	1	1	0	0	1	0	1	0	1	1	0
1	1	1	0	0	1	1	1	0	0	1	1
1	0	1	0	0	1						

*This is not strictly a functional table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly.

Table 2. H−SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND (Note 1), unless otherwise noted.)

		−40°C		0°C		25°C		70°C		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	Output HIGH Voltage	−1080	−890	−1020	−840	−980	−810	−910	−720	mV
V_{OL}	Output LOW Voltage	−1950	−1650	−1950	−1630	−1950	−1630	−1950	−1595	mV
V_{IH}	Input HIGH Voltage	−1230	−890	−1170	−840	−1130	−810	−1060	−720	mV
V_{IL}	Input LOW Voltage	−1950	−1500	−1950	−1480	−1950	−1480	−1950	−1445	mV
I_{IL}	Input LOW Current	0.5	–	0.5	–	0.5	–	0.3	–	μA

Table 3. K−SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND (Note 2), unless otherwise noted.)

		−40°C			0°C to 70°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Condition	Unit
V_{OH}	Output HIGH Voltage	−1085	−1005	−880	−1025	−955	−880	V_{IN} = V_{IH}(max)	mV
V_{OL}	Output LOW Voltage	−1830	−1695	−1555	−1810	−1705	−1620	or V_{IL}(min)	mV
V_{OHA}	Output HIGH Voltage	−1095	–	–	−1035	–	–	V_{IN} = V_{IH}(min)	mV
V_{OLA}	Output LOW Voltage	–	–	−1555	–	–	−1610	or V_{IL}(max)	mV
V_{IH}	Input HIGH Voltage	−1165	–	−880	−1165	–	−880	–	mV
V_{IL}	Input LOW Voltage	−1810	–	−1475	−1810	–	−1475	–	mV
I_{IL}	Input LOW Current	0.5	–	–	0.5	–	–	V_{IN} = V_{IL}(max)	μA

Table 4. MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0 V)	−8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0 V)	0 to −6.0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	−40 to +70	°C
V_{EE}	Operating Range (Note 3)	−5.7 to −4.2	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: ESD data available upon request.

1. 10H circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V except where otherwise specified on the individual data sheets.
2. This table replaces the three tables traditionally seen in ECL 100 K data books. The same DC parameter values at V_{EE} = −4.5 V now apply across the full V_{EE} range of −4.2 V to −5.5 V. Outputs are terminated through a 50 Ω resistor to −2.0 V except where otherwise specified on the individual data sheets.
3. Parametric values specified at: H−Series: −4.20 V to −5.50 V
K−Series: −4.94 V to −5.50 V

Table 5. DC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND, unless otherwise noted.)

Symbol	Characteristic	−40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current H K	– –	45 45	– –	38 38	45 45	52 52	38 38	45 45	52 52	38 42	45 50	52 58	mA
V_{EE}	Power Supply Voltage H K	−4.75 −4.20	−5.2 −4.5	−5.5 −5.5	−4.75 −4.20	−5.2 −4.5	−5.5 −5.5	−4.75 −4.20	−5.2 −4.5	−5.5 −5.5	−4.75 −4.20	−5.2 −4.5	−5.5 −5.5	V
I_{IH}	Input HIGH Current	–	–	150	–	–	150	–	–	150	–	–	150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 6. AC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND, unless otherwise noted.)

Symbol	Characteristic	−40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F_{MAX}	Maximum Toggle Frequency	–	800	–	650	800	–	650	800	–	650	800	–	–
t_{PLH} t_{PHL}	Propagation Delay−to−Output R, V to D, U	250	375	500	250	375	500	250	375	500	250	375	500	ps
t_r t_f	Output Rise/Fall Times Q (20 to 80%)	–	225	–	100	225	350	100	225	350	100	225	350	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

APPLICATIONS INFORMATION

The 12140 is a high speed digital circuit used as a phase comparator in an analog phase-locked loop. The device determines the “lead” or “lag” phase relationship and time difference between the leading edges of a VCO (V) signal and a Reference (R) input. Since these edges occur only once per cycle, the detector has a range of ±2π radians.

The operation of the 12140 can best be described using the plots of Figure 2. Figure 2 plots the average value of $\overline{U}$, $\overline{D}$ and the difference between $\overline{U}$ and $\overline{D}$ versus the phase difference between the V and R inputs.

There are four potential relationships between V and R: R lags or leads V and the frequency of R is less than or greater than the frequency of V. Under these four conditions the 12140 will function as follows:

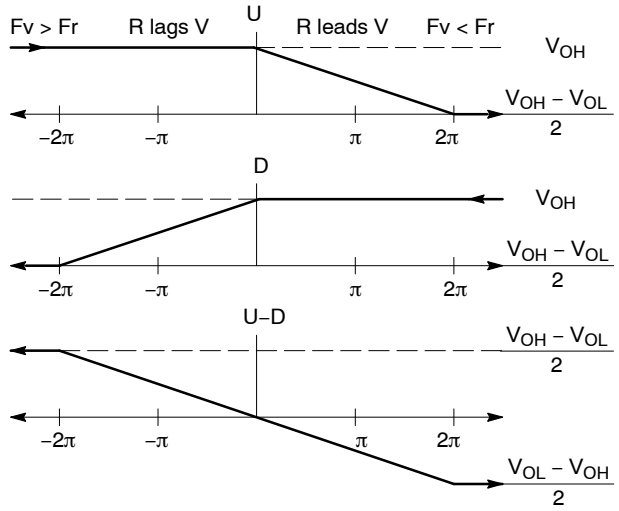


Figure 2. Average Output Voltage vs. Phase Difference

R lags V in phase

When the R and V inputs are equal in frequency and the phase of R lags that of V the $\overline{U}$ output will stay HIGH while the $\overline{D}$ output will pulse from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{D}$ indicates to the VCO to decrease in frequency to bring the loop into lock.

V frequency > R frequency

When the frequency of V is greater than that of R the 12140 behaves in a similar fashion as above. Again the signal on $\overline{D}$ indicates that the VCO frequency must be decreased to bring the loop into lock.

R leads V in phase

When the R and V inputs are equal in frequency and the phase of R leads that of V the $\overline{D}$ output will stay HIGH while the $\overline{U}$ output pulses from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{U}$ indicates to the VCO to increase in frequency to bring the loop into lock.

V frequency < R frequency

When the frequency of V is less than that of R the 12140 behaves in a similar fashion as above. Again the signal on $\overline{U}$ indicates that the VCO frequency must be decreased to bring the loop into lock.

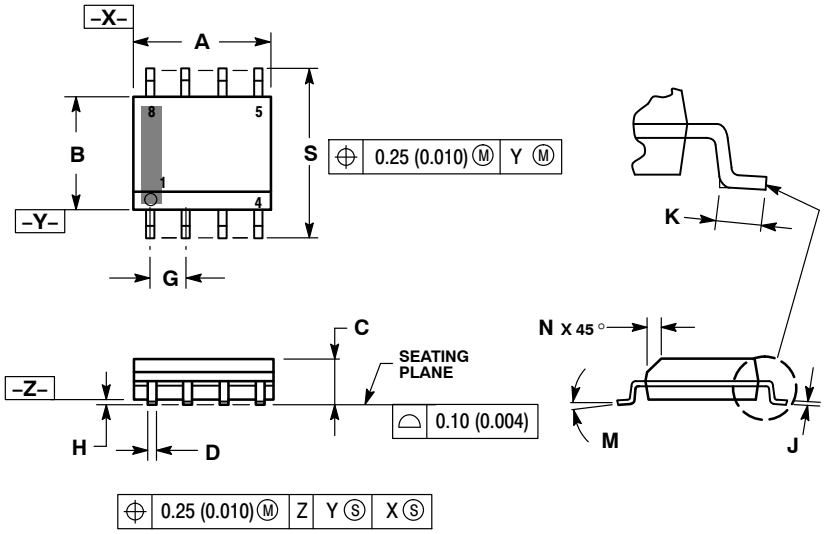
From Figure 2 when V and R are at the same frequency and in phase the value of $\overline{U} - \overline{D}$ is zero thus providing a zero error voltage to the VCO. This situation indicates the loop is in lock and the 12140 action will maintain the loop in its locked state.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

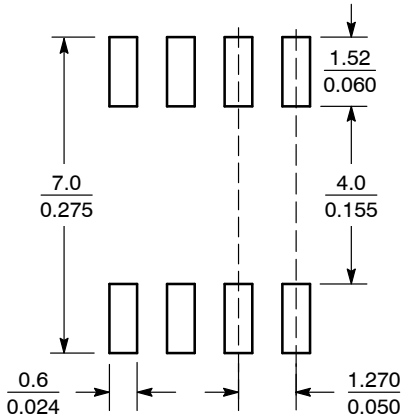
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

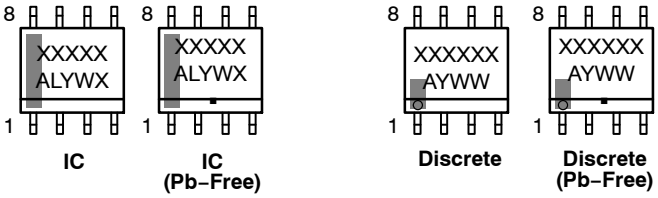
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales