

# MC74VHCT74A

## Dual D-Type Flip-Flop with Set and Reset

The MC74VHCT74A is an advanced high speed CMOS D-type flip-flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset ( $\overline{RD}$ ) and Set ( $\overline{SD}$ ) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT74A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- High Speed:  $f_{max} = 60$  MHz (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 2$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- Pb-Free Packages are Available

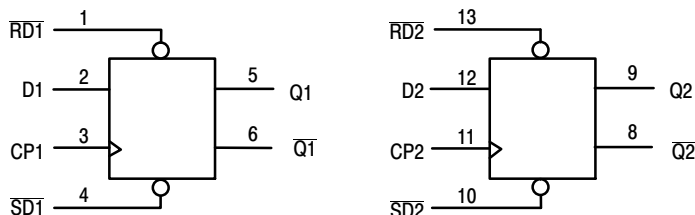


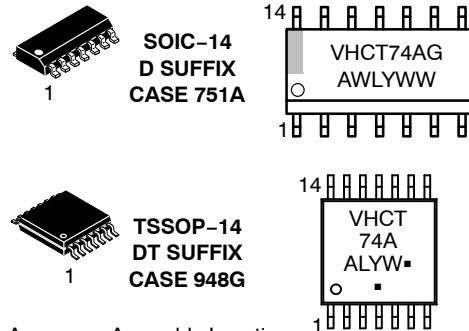
Figure 2. Logic Diagram



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### MARKING DIAGRAMS



A = Assembly Location  
 WL, L = Wafer Lot  
 Y = Year  
 WW, W = Work Week  
 G or  $\bullet$  = Pb-Free Package  
 (Note: Microdot may be in either location)

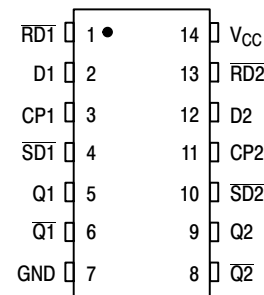


Figure 1. Pin Assignment

### FUNCTION TABLE

Inputs				Outputs	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	↔	X	No Change	No Change

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# MC74VHCT74A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage V <sub>CC</sub> = 0 High or Low State	-0.5 to +7.0 -0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current (V <sub>OUT</sub> < GND; V <sub>OUT</sub> > V <sub>CC</sub> )	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	4.5	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage V <sub>CC</sub> = 0 High or Low State	0 0	5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time V <sub>CC</sub> = 5.0 V ± 0.5 V	0	20	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55 to 125°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	4.5	4.4	4.5		4.4		V
		I <sub>OH</sub> = -8 mA	4.5	3.94			3.80		V
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	4.5		0.0	0.1		0.1	V
		I <sub>OL</sub> = 8 mA	4.5			0.36		0.44	V
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			2.0		20.0	μA
I <sub>CC(T)</sub>	Quiescent Supply Current	Per Input: V <sub>IN</sub> = 3.4 V Other Input: V <sub>CC</sub> or GND	5.5			1.35		1.50	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0			0.5		5.0	μA

# MC74VHCT74A

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -55 \text{ to } 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, CP to Q or $\bar{Q}$	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		5.8 6.3	7.8 8.8	1.0 1.0	9.0 10.0	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, $\bar{SD}$ or $\bar{RD}$ to Q or $\bar{Q}$	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		7.6 8.1	10.4 11.4	1.0 1.0	12.0 13.0	ns
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$	100 80	160 140		80 65		MHz
$C_{in}$	Maximum Input Capacitance			4	10		10	pF

Symbol	Parameter	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$		Unit
		24		
$C_{PD}$	Power Dissipation Capacitance (Note 1)			pF

1.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$  (per flip-flop).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## TIMING REQUIREMENTS (Input $t_r = t_f = 3.0 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -55 \text{ to } 125^\circ\text{C}$	
$t_w$	Minimum Pulse Width, CP	$5.0 \pm 0.5$	5.0	5.0	ns
$t_w$	Minimum Pulse Width, $\bar{RD}$ or $\bar{SD}$	$5.0 \pm 0.5$	5.0	5.0	ns
$t_{su}$	Minimum Setup Time, D to CP	$5.0 \pm 0.5$	5.0	5.0	ns
$t_h$	Minimum Hold Time, D to CP	$5.0 \pm 0.5$	0.0	0.0	ns
$t_{rec}$	Minimum Recovery Time, $\bar{SD}$ or $\bar{RD}$ to CP	$5.0 \pm 0.5$	3.5	3.5	ns

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74VHCT74AD	SOIC-14	55 Units / Rail
MC74VHCT74ADR2	SOIC-14	2500 / Tape & Reel
MC74VHCT74ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHCT74ADT	TSSOP-14*	96 Units / Rail
MC74VHCT74ADTR2	TSSOP-14*	2500 / Tape & Reel
MC74VHCT74ADTR2G	TSSOP-14*	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74VHCT74A

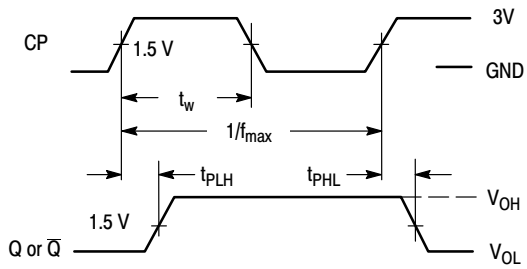


Figure 3. Switching Waveform

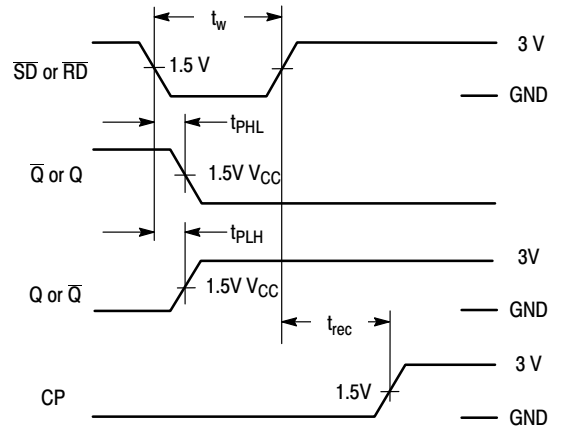


Figure 4. Switching Waveform

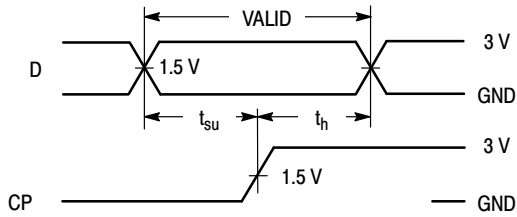
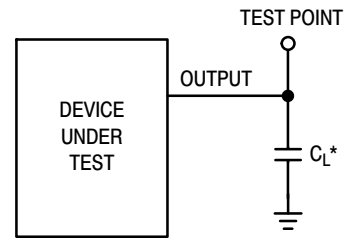


Figure 5. Switching Waveform



\*Includes all probe and jig capacitance

Figure 6. Switching Waveform

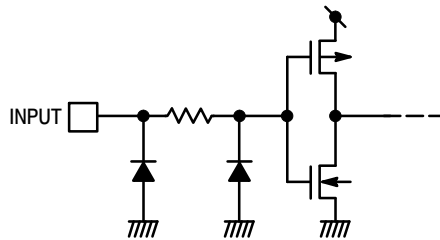


Figure 7. Input Equivalent Circuit

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

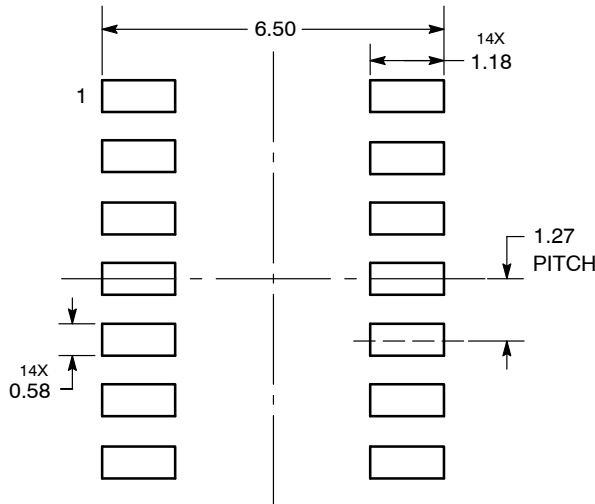


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

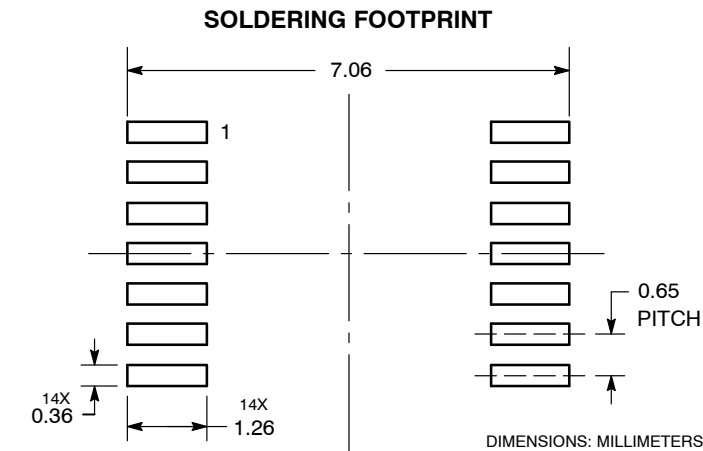
**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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