

Micropower Undervoltage Sensing Circuits

MC34164, MC33164, NCV33164

The MC34164 series are undervoltage sensing circuits specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is required. These devices offer the designer an economical solution for low voltage detection with a single external resistor. The MC34164 series features a bandgap reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 6.0 mA, and guaranteed operation down to 1.0 V input with extremely low standby current. The MC devices are packaged in 3-pin TO-92 (TO-226AA), micro size TSOP-5, 8-pin SOIC-8 and Micro8 surface mount packages. The NCV device is packaged in SOIC-8.

Applications include direct monitoring of the 3.0 V or 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

Features

- Temperature Compensated Reference
- Monitors 3.0 V (MC34164-3) or 5.0 V (MC34164-5) Power Supplies
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 6.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation With 1.0 V Input
- Extremely Low Standby Current: As Low as 9.0 μ A
- Economical TO-92 (TO-226AA), TSOP-5, SOIC-8 and Micro8 Surface Mount Packages
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These Devices are Pb-Free and are RoHS Compliant

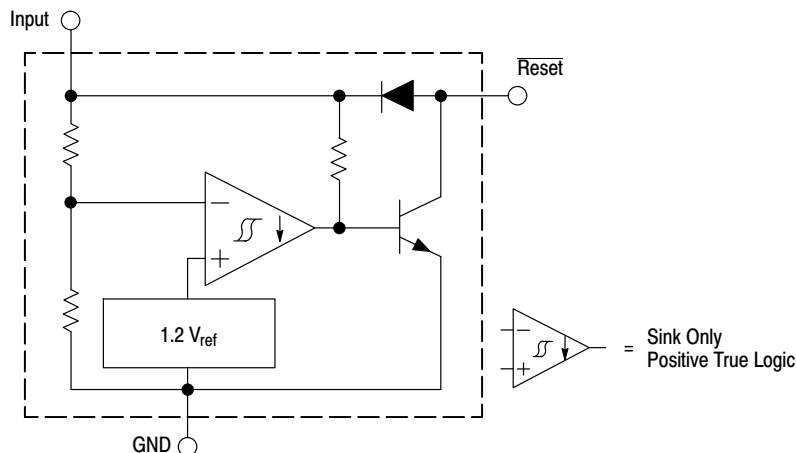
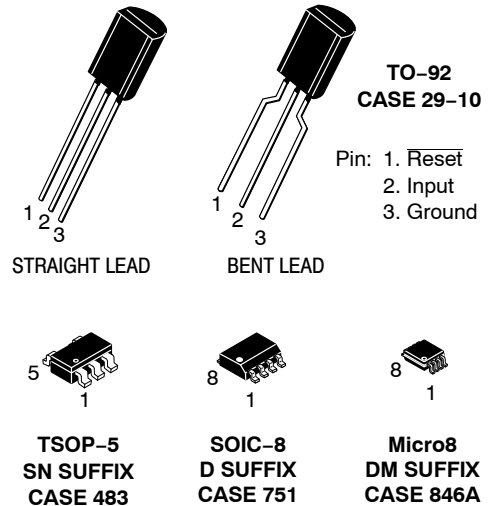
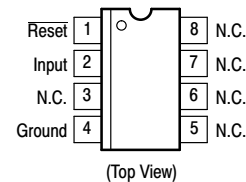


Figure 1. Representative Block Diagram

This device contains 28 active transistors.



PIN CONNECTIONS



TSOP-5

- Pin 1. Ground
Pin 2. Input
Pin 3. $\overline{\text{Reset}}$
Pin 4. NC
Pin 5. NC

TO-92

- Pin 1. $\overline{\text{Reset}}$
Pin 2. Input
Pin 3. Ground

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

MC34164, MC33164, NCV33164

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	-1.0 to 12	V
Reset Output Voltage	V_O	-1.0 to 12	V
Reset Output Sink Current	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Reset to Input Pin (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	700	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	178	$^\circ\text{C/W}$
D Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	700	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	178	$^\circ\text{C/W}$
DM Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	520	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	240	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A		$^\circ\text{C}$
MC34164 Series		0 to +70	
MC33164 Series, NCV33164		-40 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Electrostatic Discharge Sensitivity (ESD)	ESD		V
Human Body Model (HBM)		4000	
Machine Model (MM)		200	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MC34164-3, MC33164-3 SERIES, NCV33164-3

ELECTRICAL CHARACTERISTICS (For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 & 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

COMPARATOR

Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	2.55	2.71	2.80	
Low State Output (V_{in} Decreasing)	V_{IL}	2.55	2.65	2.80	
Hysteresis ($I_{Sink} = 100 \mu\text{A}$)	V_H	0.03	0.06	-	

RESET OUTPUT

Output Sink Saturation	V_{OL}				V
($V_{in} = 2.4 \text{ V}$, $I_{Sink} = 1.0 \text{ mA}$)		-	0.14	0.4	
($V_{in} = 1.0 \text{ V}$, $I_{Sink} = 0.25 \text{ mA}$)		-	0.1	0.3	
Output Sink Current (V_{in} , $\overline{\text{Reset}} = 2.4 \text{ V}$)	I_{Sink}	6.0	12	30	mA
Output Off-State Leakage	$I_R(\text{leak})$				μA
(V_{in} , $\overline{\text{Reset}} = 3.0 \text{ V}$)		-	0.02	0.5	
(V_{in} , $\overline{\text{Reset}} = 10 \text{ V}$)		-	0.02	1.0	
Clamp Diode Forward Voltage, Reset to Input Pin ($I_F = 5.0 \text{ mA}$)	V_F	0.6	0.9	1.2	V

TOTAL DEVICE

Operating Input Voltage Range	V_{in}	1.0 to 10	-	-	V
Quiescent Input Current	I_{in}				μA
$V_{in} = 3.0 \text{ V}$		-	9.0	15	
$V_{in} = 6.0 \text{ V}$		-	24	40	

- Maximum package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$ for MC34164 $T_{high} = +70^\circ\text{C}$ for MC34164
 = -40°C for MC33164, NCV33164 = $+125^\circ\text{C}$ for MC33164, NCV33164

MC34164, MC33164, NCV33164

MC34164-5, MC33164-5 SERIES, NCV33164-5

ELECTRICAL CHARACTERISTICS (For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Notes 5 & 6], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

COMPARATOR

Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.15	4.33	4.45	
Low State Output (V_{in} Decreasing)	V_{IL}	4.15	4.27	4.45	
Hysteresis ($I_{Sink} = 100 \mu\text{A}$)	V_H	0.02	0.09	-	

RESET OUTPUT

Output Sink Saturation ($V_{in} = 4.0 \text{ V}$, $I_{Sink} = 1.0 \text{ mA}$) ($V_{in} = 1.0 \text{ V}$, $I_{Sink} = 0.25 \text{ mA}$)	V_{OL}	-	0.14 0.1	0.4 0.3	V
Output Sink Current (V_{in} , $\overline{\text{Reset}} = 4.0 \text{ V}$)	I_{Sink}	7.0	20	50	mA
Output Off-State Leakage (V_{in} , $\overline{\text{Reset}} = 5.0 \text{ V}$) (V_{in} , $\overline{\text{Reset}} = 10 \text{ V}$)	$I_{R}(\text{leak})$	-	0.02 0.02	0.5 2.0	μA
Clamp Diode Forward Voltage, Reset to Input Pin ($I_F = 5.0 \text{ mA}$)	V_F	0.6	0.9	1.2	V

TOTAL DEVICE

Operating Input Voltage Range	V_{in}	1.0 to 10	-	-	V
Quiescent Input Current $V_{in} = 5.0 \text{ V}$ $V_{in} = 10 \text{ V}$	I_{in}	-	12 32	20 50	μA

- Maximum package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$ for MC34164 $T_{high} = +70^\circ\text{C}$ for MC34164
 $= -40^\circ\text{C}$ for MC33164, NCV33164 $= +125^\circ\text{C}$ for MC33164, NCV33164
- NCV prefix is for automotive and other applications requiring site and change control.

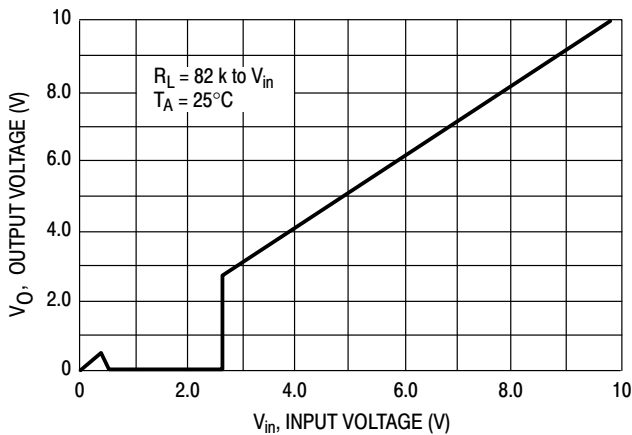


Figure 2. MC3X164-3 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

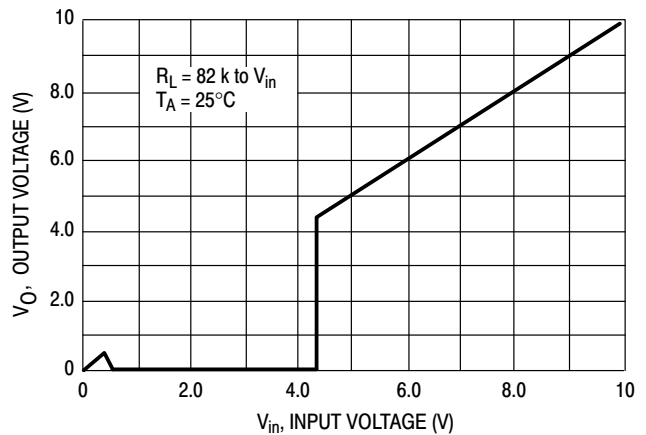


Figure 3. MC3X164-5 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

MC34164, MC33164, NCV33164

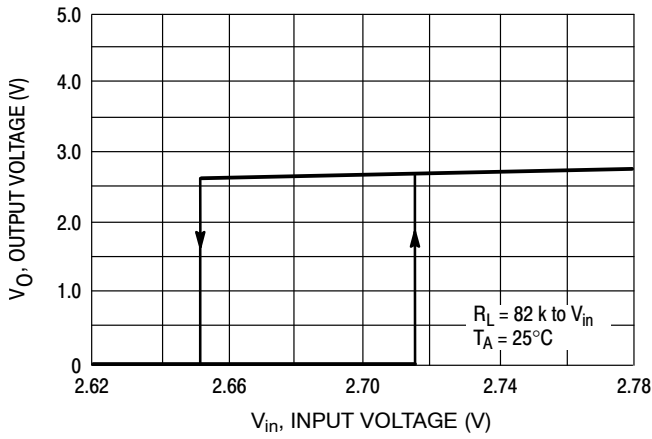


Figure 4. MC3X164-3 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

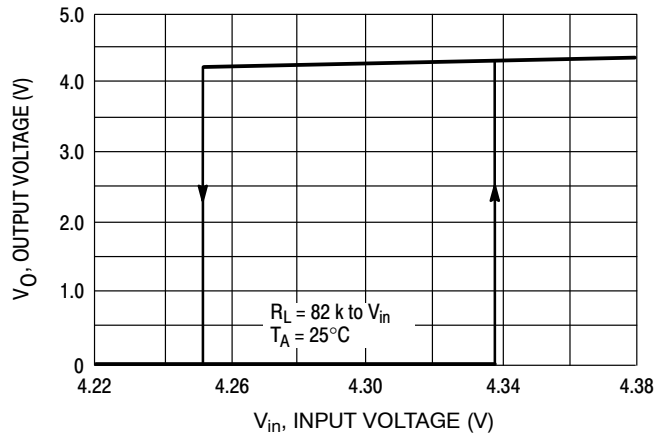


Figure 5. MC3X164-5 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

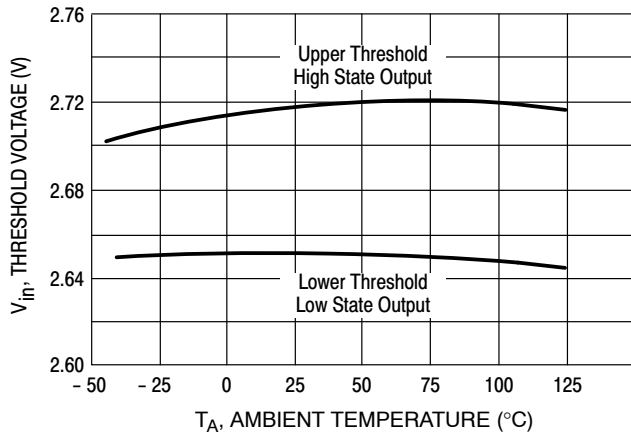


Figure 6. MC3X164-3 Comparator Threshold Voltage versus Temperature

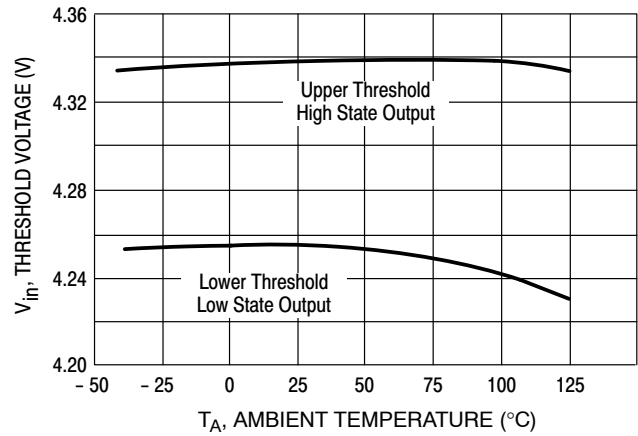


Figure 7. MC3X164-5 Comparator Threshold Voltage versus Temperature

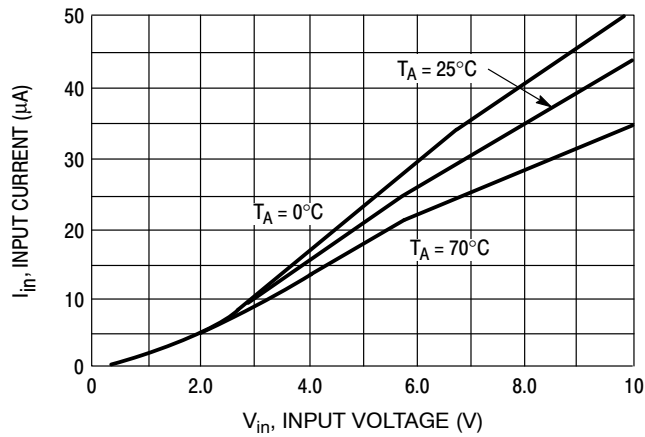


Figure 8. MC3X164-3 Input Current versus Input Voltage

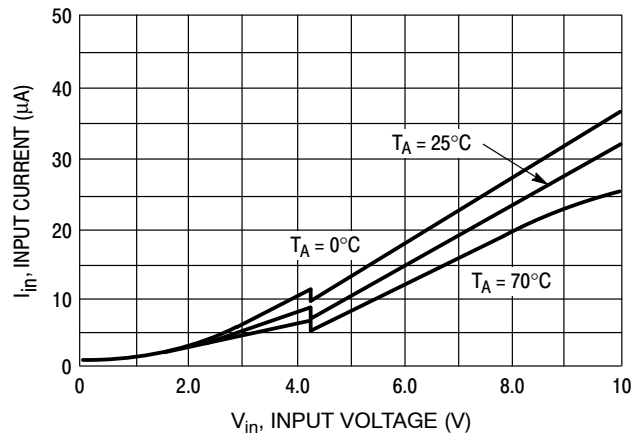


Figure 9. MC3X164-5 Input Current versus Input Voltage

MC34164, MC33164, NCV33164

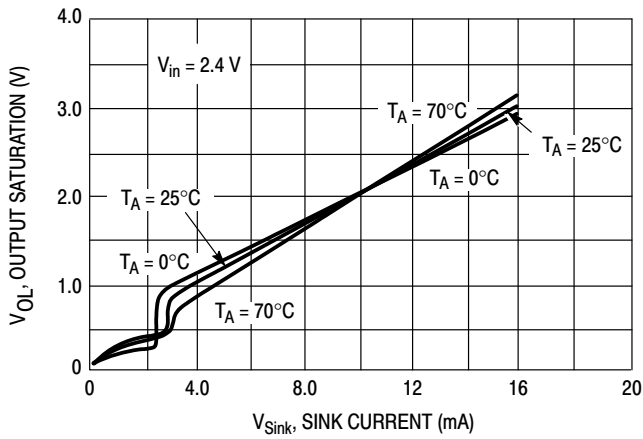


Figure 10. MC3X164-3 Reset Output Saturation versus Sink Current

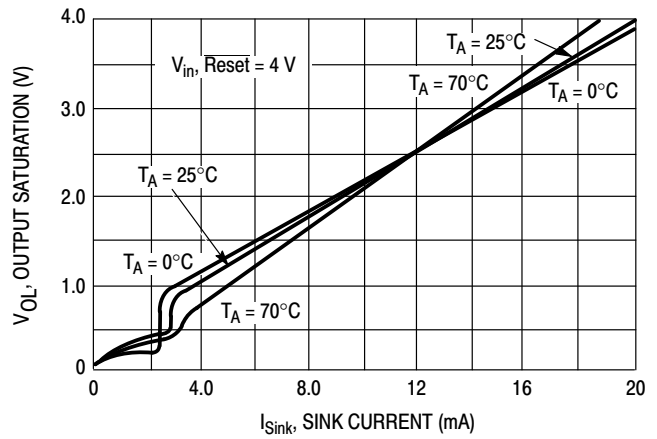


Figure 11. MC3X164-5 Reset Output Saturation versus Sink Current

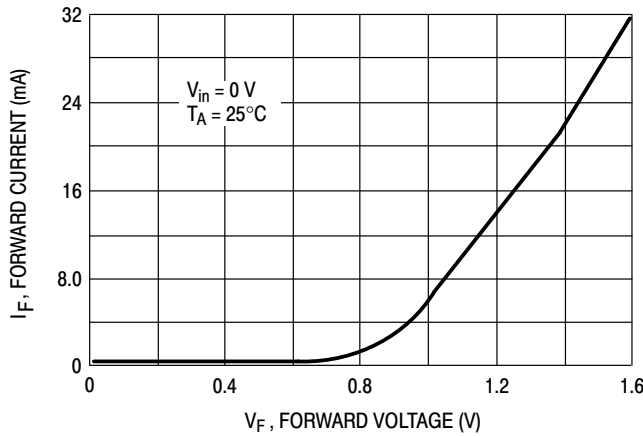


Figure 12. Clamp Diode Forward Current versus Voltage

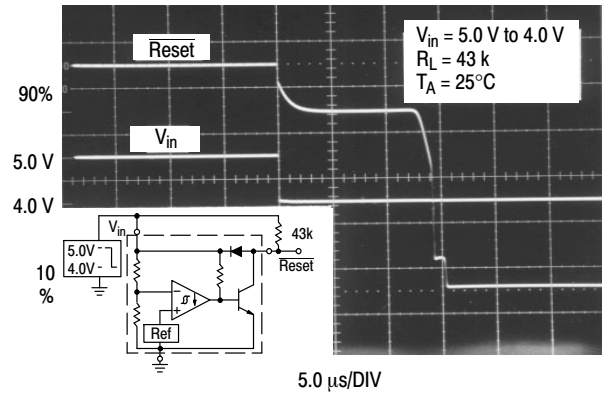
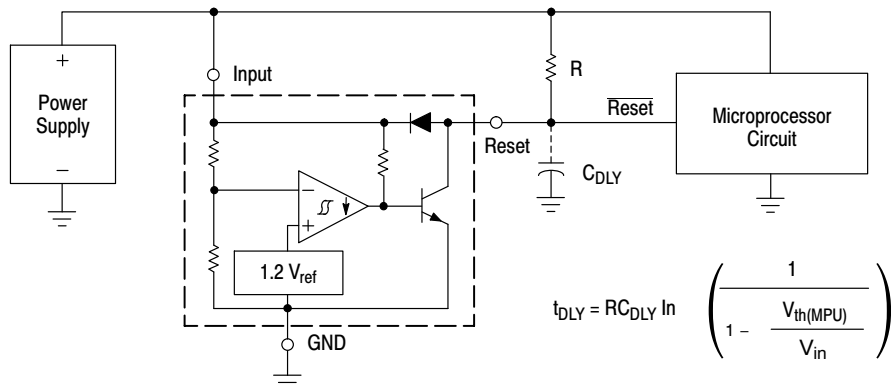


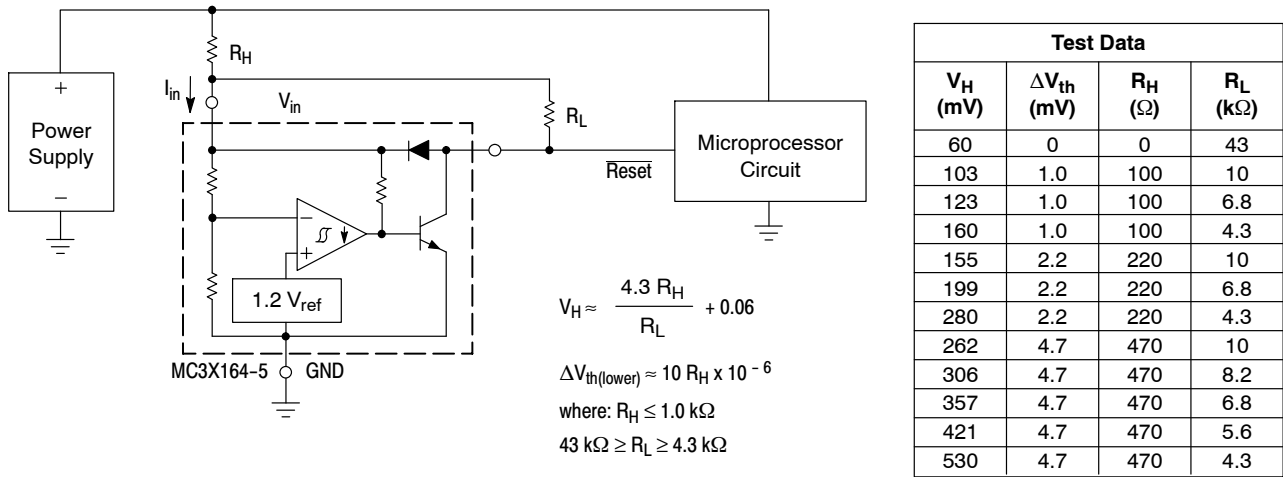
Figure 13. Reset Delay Time (MC3X164-5 Shown)



A time delayed reset can be accomplished with the addition of C_{DLY} . For systems with extremely fast power supply rise times (< 500 ns) it is recommended that the RC_{DLY} time constant be greater than 5.0 μ s. $V_{th(MPU)}$ is the microprocessor reset input threshold.

Figure 14. Low Voltage Microprocessor Reset

MC34164, MC33164, NCV33164



Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{in} crosses the comparator threshold (Figure 8). An increase of the lower threshold ΔV_{th(lower)} will be observed due to I_{in} which is typically 10 μA at 4.3 V. The equations are accurate to ±10% with R_H less than 1.0 kΩ and R_L between 4.3 kΩ and 43 kΩ.

Figure 15. Low Voltage Microprocessor Reset With Additional Hysteresis (MC3X164-5 Shown)

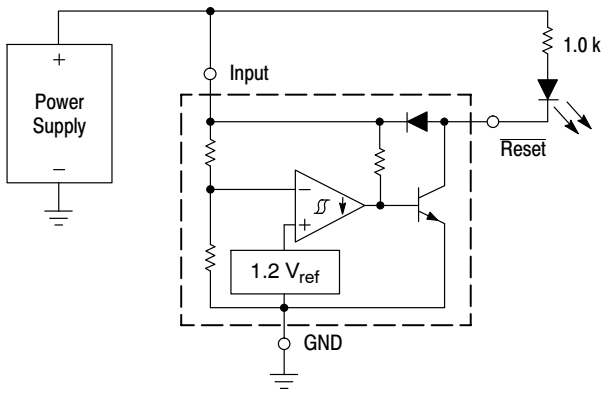


Figure 16. Voltage Monitor

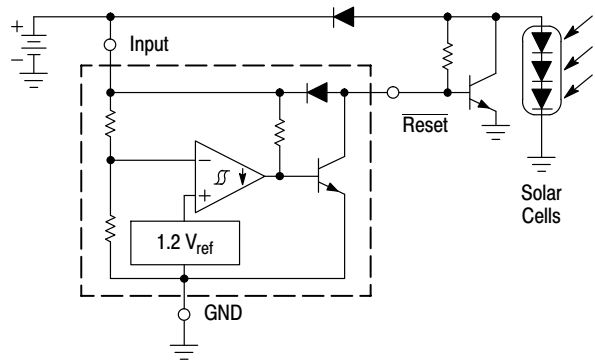
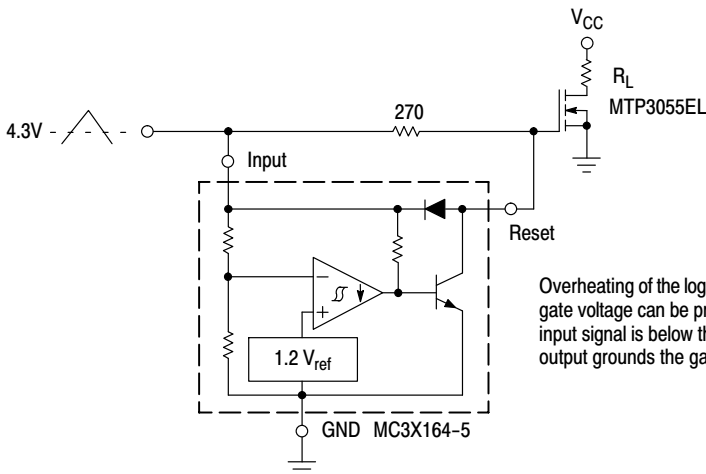


Figure 17. Solar Powered Battery Charger



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.3 V threshold of the MC3X164-5, its output grounds the gate of the L² MOSFET.

Figure 18. MOSFET Low Voltage Gate Drive Protection Using the MC3X164-5

MC34164, MC33164, NCV33164

ORDERING INFORMATION

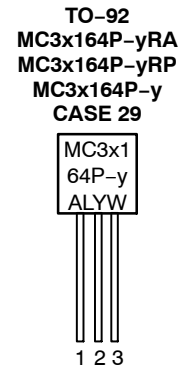
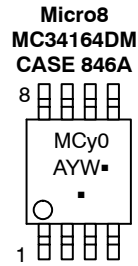
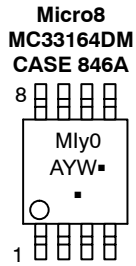
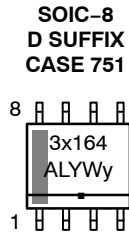
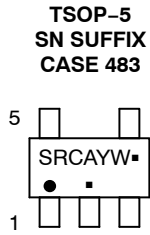
Device	Package	Shipping†
MC33164D-3G	SOIC-8 (Pb-Free)	98 Units / Rail
MC33164D-3R2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
NCV33164D-3R2G*	SOIC-8 (Pb-Free)	
MC33164DM-3R2G	Micro8 (Pb-Free)	4000 Units / Tape & Reel
MC33164P-3G	TO-92 (Pb-Free)	2000 Units / Box
MC33164P-3RAG	TO-92 (Pb-Free)	2000 Units / Tape & Reel
MC33164P-3RPG	TO-92 (Pb-Free)	2000 Units / Pack
MC33164D-5G	SOIC-8 (Pb-Free)	98 Units / Rail
MC33164D-5R2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
NCV33164D-5R2G*	SOIC-8 (Pb-Free)	
MC33164DM-5R2G	Micro8 (Pb-Free)	4000 Units / Tape & Reel
MC33164P-5G	TO-92 (Pb-Free)	2000 Units / Box
MC33164P-5RAG	TO-92 (Pb-Free)	2000 Units / Tape & Reel
MC33164P-5RPG	TO-92 (Pb-Free)	2000 Units / Pack
MC34164D-3G	SOIC-8 (Pb-Free)	98 Units / Rail
MC34164D-3R2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC34164DM-3R2G	Micro8 (Pb-Free)	4000 Units / Tape & Reel
MC34164P-3G	TO-92 (Pb-Free)	2000 Units / Box
MC34164P-3RPG	TO-92 (Pb-Free)	2000 Units / Pack
MC34164D-5G	SOIC-8 (Pb-Free)	98 Units / Rail
MC34164D-5R2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC34164DM-5R2G	Micro8 (Pb-Free)	4000 Units / Tape & Reel
MC34164SN-5T1G	TSOP-5 (Pb-Free)	3000 Units / Tape & Reel
MC34164P-5G	TO-92 (Pb-Free)	2000 Units / Box
MC34164P-5RAG	TO-92 (Pb-Free)	2000 Units / Tape & Reel
MC34164P-5RPG	TO-92 (Pb-Free)	2000 Units / Pack

*NCV33164: $T_{low} = -40^{\circ}\text{C}$, $T_{high} = +125^{\circ}\text{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC34164, MC33164, NCV33164

PIN CONNECTIONS AND MARKING DIAGRAMS

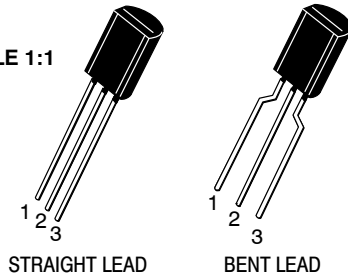


- SRC = Device Code
- x = Device Number 3 or 4
- y = Suffix Number 3 or 5
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



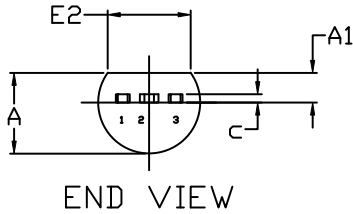
SCALE 1:1



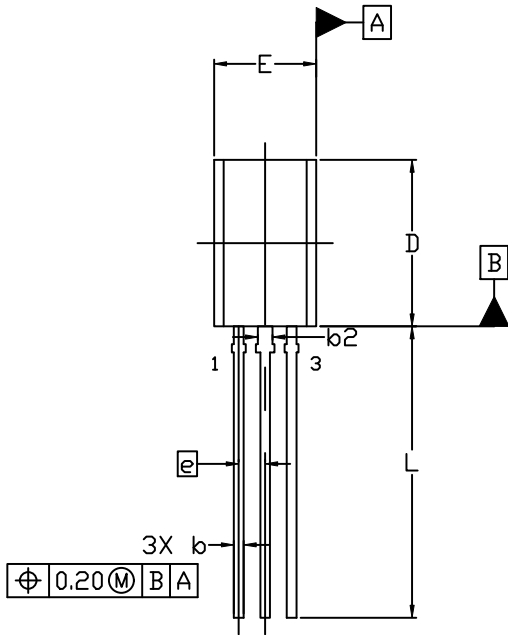
TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



END VIEW



TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

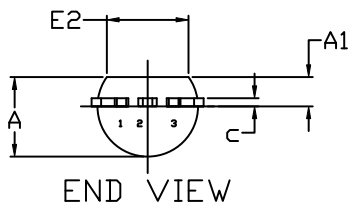
DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 (TO-226) 1 WATT	PAGE 1 OF 3

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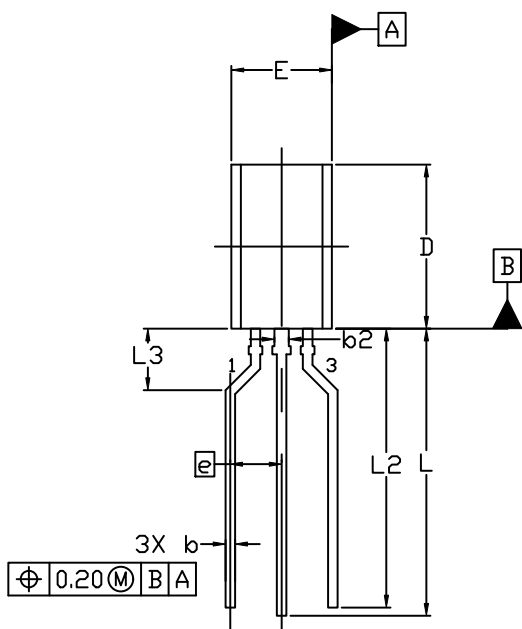
TO-92 (TO-226) 1 WATT
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ISSUE D

DATE 05 MAR 2021

FORMED LEAD



END VIEW



TOP VIEW


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

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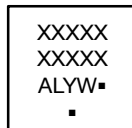
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**TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D**

DATE 05 MAR 2021

- | | | | | |
|---|--|--|---|---|
| <p>STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR</p> | <p>STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR</p> | <p>STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE</p> | <p>STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE</p> |
| <p>STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN</p> | <p>STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE</p> | <p>STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE</p> | <p>STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2</p> | <p>STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE</p> |
| <p>STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE</p> | <p>STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2</p> | <p>STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2</p> | <p>STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE</p> | <p>STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2</p> |
| <p>STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE</p> | <p>STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER</p> | <p>STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED</p> | <p>STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE</p> | <p>STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE</p> |
| <p>STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE</p> | <p>STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN</p> | <p>STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN</p> | <p>STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE</p> | <p>STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2</p> |
| <p>STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT</p> | <p>STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT</p> | <p>STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE</p> | <p>STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE</p> | <p>STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE</p> |
| <p>STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE</p> | <p>STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER</p> | <p>STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT</p> | <p>STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC</p> | <p>STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER</p> |

**GENERIC
MARKING DIAGRAM***




- XXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

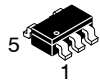
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

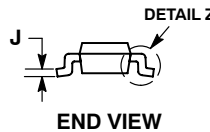
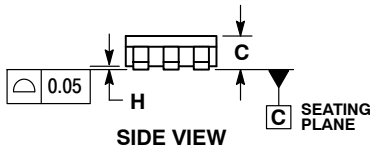
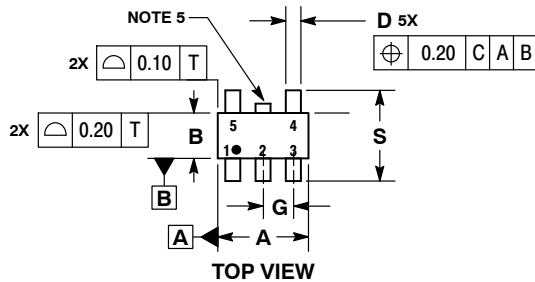
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SCALE 2:1

TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020

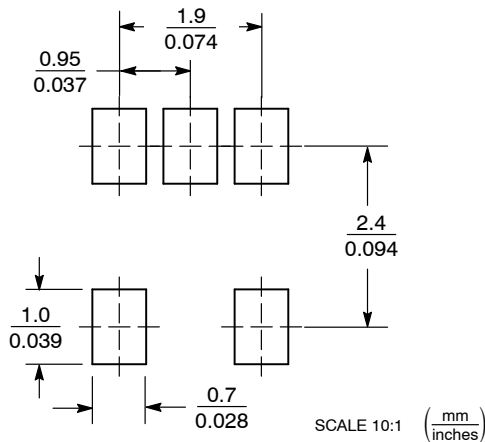


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

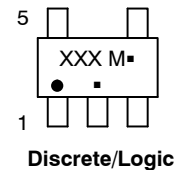
DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ■ = Pb-Free Package
- XXX = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW



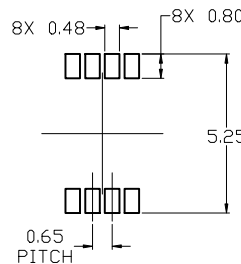
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S

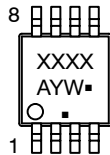
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H_E</i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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