Click here to ask about the production status of specific part numbers.

MAX77932C 8A Dual-Phase Switched-Capacitor Converter

General Description

The MAX77932C is a standalone, dual-phase switched-capacitor converter with integrated power switches that delivers 8A output current and divides the input voltage by two. The IC is suitable for applications that utilize 2S Li+ batteries while powering circuitry that operates at 1S-equivalent voltage. It is also suitable for applications migrating from 1S to 2S battery configurations. The IC simplifies this migration by converting the 2S battery voltage to 1S-equivalent output and allows designers to preserve the existing downstream 1S power architecture.

The inductorless switched-capacitor converter topology of the IC shrinks the overall footprint and reduces the maximum height of the circuit. Its high switching frequency, up to 1.5MHz, reduces the size and number of capacitors required, further minimizing the solution footprint. The IC ensures safe operation with integrated overvoltage, undervoltage, overcurrent, and thermal protection, and also minimizes EMI with built-in frequency dithering. In addition to the small solution size, lower EMI, and protection features, the ICs class-leading peak efficiency of 98.5% simplifies thermal design and makes it ideal for consumer, medical, and industrial applications.

The IC features an I²C compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The IC supports SCL clock rates up to 3.4MHz. The converter parameters such as OCP, OVLO or UVLO thresholds, switching frequency, soft-start current, and duration are easily adjustable through the I²C interface. The IC consumes a low quiescent current of 30µA when operating and 4µA in shutdown. The IC is available in a tiny, lead-free 0.4mm pitch, 2.4mm x 2.8mm 42-pin wafer-level package (WLP).

Applications

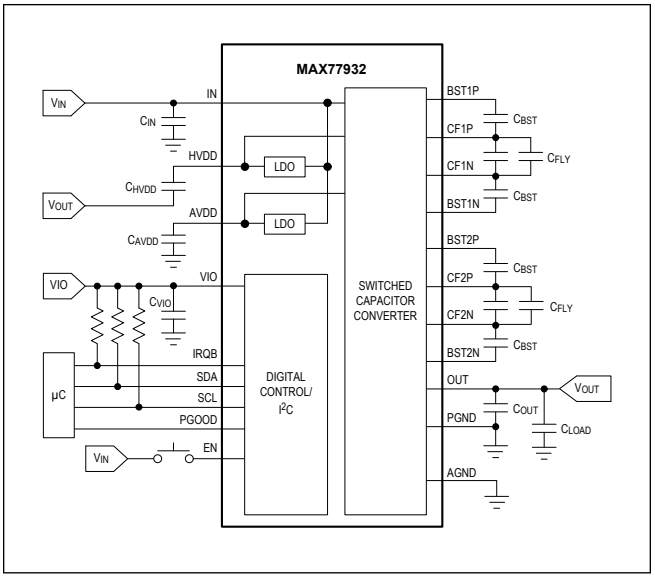
- Smartphones and Tablets
- Ultrabook Computers
- Chromebooks
- DSLR and Mirrorless Cameras
- Power Banks
- 2S Li+ Battery Applications
- Smartphone Direct Charging
- Portable Printers
- Portable Gaming Devices
- Mobile Point-of-Sale (mPOS) Devices
- Two-Way Radios

Benefits and Features

- 8A Switched Capacitor Converter
- 2S to 1S Battery Voltage Conversion ($V_{OUT} = V_{IN}/2$)
- Integrated Power Switches
- Low I_Q: 30µA Operating, 4µA Shutdown
- Soft-Start with Programmable Current and Timeout
- Programmable Input Overvoltage Lockout
- Programmable Output Overvoltage Lockout
- Programmable Overcurrent Protection
- Programmable Switching Frequency 0.25MHz to 1.5MHz
- Thermal Alarm and Protection
- Chip Enable Input
- Power Good Indicator Output
- Frequency Dithering
- I²C Interface with Interrupt

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



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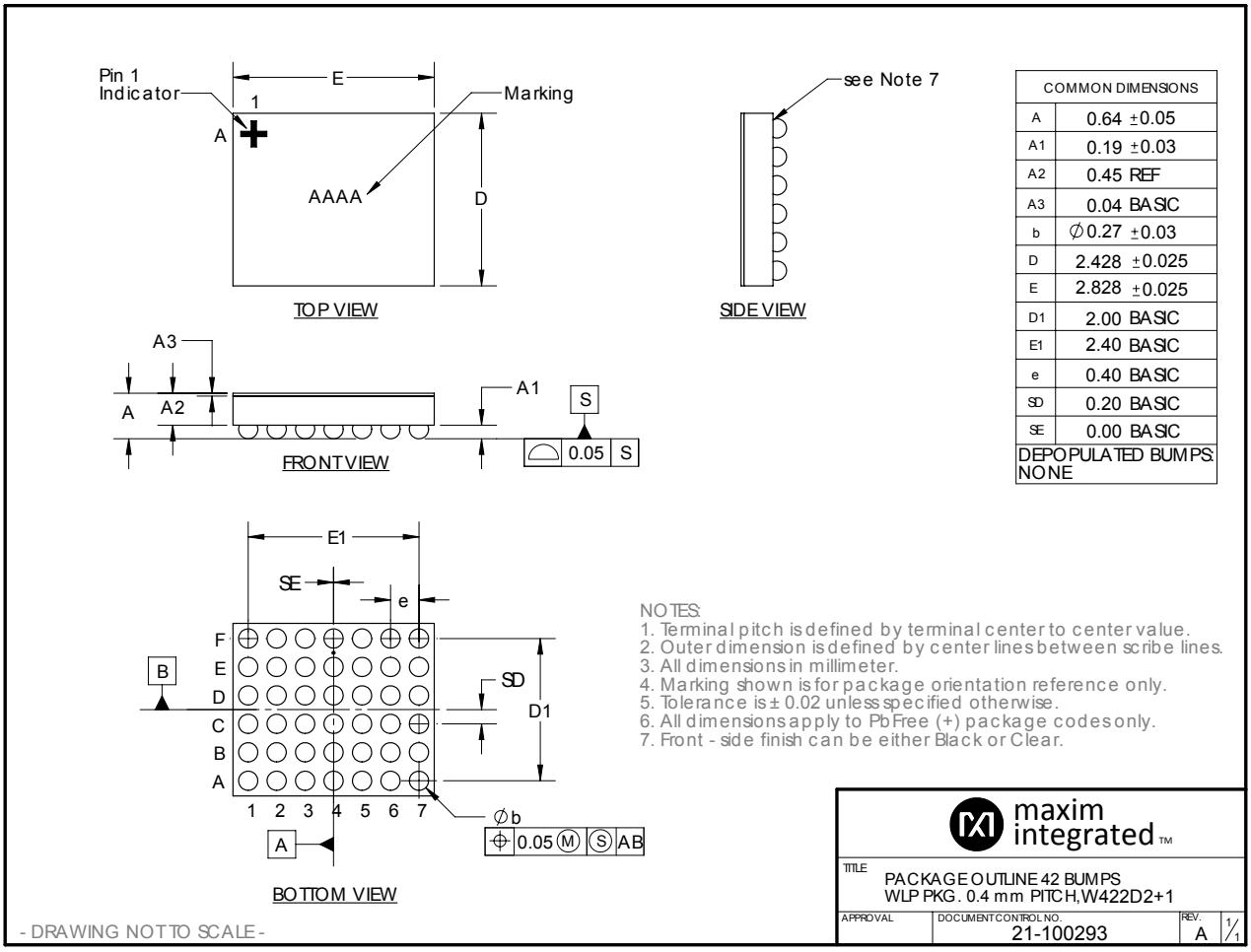
BSTxP to PGND ..... -0.3V to +16V
BSTxN to PGND ..... -0.3V to +8V
BSTxP to CFxP ..... -0.3V to +2V
BSTxN to CFxN ..... -0.3V to +2V
CFxP to PGND ..... -0.3V to V_{OUT} + 6V
CFxN to PGND ..... -0.3V to +6V
OUT to PGND ..... -0.3V to +6V
PGND to AGND ..... -0.3V to +0.3V
HVDD to AGND ..... -0.3V to V_{OUT} + 2V
AVDD to AGND ..... -0.3V to +2V
EN to AGND ..... -0.3V to +16V
NC to AGND ..... -0.3V to +2V
IRQB to DGND ..... -0.3V to +6V
VIO to AGND ..... -0.3V to +6V
SDA to DGND ..... -0.3V to V_{VIO} + 0.3V
SCL to DGND ..... -0.3V to V_{VIO} + 0.3V
PGOOD to AGND ..... -0.3V to +2.0V
OUT Continuous RMS Current 8A
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 22.67mW/°C above +70°C) 1813.64mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W422D2+ 1
Outline Number	21-100293
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	44.11°C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	∅0.27 ±0.03
D	2.428 ±0.025
E	2.828 ±0.025
D1	2.00 BASIC
E1	2.40 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to Pb Free (+) package codes only.
7. Front - side finish can be either Black or Clear.

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TITLE	PACKAGE OUTLINE 42 BUMPS WLP PKG. 0.4 mm PITCH, W422D2+1		
APPROVAL	DOCUMENT CONTROL NO. 21-100293	REV. A	1/1

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = +7.6V, C_{FLY}/phase = 2x47µF, V_{VIO} = +1.8V, f_{SW} = 0.5MHz, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL INPUT SUPPLY						
Shutdown Supply Current	I_{SHDN}	EN = LOW, V_{IN} = 8.4V, V_{VIO} = 0V, T_A = +25°C		4	15	µA
Quiescent Current 1	I_{Q1}	V_{IN} = 8.4V, automatic mode		30		µA
Shutdown VIO Current	I_{SHDN_VIO}			0		µA
OUT Leakage Current	I_{LK_OUT}	V_{OUT} = 4.2V, AD_EN = 0		1.4		µA
INPUT UNDERVOLTAGE LOCKOUT						
Undervoltage-Lockout Threshold	V_{UVLO_R}	Rising (when V_{UVLO_F} = 4.1V)		4.9		V
	V_{UVLO_F}	Falling (OTP options: 4.1V, 4.3V, 4.5V, 4.7V)	3.977	4.1	4.223	
THERMAL ALARMS AND SHUTDOWN						
Thermal Alarm at +100°C	T_{INT100}	T_J rising, +15°C hysteresis		100		°C
Thermal Alarm at +120°C	T_{INT120}	T_J rising, +15°C hysteresis		120		°C
ENABLE INPUTS AND LOGIC						
EN Debounce Time	t_{EN}	EN_DEB[2:0] = 010		2		ms
Input LOW Level	V_{IL}				0.4	V
Input HIGH Level	V_{IH}		1.1			V
Input Leakage Current	I_{LK}			0.1		µA
Output High Leakage IRQB		V_{IRQB} = 5.5V, T_A = +85°C		0.1		µA
SWITCHED-CAPACITOR CONVERTER						
Input Operating Voltage Range	V_{IN}		V_{UVLO_F}		V_{IOVP}	V
Input OVP	V_{IOVP}	I^2C programmable 9.5V, 10.0V, 10.5V, 11.0V; default 9.5V		9.5		V
Output OVP	V_{OOVP}	Default = 5V		5		V
OCP Threshold	I_{OCP}	I^2C programmable from 4.2A to 11.6A with 200mA step; default 8.8A		8.8		A
OCP Accuracy	I_{OCP_ACC}	I_{OCP} = 8.8A	-10		+10	%
		In the entire I_{OCP} range	-16		+16	
OCP2 Offset	I_{OCP2}	I^2C programmable from 90mV to 240mV with 10mV step; default 240mV		240		mV
Soft-Start Current	I_{SS}	I^2C programmable options: 145mA, 290mA, 435mA, 580mA; default 580mA		580		mA
Soft-Start Current Accuracy	I_{SS_ACC}	I_{SS} = 290mA	-30		+30	%
Light Load Efficiency 1	η_{LIGHT1}	I_{OUT} = 1mA, V_{IN} = 7.4V		92		%
Light Load Efficiency 2	η_{LIGHT2}	I_{OUT} = 30mA, V_{IN} = 7.4V		97		%

Electrical Characteristics (continued)

(V_{IN} = +7.6V, C_{FLY}/phase = 2x47µF, V_{VIO} = +1.8V, f_{SW} = 0.5MHz, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak Efficiency	η_{PEAK}	V_{IN} = 7.4V, f_{SW} = 0.25MHz		98.5		%
Heavy Load Efficiency	η_{HEAVY}	I_{OUT} = 8A, V_{IN} = 7.4V		95		%
S1, S5 NMOS ON Resistance	R_{DSON}	IN to CFxP		11		mΩ
S2, S6 NMOS ON Resistance	R_{DSON}	OUT to CFxN		13		mΩ
S3, S7 NMOS ON Resistance	R_{DSON}	CFxP to OUT		13		mΩ
S4, S8 NMOS ON Resistance	R_{DSON}	CFxN to PGND		13		mΩ
Switching Frequency	f_{SW}	I^2C programmable options: 0.25MHz, 0.5MHz, 0.75MHz, 1MHz, 1.2MHz, 1.5MHz; when 0.5MHz is selected	0.47	0.5	0.53	MHz
Switching Frequency Dither Rate	f_{SW_DTHR}	I^2C programmable options: OFF, 3%, 6%, 12%; default 3%	-3		+3	%
Dead Time	t_{DDT}	S1 off to S3 on, S3 off to S1 on S2 off to S4 on, S4 off to S2 on S5 off to S7 on, S7 off to S5 on S6 off to S8 on, S8 off to S6 on		10		ns
SKIP Mode Threshold	I_{SKIP}	Enter to SKIP mode, 0.5A hysteresis		1.1		A
OUT Active Discharge Resistance	R_{AD_OUT}	Enable output active discharge; disable output		1k	1.5k	Ω
LINEAR REGULATORS						
AVDD Linear Regulator Output Voltage	V_{AVDD}		1.71	1.8	1.89	V
HVDD Linear Regulator Output Voltage				V_{OUT} + 1.8		V
INTERNAL PULLUP/DOWN RESISTANCE						
EN Pulldown Resistance	R_{PUPD}	Pulled down to AGND, when internal pulldown enabled		1.5		MΩ
SDA AND SCL I/O STAGE						
SCL, SDA Input Low Level		T_A = +25°C			0.3 x V_{VIO}	V
SCL, SDA Input High Level		T_A = +25°C	0.7 x V_{VIO}			V
SCL, SDA Input Hysteresis		T_A = +25°C		0.05 x V_{VIO}		V
SCL, SDA Logic Input Current		V_{SCL} = V_{SDA} = V_{VIO} = 1.8V	-10		+10	µA
SCL, SDA Input capacitance				10		pF

Electrical Characteristics (continued)

(V_{IN} = +7.6V, C_{FLY}/phase = 2x47µF, V_{VIO} = +1.8V, f_{SW} = 0.5MHz, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Output Low Voltage		Sinking 20mA			0.4	V
I²C COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns
I²C COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns
I²C COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz

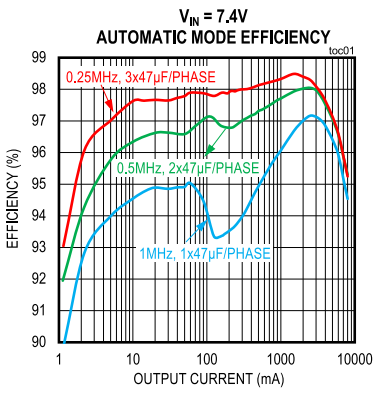
Electrical Characteristics (continued)

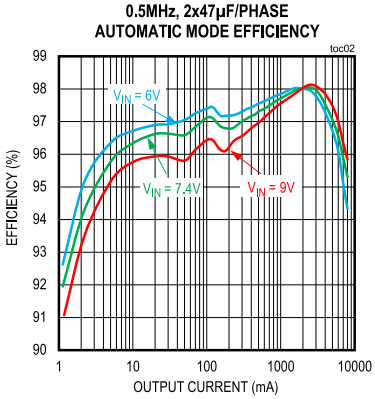
(V_{IN} = +7.6V, C_{FLY}/phase = 2x47µF, V_{VIO} = +1.8V, f_{SW} = 0.5MHz, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

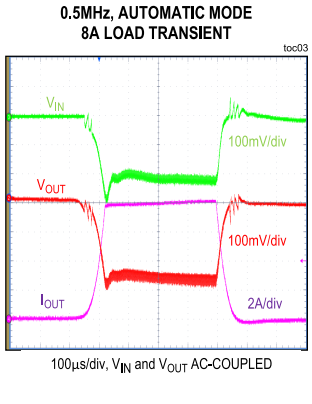
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns

Typical Operating Characteristics

(V_{IN} = +7.4V, V_{VIO} = +1.8V, C_{FLY}/phase = 2x47µF; F_{SW} = 0.5MHz, T_A = +25°C, unless otherwise noted.)



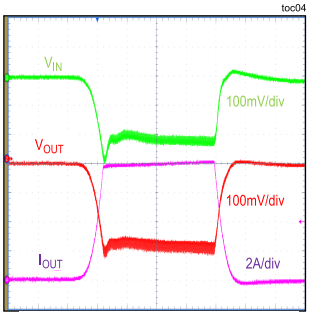




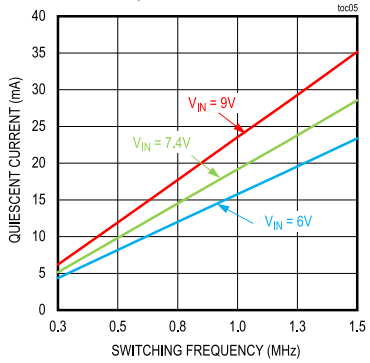
Typical Operating Characteristics (continued)

(V_{IN} = +7.4V, V_{VIO} = +1.8V, C_{FLY}/phase = 2x47µF; F_{SW} = 0.5MHz, T_A = +25°C, unless otherwise noted.)

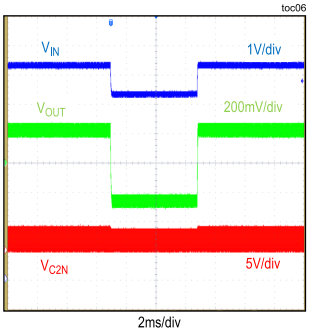
0.5MHz, FIXED FREQUENCY 8A LOAD TRANSIENT



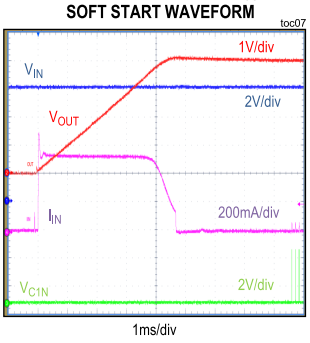
FIXED FREQUENCY MODE QUIESCENT CURRENT



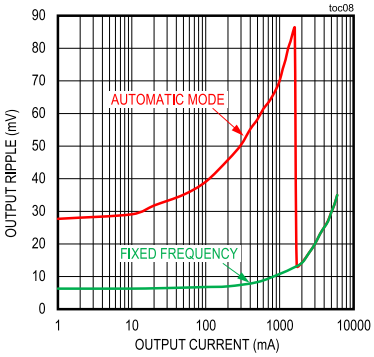
0.5MHz, 1A LOAD 1V LINE TRANSIENT



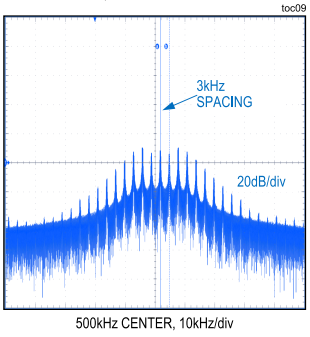
580mA SETTING, 470µF C_{OUT} SOFT START WAVEFORM



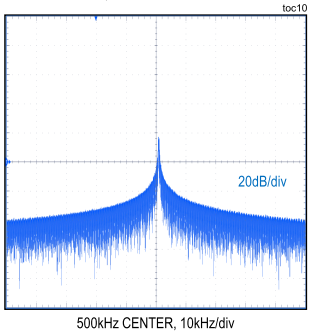
V_{IN} = 7.4V, 0.5MHz OUTPUT RIPPLE



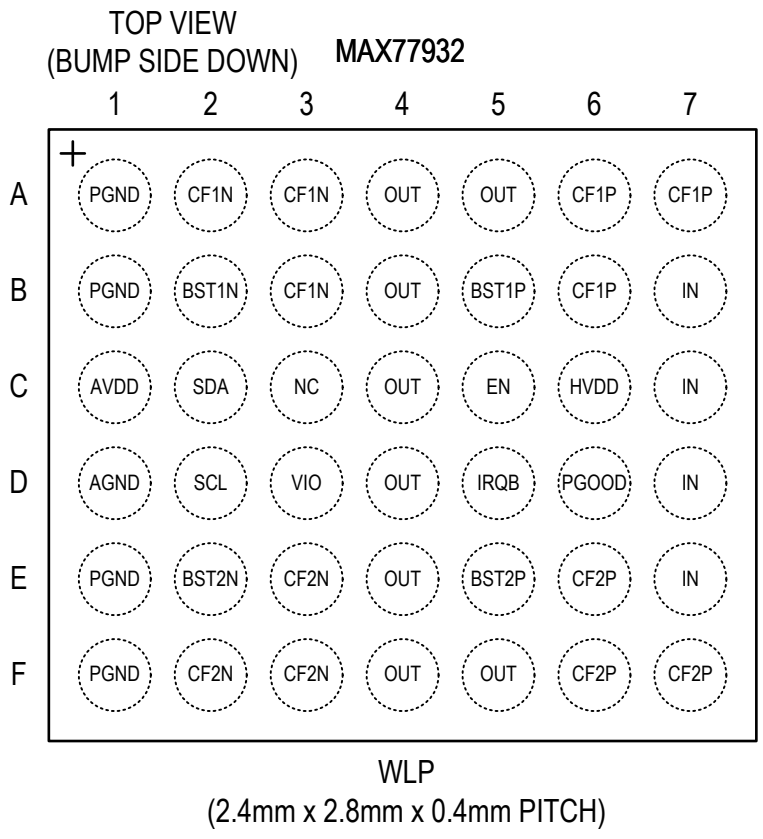
0.5MHz, 3% DITHERING FREQUENCY SPECTRUM



0.5MHz, DITHERING DISABLED FREQUENCY SPECTRUM



Pin Configuration



WLP
(2.4mm x 2.8mm x 0.4mm PITCH)

Pin Description

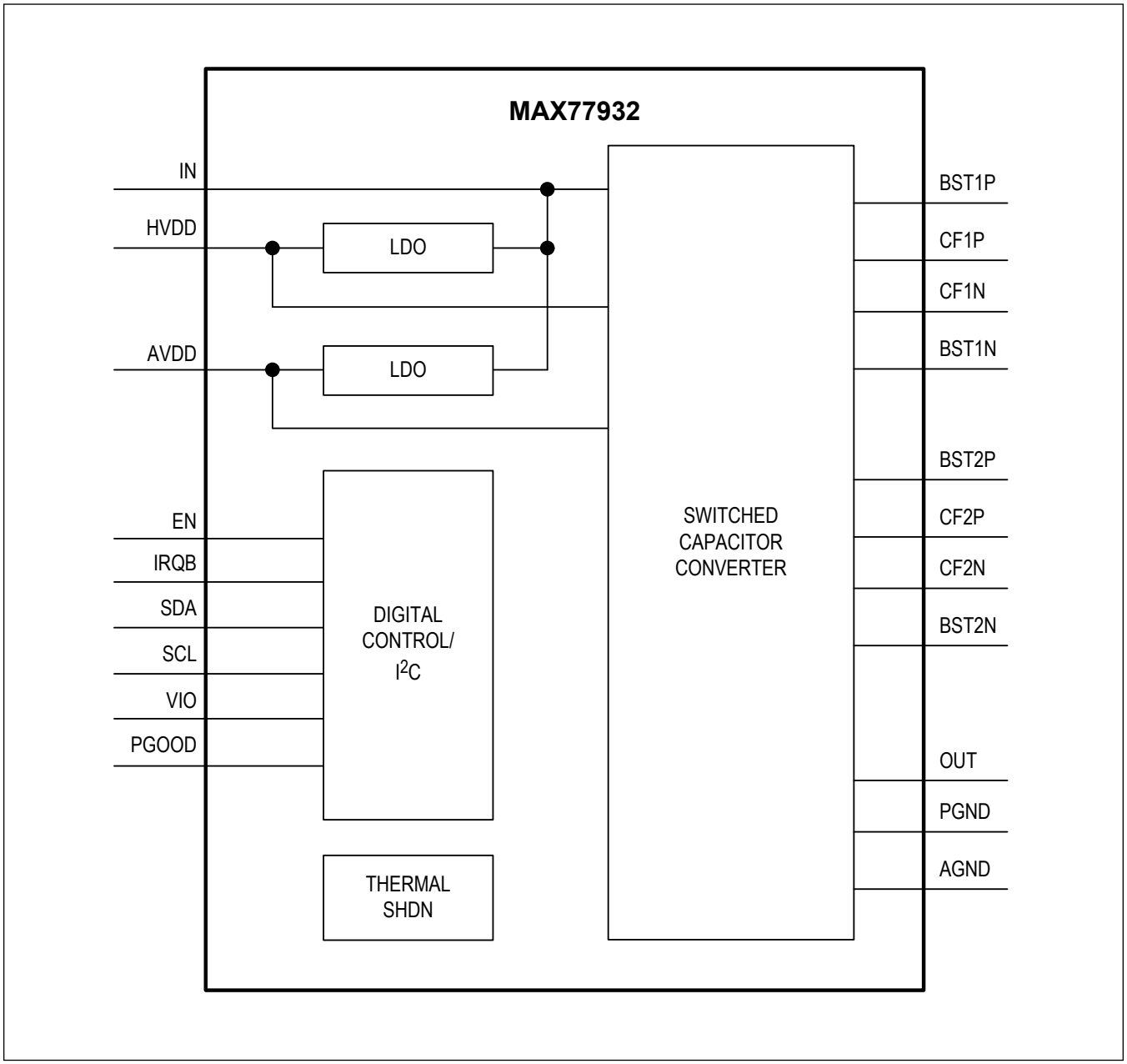
PIN	NAME	FUNCTION	TYPE
B7, C7, D7, E7	IN	The Power Input for the IC. Connect a 4.7µF capacitor between IN and PGND.	Power
B5	BST1P	Supply Input for Internal Gate Driver. Connect a 0.047µF bootstrap capacitor between BST1P and CF1P.	Analog
B2	BST1N	Supply Input for Internal Gate Driver. Connect a 0.047µF bootstrap capacitor between BST1N and CF1N.	Analog
E5	BST2P	Supply Input for Internal Gate Driver. Connect a 0.047µF bootstrap capacitor between BST2P and CF2P.	Analog
E2	BST2N	Supply Input for Internal Gate Driver. Connect a 0.047µF bootstrap capacitor between BST2N and CF2N.	Analog
A6, A7, B6	CF1P	Flying Capacitor Positive Terminal. Connecting 2 x 47µF capacitors between CF1P and CF1N is suggested.	Power
A2, A3, B3	CF1N	Flying Capacitor Negative Terminal	Power

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
E6, F6, F7	CF2P	Flying Capacitor Positive Terminal. Connecting 2 x 47µF capacitors between CF2P and CF2N is suggested.	Power
E3, F2, F3	CF2N	Flying Capacitor Negative Terminal	Power
A4, A5, B4, C4, D4, E4, F4, F5	OUT	Switched Capacitor Converter Output. Connect 2 x 10µF capacitors between OUT and PGND.	Power
A1, B1, E1, F1	PGND	Power Ground Pin	Power
C1	AVDD	1.8V Linear Regulator Output. Bypass to PGND with a 1µF capacitor. Do not apply an external load.	Analog
C6	HVDD	Linear Regulator Outputs V_{OUT} + 1.8V. Bypass to OUT with a 1µF capacitor. Do not apply an external load.	Analog
D1	AGND	Analog Ground Pin	Analog
D6	PGOOD	Power Good Indicator Output	Digital Output
C5	EN	Active-High Chip Enable Input	Digital Input
C3	NC	Do Not Connect	
D5	IRQB	Interrupt Output. Connect a 100kΩ pullup resistor between IRQB and VIO.	Digital Output
C2	SDA	I^2C Interface Data I/O	Digital I/O
D2	SCL	I^2C Interface Clock Input	Digital Input
D3	VIO	I/O Supply Voltage Input. Bypass to AGND with a 1µF capacitor.	Power

Functional Diagrams

Block Diagram



Detailed Description

In modern electronic devices, system level current consumption is ever increasing to fulfill the needs of more power-hungry end applications. This generally requires larger battery energy storage and thus higher power charging to keep the same charging time. For many low-voltage applications, it is sometimes advantageous to configure the battery source as a 2-series battery and use a highly-efficient 2-to-1 voltage converter to supply the system. With the same charging current, it is much faster to charge 2-series batteries than 2-parallel batteries because of the higher charger voltage. On the system side, the 2-to-1 converter acts as a current-doubler, thus delivering much higher current to the system. In this configuration, the system uses the 2-series battery as if it is 2-parallel, with the benefit of charging much faster. The switched-capacitor converter fits this requirement well by providing ultra-high DC-DC conversion efficiency and occupying less PCB design area.

Switched-Capacitor Converter (SCC)

The SCC is a type of DC-DC converter that only utilizes capacitors as the energy storage device. Compared to the buck converter which utilizes inductors, the switched-capacitor converter topology achieves higher efficiency with smaller solution size and lower cost.

The IC is an interleaved, dual-phase switched-capacitor converter. It generates an output voltage of $V_{IN}/2$ and is capable of supplying up to 8A output current. Each phase of the interleaved SCC operates with a fixed 50% duty cycle and reduces the ripple on the output voltage and current.

Enable or Disable the Device by EN

The IC can be enabled or disabled by digitally controlling the EN pin when VIO is kept low. The EN pin is active-high. Once EN is pulled high for longer than the EN debounce time, the IC initiates the soft-start operation. If the soft-start operation is successful, it is followed by the SCC fully-active state. The SCC turns off immediately when EN is low. To always enable the IC, tie the EN pin to VIN.

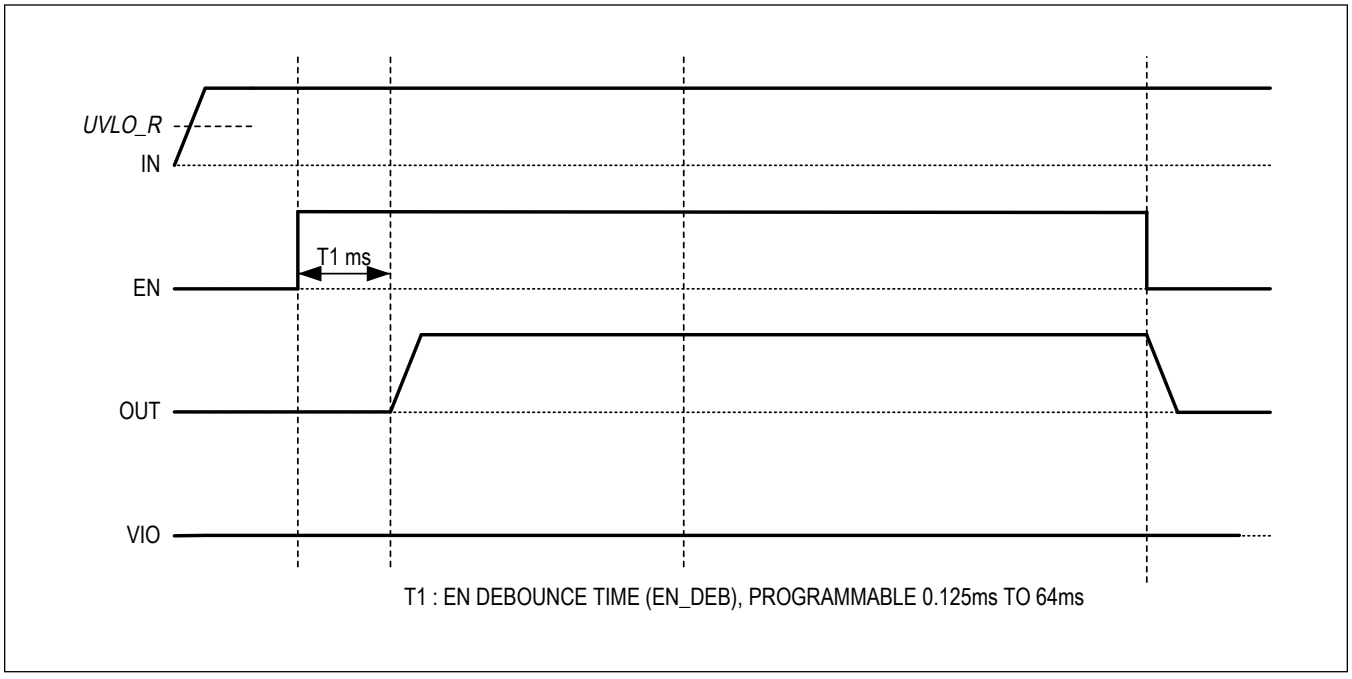


Figure 1. Enable Timing Waveform Without VIO

Enable or Disable the Device by EN and V_{IO}

The IC can be kept enabled by holding valid V_{IO}, and EN can be configured as push-button operation.

Once the EN pin is pulled high for longer than the EN debounce time, the IC initiates the soft-start followed by the SCC fully active. If V_{IO} is asserted and valid (V_{IO} > V_{IO}_OK threshold) IC before EN is released (means goes HIGH), then this holds the output. If EN goes LOW before V_{IO} is valid, the IC disables the output. After the output is on hold, the SCC can be turned off by turning off the V_{IO} regulator in the application system. The SCC turns off after OFF_DEB has passed after the moment V_{IO} goes low. Usually, V_{IO} is system IO voltage rail so this feature enables the device with a push-button easier and disables when the system is going to shutdown.

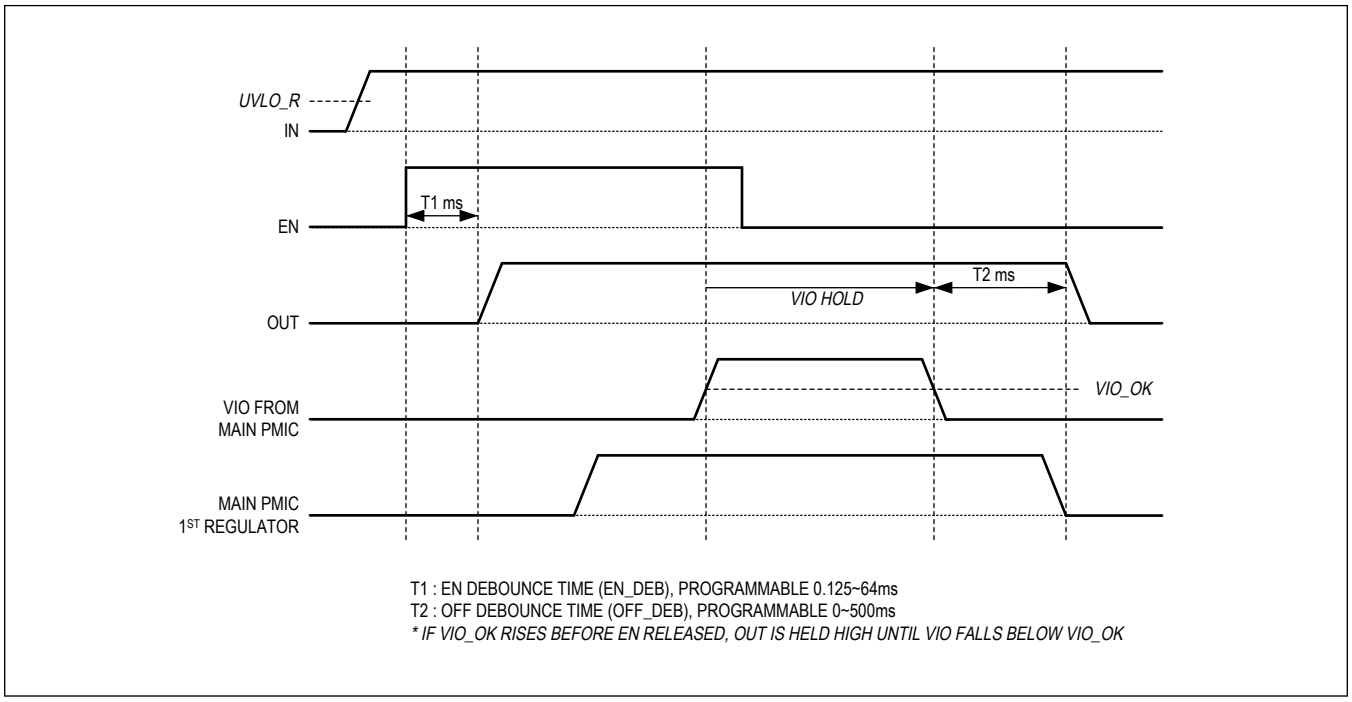


Figure 2. Enable Timing Waveform with VIO Hold

Enable by I^2C

Some applications can supply VIO before the IC output is enabled. In this case, the host microcontroller can enable the IC output by writing SCC_EN register to 0x1 through I^2C. The host can disable the output by writing the SCC_EN register to 0x0 through I^2C.

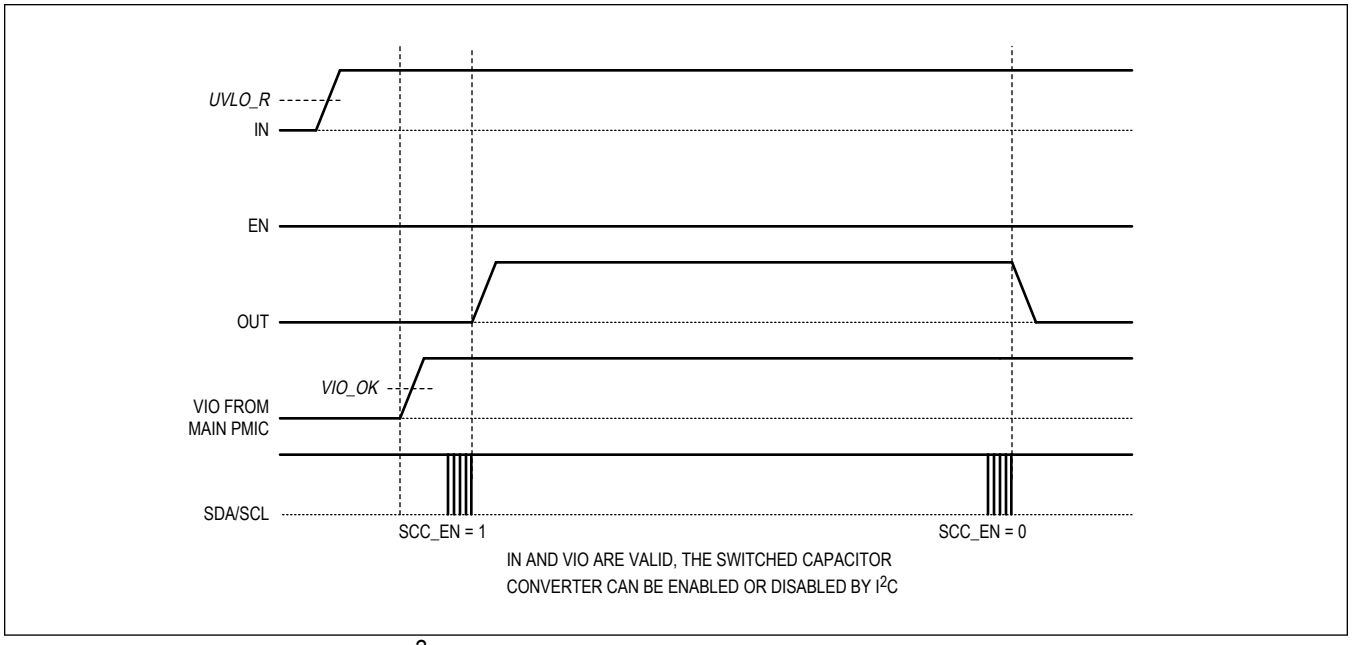


Figure 3. Enable Timing Waveform with I^2C Command

Startup and Soft-Start

During the device startup, the flying capacitors (C_{FLY}) are connected in parallel to the output capacitor. An internal current source charges the capacitors up to the voltage close to the target $V_{IN}/2$ in normal operation. The soft-start current can be configured through I^2C.

If the output voltage has not reached the voltage close to $V_{IN}/2$ within 120ms (default soft-start timeout setting), the IC generates the interrupt of SS_FLT_INT (Soft-Start Timer Fault Interrupt) and it returns to the STANDBY state. If the soft-start is successful, the SCC enters the normal operation.

PGOOD

PGOOD is a power good indicator output. After soft-start, the PGOOD pin outputs 1.8V. PGOOD remains at 1.8V as long as SCC is operating normally. If the PGOOD feature is used, an external RC filter with 1kΩ and 10nF is required to add at the PGOOD pin.

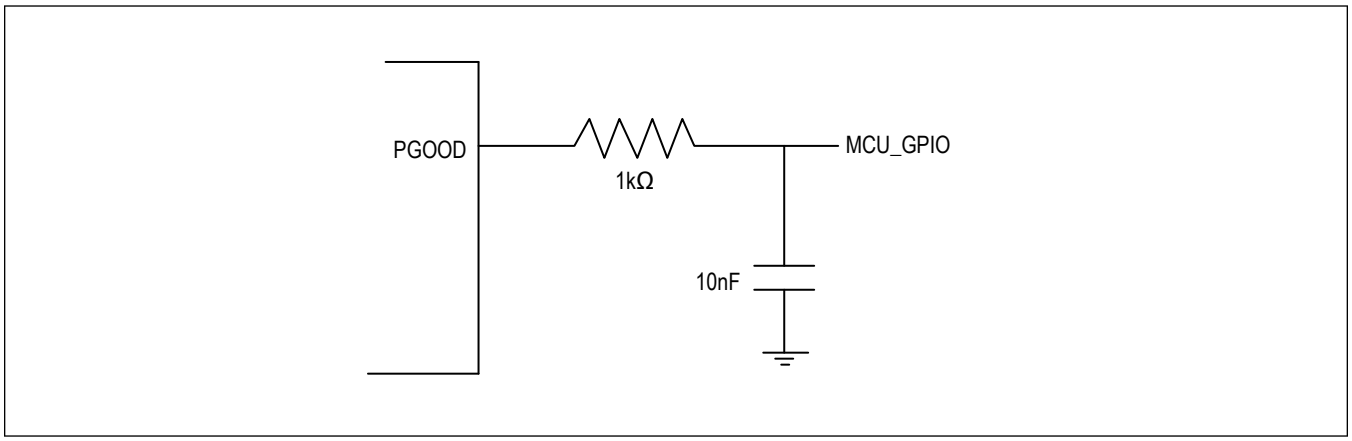


Figure 4. PGOOD Filter Example Circuit

Automatic Mode (Automatic-Skip Mode) and Fixed-Frequency Mode

When the IC enters normal operation, the SCC operates with 50% duty cycle. The switching frequency can be configured through the SCC_CFG2 register.

In the fixed-frequency mode, the SCC always operates, which provides unregulated $V_{IN}/2$ voltage at the OUT pin. When load current is low, the switcher consumption becomes significant enough to affect efficiency. To save power, the IC can enter the automatic-skip mode to only turn on the switcher when OUT voltage drops below the SKIP operation threshold.

To enable the IC to automatically enter SKIP mode when OUT load current is low, configure as SCC_CFG1.FIX_FREQ = 0. This is the default setting.

To configure the IC to always operate in fixed-frequency mode, configure as SCC_CFG1.FIX_FREQ = 1.

Operation detail for the SKIP mode is illustrated in Figure 5. When the output voltage is higher than REF_DCM, the IC enters into SKIP mode. In SKIP mode, the IC only switches when the output voltage drops below REF_SKIP. The IC stops switching when output voltage reaches the REF_SKIP_H threshold. When a heavy load is applied and the output falls down to the REF_CCM threshold, the IC enters the fixed-frequency mode. By doing it this way, it saves power in light loads and eventually provides higher efficiency at the entire load range as well as still maintaining the output close to $V_{IN}/2$.

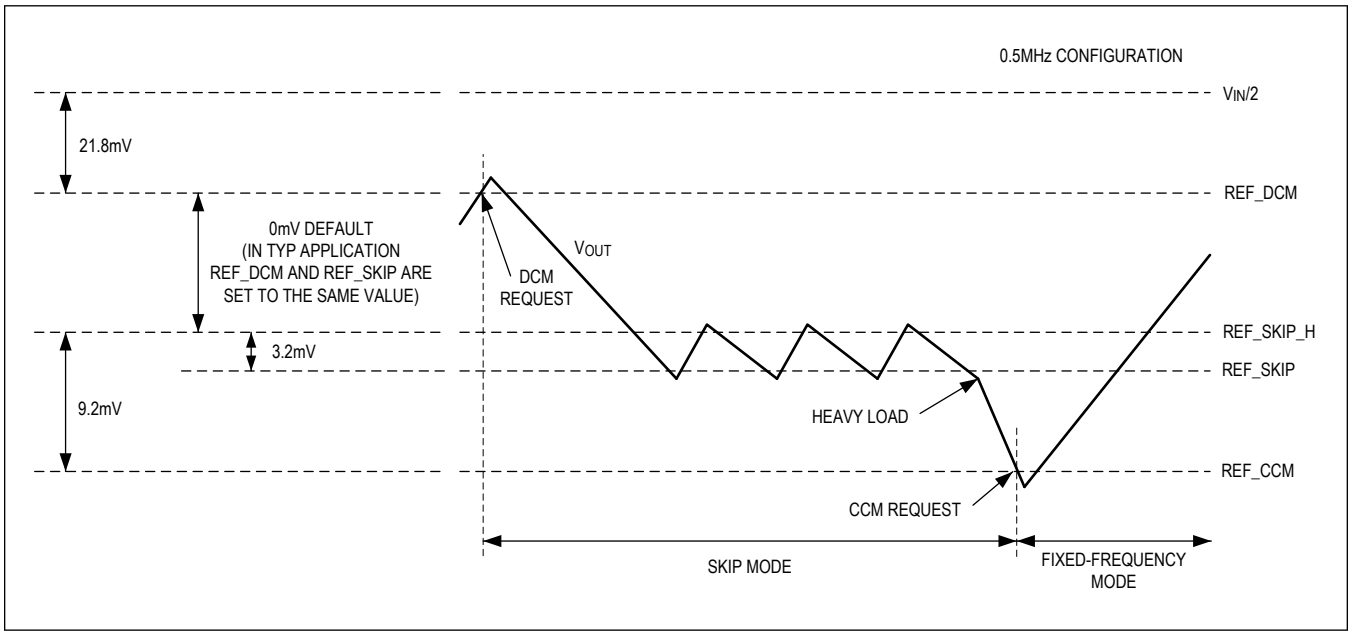


Figure 5. SKIP Mode Operation Diagram

Undervoltage Lockout

When V_{IN} falls below V_{UVLO_F} (typ 4.1V, OTP option), the IC enters into the shutdown state and UVLO forces the IC to a dormant state until V_{IN} rises above the V_{UVLO_R} threshold which allows the IC to be securely functional. V_{UVLO_F} is programmable through I^2C or OTP.

Frequency Dithering

Switched DC-DC converter operation can produce EMI emissions with a dominant peak frequency. Frequency dithering can reduce the peak emission of the converter by spreading the emission over a frequency band. The IC includes a frequency dithering feature applicable to all synthesized frequencies (from 0.25MHz up to 1.5MHz). Dithering can be disabled or enabled with different programmable spreads (3%, 6%, 12%).

Overcurrent Protections

During operation, the IC provides two layers of overcurrent protection. The output current is monitored for detecting overcurrent condition OCP1. The output voltage is sensed for faster short-circuit protection OCP2.

The IC protects and disables the output if the output current ≥ OCP1 or the output voltage ≤ $V_{IN}/2$ - OCP2.

OCP1 can be programmed from 4.2A to 9.6A in steps of 200mA, or additionally to 10.0A, 10.4A, 11.0A, or 11.6A through I^2C. OCP2 is programmable from 110mV to 240mV in steps of 10mV, or additionally set to OFF or 310mV through I^2C.

High Current Alarm

When I_{OUT} reaches 90% of I_{OCP} (progammable to 80% or 90% through I^2C), OC_ALM_INT interrupt bit and OC_ALM status bits are set.

When I_{OUT} decreases below 85% of the level of I_{OCP}, the OC_ALM status bit resets.

Thermal Alarms and Fault

The IC has a thermal protection circuit which monitors temperature on the die. If the die temperature exceeds +155°C, the IC enters the thermal shutdown state, and the T_SHDN_INT sets. After the thermal shutdown, if the die temperature reduces by +15°C, the thermal shutdown is deasserted and the user can re-enable the SCC again.

In addition to the +155°C threshold, there are additional comparators which trip at +100°C and +120°C. T_ALM1 and T_ALM2 interrupts are generated respectively.

Input Overvoltage Protection (IOVP)

When V_{IN} is higher than V_{IOVP} (I^2C programmable to 9.5V, 10.0V, 10.5V, or 11.0V), the switched-capacitor converter disables output and enters the standby mode.

State Diagram

Figure 6 shows the operation states and conditions to trigger state transitions.

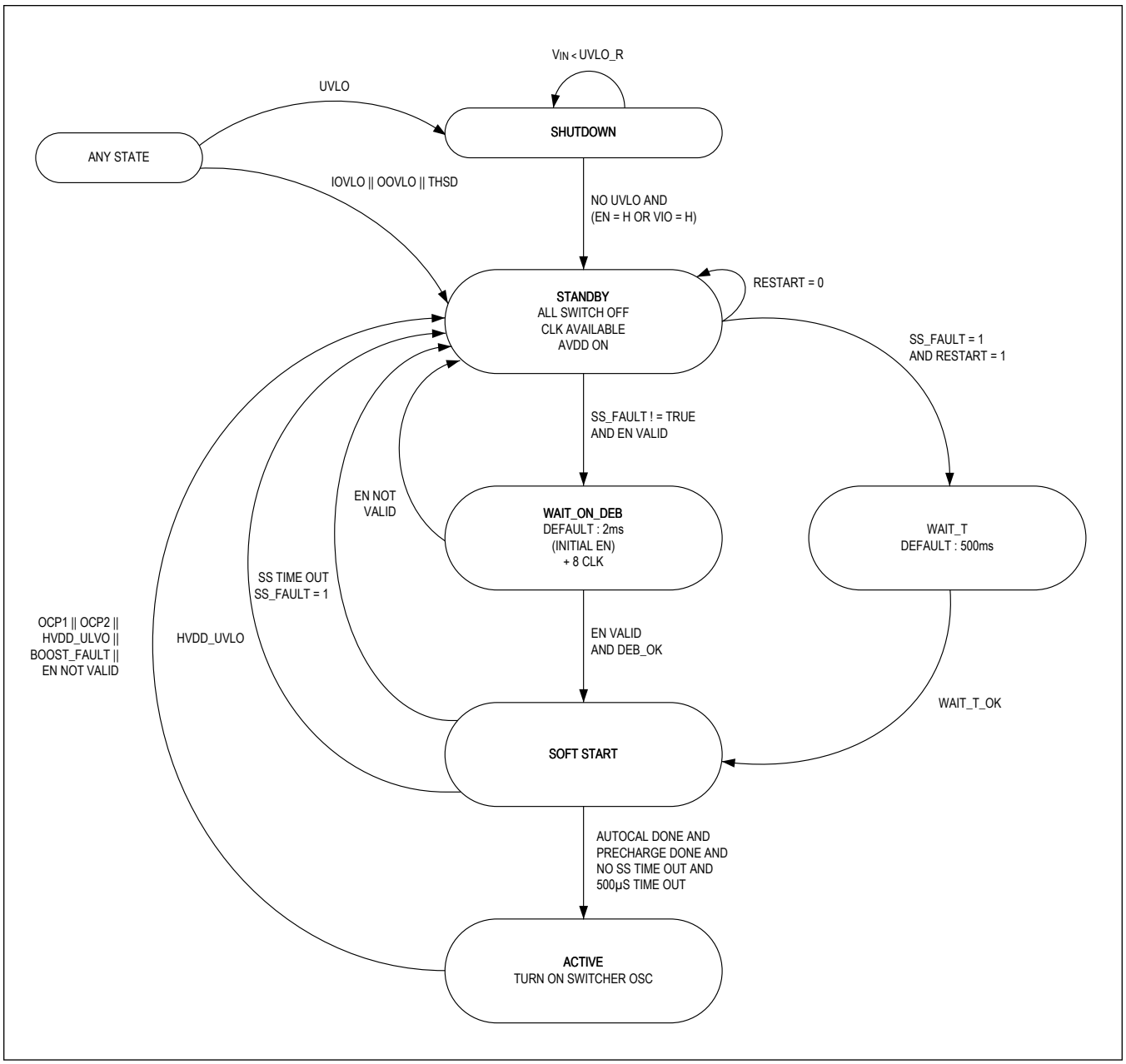


Figure 6. Device State Diagram

I²C Interface Description

Main I²C Interface

The IC acts as a Slave Transmitter/Receiver and has the following slave addresses:

Slave Address (7 bit) 110 1000

Slave Address (Write) 0xD0 1101 0000

Slave Address (Read) 0xD1 1101 0001

I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

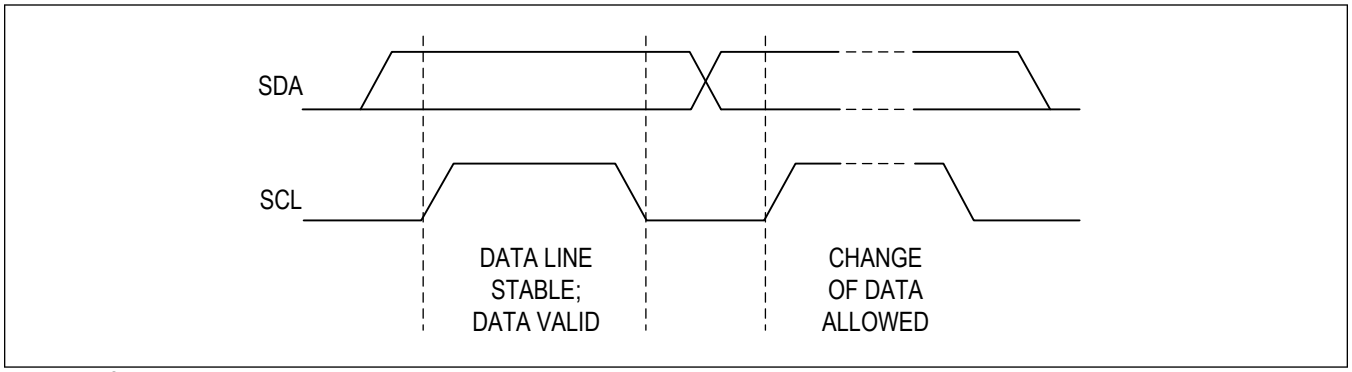


Figure 7. I²C Bit Transfer

I²C Start And Stop Conditions

Both SDA and SCL remain High when the bus is not busy. The Start (S) condition is defined as a high-to-low transition of the SDA while the SCL is high. The Stop (P) condition is defined as a low-to-high transition of the SDA while the SCL is high.

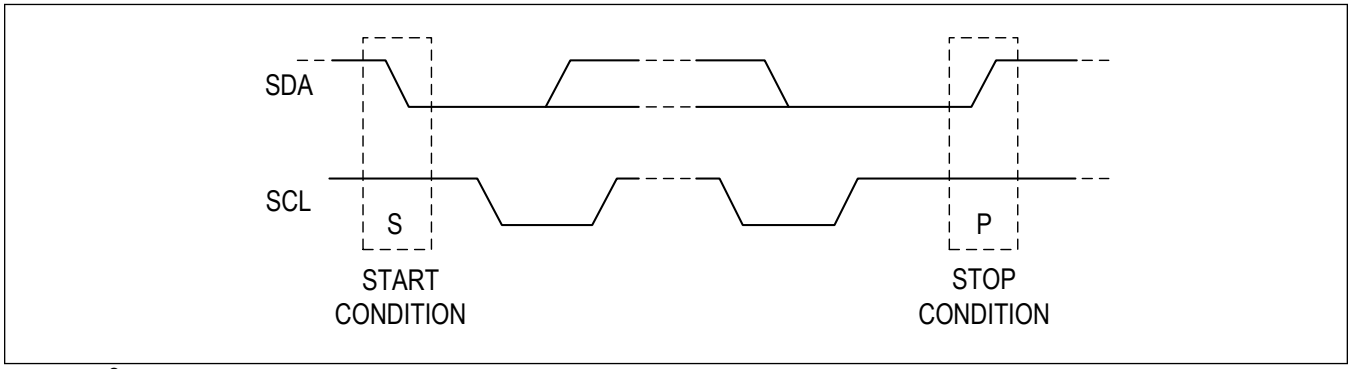


Figure 8. I²C Start and Stop

I²C System Configuration

A device on the I²C bus that generates a “message” is called a “Transmitter” and a device that receives the message is a “Receiver”. The device that controls the message is the “Master” and the devices that are controlled by the “Master” are called “Slaves”.

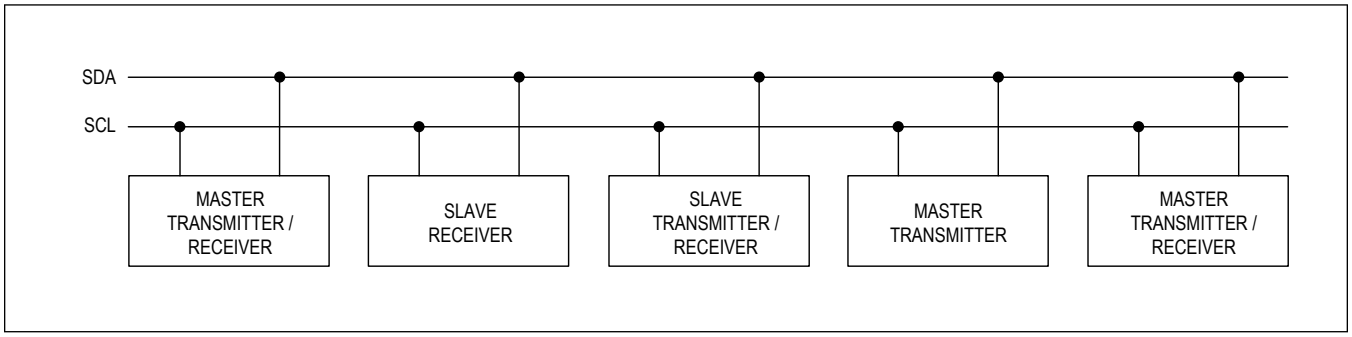


Figure 9. System Configurations

I²C Acknowledge

The number of data bytes between the start and stop conditions for the Transmitter and Receiver are unlimited.

Each 8-bit byte is followed by an Acknowledge bit. The Acknowledge bit is a high level signal put on SDA by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after each byte it receives. Also a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pulldown the SDA line during the acknowledge-clock pulse, so that the SDA line is stable and low during the high period of the acknowledge-clock pulse (setup and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a stop condition.

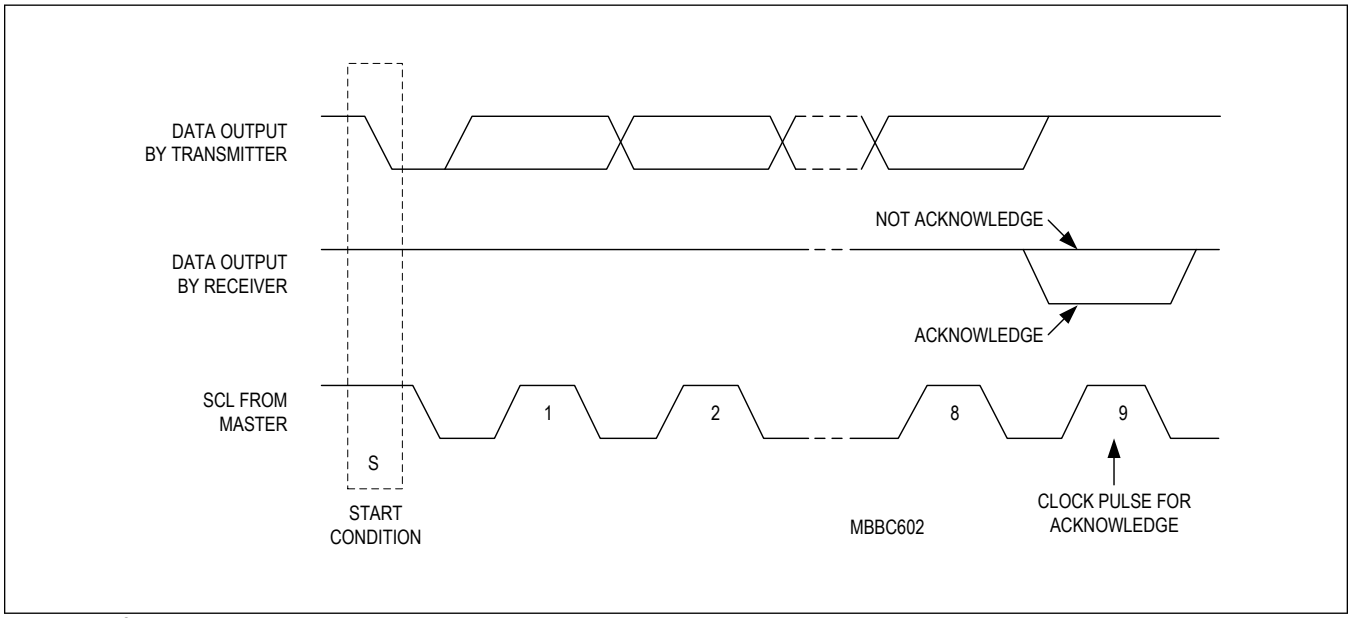


Figure 10. I²C Acknowledge

Master Transmits (Write Mode)

Use the following format when the master writes to the slave.

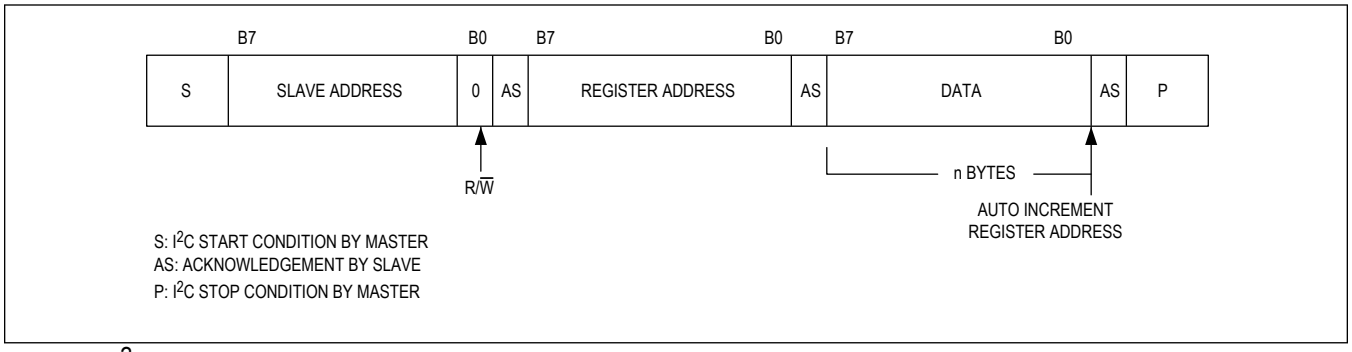


Figure 11. I²C Master Transmits

Master Reads After Setting Register Address (Write Register Address and Read Data)

Use the following format to read a specific register.

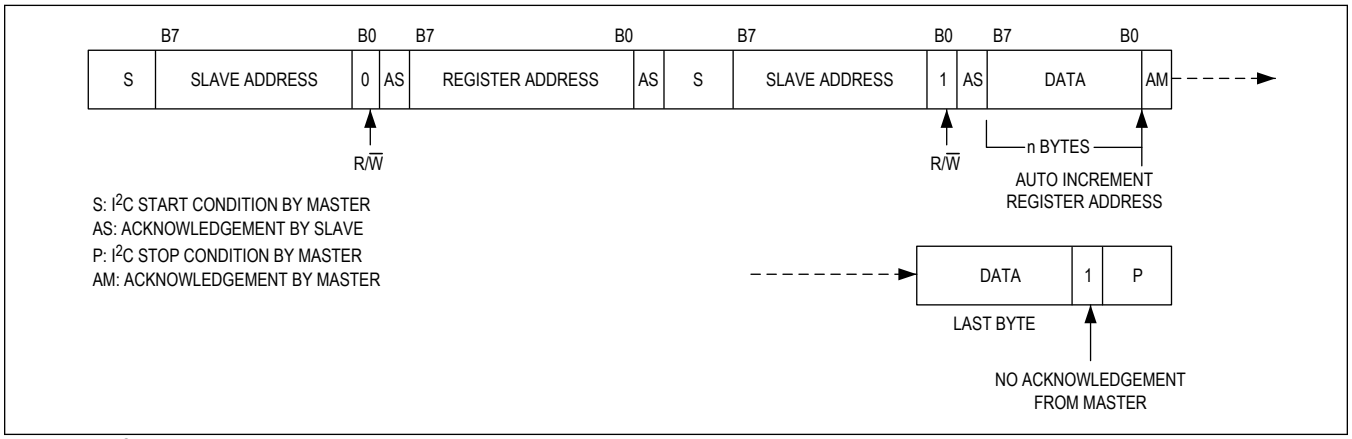


Figure 12. I²C Master Reads After Setting Register Address

Master Reads Register Data Without Setting Register Address (Read Mode)

Use the following format to read registers continuously starting from first address.

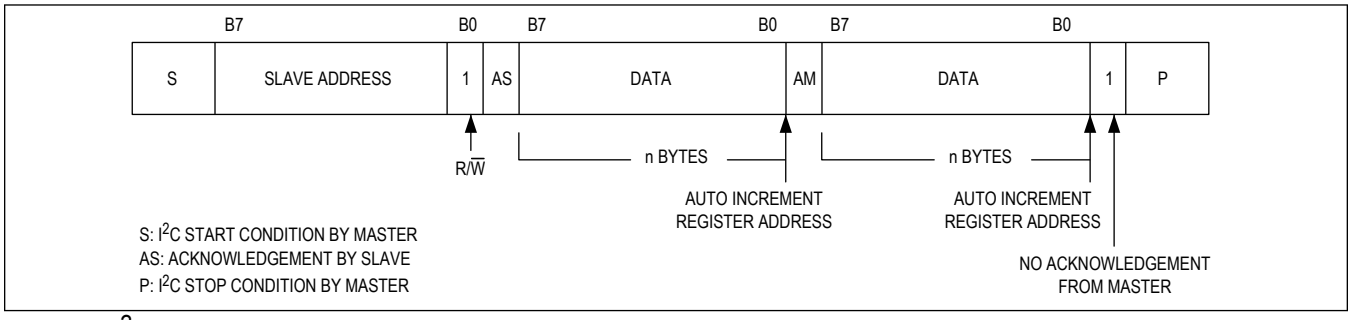


Figure 13. I²C Master Block Read

Register Map

Device Registers

ADDRESS	NAME	MSB							LSB
SCC									
0x00	INT_SRC[7:0]	IOVP_INT	OOVP_INT	OC_ALM_INT	OCP_INT	T_ALM1_INT	T_ALM2_INT	T_SHDN_INT	SS_FLT_INT
0x01	INT_SRC_M[7:0]	IOVP_M	OOVP_M	OC_ALM_M	OCP_M	T_ALM1_M	T_ALM2_M	T_SHDN_M	SS_FLT_M
0x02	STATUS[7:0]	IOVP	OOVP	OC_ALM	RSVD	T_ALM1	T_ALM2	T_SHDN	RSVD
0x03	SCC_EN[7:0]	RSVD[6:0]							SCC_EN
0x04	SCC_CFG1[7:0]	RSVD[2:0]			AD_EN	RSVD[2:0]			FIX_FREQ
0x05	SCC_CFG2[7:0]	SPR[1:0]		DTHR[1:0]		RSVD	FREQ[2:0]		
0x06	OVP_UVLO[7:0]	RSVD[1:0]		IOVP_R[1:0]		RSVD[1:0]		UVLO_F[1:0]	
0x07	OCP1[7:0]	OCP_ALM_TH	SPR[1:0]		OCP1[4:0]				
0x08	OCP2[7:0]	RSVD[3:0]				OCP2[3:0]			
0x09	OOVP[7:0]	RSVD[2:0]			OOVP_R[4:0]				
0x0A	SS_CFG[7:0]	RSVD[1:0]		SS_I[1:0]		RSVD	SS_T[2:0]		
0x0B	EN_CFG1[7:0]	RPUPD_EN	RSVD[3:0]				EN_DEB[2:0]		
0x0C	EN_CFG2[7:0]	DCVIO	RSVD	UVLO_F_DEB[1:0]		RSVD	OFF_DEB[2:0]		
0x14	I2C_CFG[7:0]	RSVD	–	–	PAIR0	RSVD[2:0]			HS_EXT_EN
0x15	CHIP REV[7:0]	OTP_VER[3:0]				CHIP_REV[3:0]			
0x16	DEVICE ID[7:0]	DEVICE_ID[7:0]							

Register Details

INT_SRC (0x00)

BIT	7	6	5	4	3	2	1	0
Field	IOVP_INT	OOVP_INT	OC_ALM_INT	OCP_INT	T_ALM1_INT	T_ALM2_INT	T_SHDN_INT	SS_FLT_INT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
IOVP_INT	7	Input Overvoltage Protection Interrupt	0b0 0b1: Input OVP interrupt has triggered.
OOVP_INT	6	Output Overvoltage Protection Interrupt	0b0 0b1: Output OVP interrupt has triggered.
OC_ALM_INT	5	Output Overcurrent Alarm Interrupt	0b0 0b1: Overcurrent alarm interrupt has triggered.

BITFIELD	BITS	DESCRIPTION	DECODE
OCP_INT	4	Output Overcurrent Protection Interrupt	0b0 0b1: Overcurrent protection has triggered.
T_ALM1_INT	3	Thermal Alarm 1 Interrupt	0b0 0b1: Overtemperature alarm 1 (100°C) has triggered.
T_ALM2_INT	2	Thermal Alarm 2 Interrupt	0b0 0b1: Overtemperature alarm 2 (120°C) has triggered.
T_SHDN_INT	1	Thermal Shutdown Interrupt	0b0 0b1: Thermal shutdown (155°C) interrupt has triggered.
SS_FLT_INT	0	Soft-Start Fault Interrupt	0b0 0b1: Soft-start fault interrupt has triggered.

INT_SRC_M (0x01)

BIT	7	6	5	4	3	2	1	0
Field	IOVP_M	OOVP_M	OC_ALM_M	OCP_M	T_ALM1_M	T_ALM2_M	T_SHDN_M	SS_FLT_M
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IOVP_M	7	Input Overvoltage Protection Interrupt Mask	0b0: Enable IOVP_INT 0b1: Mask IOVP_INT
OOVP_M	6	Output Overvoltage Protection Interrupt Mask	0b0: Enable OOVP_M 0b1: Mask OOVP_M
OC_ALM_M	5	Output Overcurrent Alarm Interrupt Mask	0b0: Enable OC_ALM_INT 0b1: Mask OC_ALM_INT
OCP_M	4	Output Overcurrent Protection Interrupt Mask	0b0: Enable OCP_INT 0b1: Mask OCP_INT
T_ALM1_M	3	Thermal Alarm 1 Interrupt Mask	0b0: Enable T_ALM1_INT 0b1: Mask T_ALM1_INT
T_ALM2_M	2	Thermal Alarm 2 Interrupt Mask	0b0: Enable T_ALM2_INT 0b1: Mask T_ALM2_INT
T_SHDN_M	1	Thermal Shutdown Interrupt Mask	0b0: Enable T_SHDN_INT 0b1: Mask T_SHDN_INT
SS_FLT_M	0	Soft-Start Fault Interrupt Mask	0b0: Enable SS_INT 0b1: Mask SS_INT

STATUS (0x02)

BIT	7	6	5	4	3	2	1	0
Field	IOVP	OOVP	OC_ALM	RSVD	T_ALM1	T_ALM2	T_SHDN	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
IOVP	7	Input Overvoltage Protection Status Bit	0b0: V_{IN} < 10.5V 0b1: V_{IN} ≥ 10.5V
OOVP	6	Output Overvoltage Status Bit	0b0: V_{OUT} < OVP_TH (default 5.6V) 0b1: V_{OUT} ≥ OVP_TH
OC_ALM	5	Output Overcurrent Alarm Status Bit	0b0: I_{OUT} < 90% of OCP_TH 0b1: I_{OUT} ≥ 90% of OCP_TH
RSVD	4	Reserved. Reads back 0.	
T_ALM1	3	Thermal Alarm 1 Status Bit	0b0: Junction temperature (T_J) < +100˚C 0b1: Junction temperature (T_J) ≥ +100˚C
T_ALM2	2	Thermal Alarm 2 Status Bit	0b0: Junction temperature (T_J) < +120˚C 0b1: Junction temperature (T_J) ≥ +120˚C
T_SHDN	1	Thermal Shutdown Status Bit	˚˚ 0b0: Junction temperature (T_J) < +155˚C 0b1: Junction temperature (T_J) ≥ +155˚C
RSVD	0	Reserved. Reads back 0.	

SCC_EN (0x03)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[6:0]							SCC_EN
Reset	0b0000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:1	Reserved. Reads back 0.	
SCC_EN	0	Switched-Capacitor Converter Enable Bit	0b0: Disable SCC 0b1: Enable SCC

SCC_CFG1 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			AD_EN	RSVD[2:0]			FIX_FREQ
Reset	0b000			0b1	0b000			0b0
Access Type	Write, Read			Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:5	Reserved. Reads back 0.	
AD_EN	4	Output Active Discharge Enable Bit	0b0: Disable Output Active Discharge 0b1: Enable Output Active Discharge
RSVD	3:1	Reserved. Reads back 0.	
FIX_FREQ	0	Fixed-Frequency Mode Enable Bit	0b0: Auto mode 0b1: Fixed-frequency mode

SCC_CFG2 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	SPR[1:0]		DTHR[1:0]		RSVD	FREQ[2:0]		
Reset	0x0		0b11		0b0	0b001		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:6	Reserved. Reads back 0.	
DTHR	5:4	Frequency Dithering Enable and Ratio	0b00: Minimum spread (3%) 0b01: Medium spread (6%) 0b10: Maximum spread (12%) 0b11: OFF
RSVD	3	Reserved. Reads back 0.	
FREQ	2:0	Switching Frequency Selection Bit	0b000: 0.25MHz 0b001: 0.50MHz 0b010: 0.75MHz 0b011: 1.0MHz 0b100: 1.2MHz 0b101: 1.5MHz 0b110: 1.5MHz 0b111: 1.5MHz

OVP_UVLO (0x06)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		IOVP_R[1:0]		RSVD[1:0]		UVLO_F[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved. Reads back 0.	
IOVP_R	5:4	Input Overvoltage-Protection Threshold (Rising)	0b00: 9.5V 0b01: 10.0V 0b10: 10.5V 0b11: 11.0V
RSVD	3:2	Reserved. Reads back 0.	
UVLO_F	1:0	Input UVLO (Falling) Threshold	0b00: 4.1V 0b01: 4.3V 0b10: 4.5V 0b11: 4.7V

OCP1 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	OCP_ALM_TH	SPR[1:0]		OCP1[4:0]				
Reset	0x1	0b00		0b10111				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OCP_ALM_TH	7	Output Overcurrent-Alarm Threshold	0b0: 80% of OCP 0b1: 90% of OCP
SPR	6:5	Reserved. Reads back 0.	
OCP1	4:0	Output Overcurrent (Layer1) Threshold	0b00000: 4.2A 0b00001: 4.4A 0b00010: 4.6A 0b00011: 4.8A 0b00100: 5.0A 0b00101: 5.2A 0b00110: 5.4A 0b00111: 5.6A 0b01000: 5.8A 0b01001: 6.0A 0b01010: 6.2A 0b01011: 6.4A 0b01100: 6.6A 0b01101: 6.8A 0b01110: 7.0A 0b01111: 7.2A 0b10000: 7.4A 0b10001: 7.6A 0b10010: 7.8A 0b10011: 8.0A 0b10100: 8.2A 0b10101: 8.4A 0b10110: 8.6A 0b10111: 8.8A 0b11000: 9.0A 0b11001: 9.2A 0b11010: 9.4A 0b11011: 9.6A 0b11100: 10.0A 0b11101: 10.4A 0b11110: 11.0A 0b11111: 11.6A

OCP2 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				OCP2[3:0]			
Reset	0b0000				0b1101			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:4	Reserved. Reads back 0.	

BITFIELD	BITS	DESCRIPTION	DECODE
OCP2	3:0	Output Overcurrent (Layer 2) Threshold	0b0000: 110mV 0b0001: 120mV 0b0010: 130mV 0b0011: 140mV 0b0100: 150mV 0b0101: 160mV 0b0110: 170mV 0b0111: 180mV 0b1000: 190mV 0b1001: 200mV 0b1010: 210mV 0b1011: 220mV 0b1100: 230mV 0b1101: 240mV 0b1110: 310mV 0b1111: OFF

OOVP (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			OOVP_R[4:0]				
Reset	0b000			0b10010				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:5	Reserved. Reads back 0.	
OOVP_R	4:0	Output Overvoltage-Protection Threshold (Rising)	0b0 0000: 4.150V 0b0 0001: 4.175V 0b0 0010: 4.200V 0b0 0011: 4.225V 0b0 0100: 4.250V 0b0 0101: 4.275V 0b0 0110: 4.300V 0b0 0111: 4.325V 0b0 1000: 4.350V 0b0 1001: 4.375V 0b0 1010: 4.400V 0b0 1011: 4.425V 0b0 1100: 4.450V 0b0 1101: 4.5V 0b0 1110: 4.6V 0b0 1111: 4.7V 0b1 0000: 4.8V 0b1 0001: 4.9V 0b1 0010: 5.0V 0b1 0011: 5.1V 0b1 0100: 5.2V 0b1 0101: 5.3V 0b1 0110: 5.4V 0b1 0111: 5.5V 0b1 1xxx: 5.5V

SS_CFG (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		SS_I[1:0]		RSVD	SS_T[2:0]		
Reset	0b00		0b11		0b0	0b001		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved. Reads back 0.	
SS_I	5:4	Soft-Start Current	0b00: 145mA 0b01: 290mA 0b10: 435mA 0b11: 580mA
RSVD	3	Reserved. Reads back 0.	
SS_T	2:0	Soft-Start Timeout	0b000: 0.06s 0b001: 0.12s 0b010: 0.19s 0b011: 0.25s 0b100: 0.31s 0b101: 0.38s 0b110: 0.44s 0b111: 0.50s

EN_CFG1 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	RPUPD_EN	RSVD[3:0]				EN_DEB[2:0]		
Reset	0b1	0b0000				0b010		
Access Type	Write, Read	Write, Read				Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RPUPD_EN	7	EN Input Pulldown Resistor Enable	0b0: Disable EN pulldown resistor. 0b1: Enable EN pulldown resistor.
RSVD	6:3	Reserved. Reads back 0.	
EN_DEB	2:0	EN Input Debounce Time	0b000: 0.125ms 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: 64ms

EN_CFG2 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	DCVIO	RSVD	UVLO_F_DEB[1:0]		RSVD	OFF_DEB[2:0]		
Reset	0b0	0b0	0b10		0b0	0b110		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
DCVIO	7	Write 0, Do not write 1	
RSVD	6	Reserved. Reads back 0.	
UVLO_F_DEB	5:4	Input UVLO (Falling) Debounce Time	0b00: 0s 0b01: 15µs 0b10: 108µs 0b11: 1ms
RSVD	3	Reserved. Reads back 0.	
OFF_DEB	2:0	OFF Debounce Time	0b000: No debounce time 0b001: 8ms 0b010: 16ms 0b011: 32ms 0b100: 64ms 0b101: 125ms 0b110: 250ms 0b111: 500ms

I2C_CFG (0x14)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	PAIR0	RSVD[2:0]			HS_EXT_EN
Reset	0b0	–	–	0b0	0b000			0b0
Access Type	Write, Read	–	–	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Reads back 0.	
PAIR0	4	I2C Sequential Write Mode Enable	0b0: Disable (Sequential Mode) 0b1: Enable
RSVD	3:1	Reserved. Reads back 0.	
HS_EXT_EN	0	I2C HS Mode Extension Enable	0b0: Disable HS mode extension 0b1: Enable HS mode extension

CHIP REV (0x15)

BIT	7	6	5	4	3	2	1	0
Field	OTP_VER[3:0]				CHIP_REV[3:0]			
Reset	0b1000				0b0010			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
OTP_VER	7:4	OTP Receipt Version
CHIP_REV	3:0	IC Revision

DEVICE ID (0x16)

BIT	7	6	5	4	3	2	1	0
Field	DEVICE_ID[7:0]							
Reset	0x60							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DEVICE_ID	7:0	Identification Number for Device When Communicating to Multiple I^2C Slaves

Applications Information

Capacitor Selection

The input capacitor, C_{IN}, reduces the current peaks drawn from the input power source and reduces switching noise in the device. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 4.7µF capacitor per phase is sufficient.

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. The recommended minimum output capacitance is 10µF per phase.

The flying capacitor, C_{FLY}, is required to have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For optimized efficiency, it is recommended to select 2x47µF for each phase.

Table 1. Suggested Input Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (Inch)	DIMENSIONS L x W x H (mm)
Murata	GRM188B31C475KAAJ	4.7	16	X5R	0603	1.6 x 0.8 x 0.8

Table 2. Suggested Flying Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (Inch)	DIMENSIONS L x W x H (mm)
Murata	GRM188R60J476ME15	47	6.3	X5R	0603	1.6 x 0.8 x 0.8
Murata	GRM219R60J476ME44	47	6.3	X5R	0805	2.0 x 1.2 x 0.85

Table 3. Suggested Output Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (Inch)	DIMENSIONS L x W x H (mm)
Murata	GRM155R60J106ME15	10	6.3	X5R	0402	1.0 x 0.5 x 0.5

Table 4. HVDD/AVDD Output Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (Inch)	DIMENSIONS L x W x H (mm)
Murata	GRM033R61A105ME15	1	10	X5R	0201	0.6 x 0.3 x 0.3

Table 5. Bootstrap Output Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (Inch)	DIMENSIONS L x W x H (mm)
Murata	GRM033R60J473KE15	0.047	6.3	X5R	0201	0.6 x 0.3 x 0.3

Layout Guide

Layout Guidelines

1. The C_{FLY} capacitors need to be placed as close as possible to the IC. This is a high priority.
2. All power traces must be as symmetrical as possible across two phases. For example, the CF1P is symmetrical with CF1N, and the OUT trace is symmetrical on both sides.
3. The guide has a power trace under the capacitor. For some designs, this is not allowed. If this is not allowed, keep the same flying capacitor location, and put a lot of via near the OUT pin of the IC to bring it down to another layer, and use multiple layers of the same trace to reinforce the OUT trace. Refer to the *MAX77932 EV kit* as an example.
4. For the AGND pin, **do not** directly tie to the top layer PGND. Run via through and tie it to the more stable system ground plane.
5. For inner pins, especially BST1P/N, BST2P/N, and HVDD, they need to connect through via. They are critical to the operation of the converter. Use a trace as wide as possible on the connecting layer to connect these pins, and the shortest path possible to the corresponding capacitors.

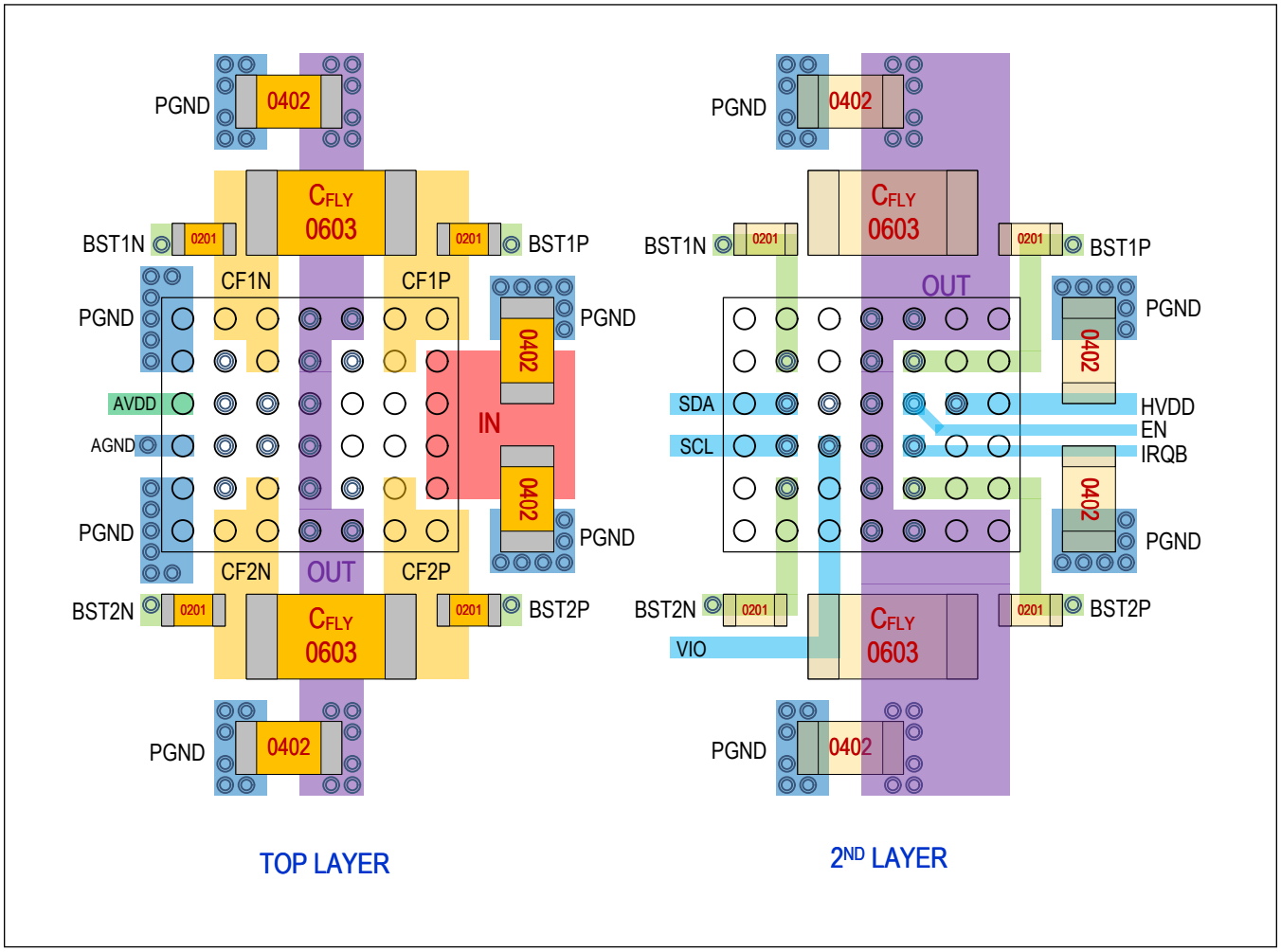
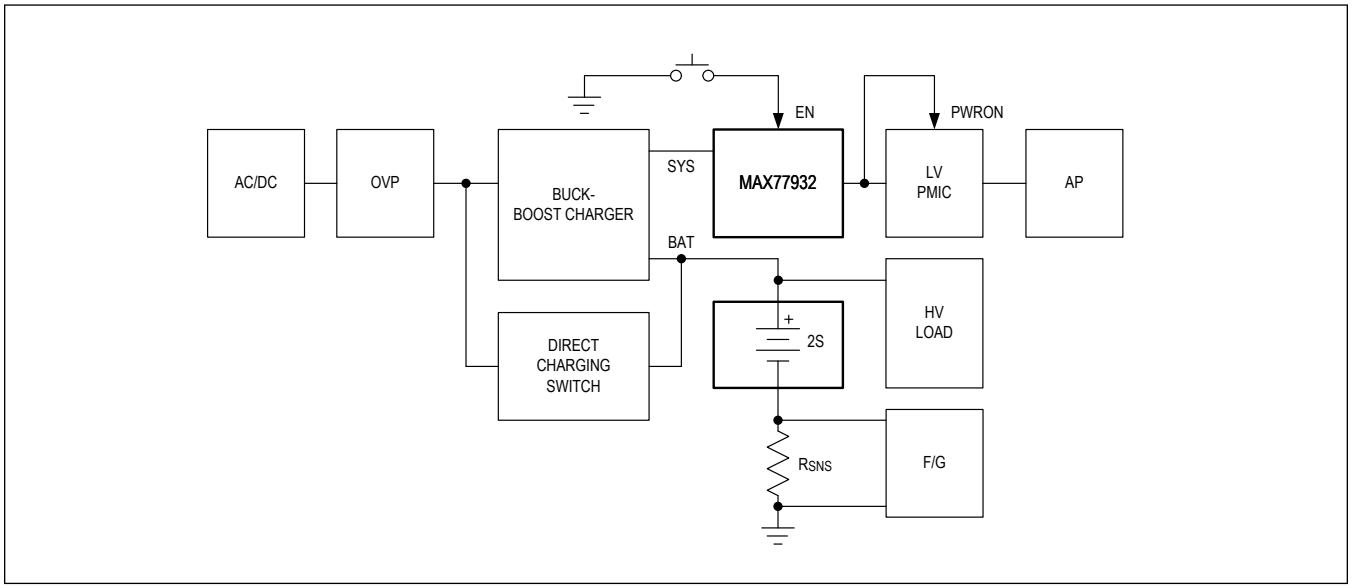


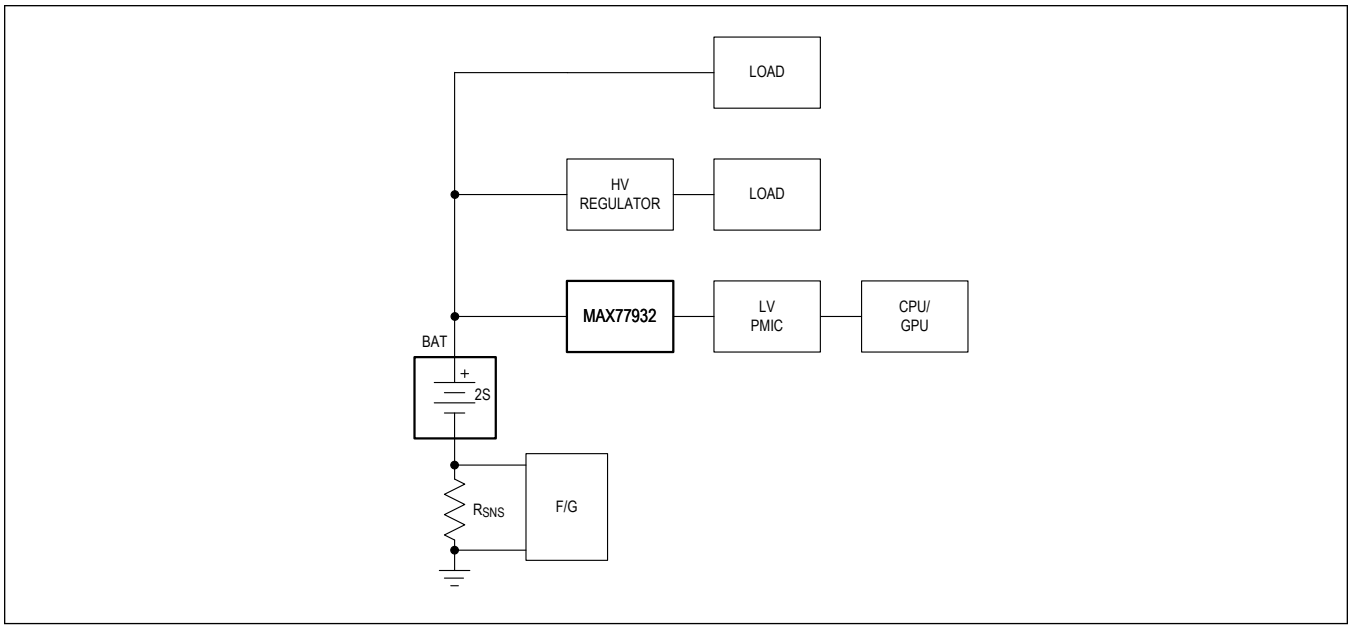
Figure 14. Layout Guide

Typical Application Circuits

System Block Diagram A



System Block Diagram B



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX77932CEWO+	-40°C to +85°C	42 WLP (0.4mm Pitch)
MAX77932CEWO+T	-40°C to +85°C	42 WLP (0.4mm Pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/20	Initial release	—