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# 3.15A USB Type-C Autonomous Charger with JEITA for 1-Cell Li-ion/LiFePO4 Batteries

**MAX77787**

## General Description

The MAX77787 is a standalone, 3.15A charger with integrated USB Type-C® CC detection and reverse-boost capability. The fast-charge current and termination voltage is easily configured with resistors. The IC operates with an input voltage of 4.5V to 13.4V and has a maximum input current limit of 3A. The IC also implements the adaptive input current limit (AICL) function that regulates the input voltage by reducing input current to prevent the voltage of a weak adapter from collapsing or folding back.

The USB Type-C Configuration Channel (CC) detection pins on the IC enable automatic USB Type-C power source detection and input current limit configuration without any software control as soon as the USB plug is inserted. The IC also integrates BC1.2 and proprietary adapter detection using the D+ and D- pins.

The IC offers reverse-boost capability up to 5.1V, 1.5A, that can be enabled with the ENBST pin, also BYP reverse-boost that can be enabled with the ENBST and STBY pin combination. The STAT pin indicates charging status, while the INOKB pin indicates valid input voltage. Charging can be stopped by pulling the CHGENB pin low.

The IC is equipped with a Smart Power Selector™ and a battery true-disconnect FET to control the charging and discharging of the battery or isolate the battery in case of a fault. The IC supports Li-ion batteries with JEITA compliance. It also has another option that supports $LiFePO_4$ batteries with non-JEITA compliance. The IC comes in a 2.758mm x 2.758mm, 0.4mm pitch, 6 x 6 wafer-level package (WLP) making it suitable for low-cost PCB assembly.

## Applications

- Mobile Point-of-Sale (mPOS) Terminals
- Portable Medical Devices
- Wireless Headphones
- GPS Trackers
- Charging Cradles for Wearable Devices
- Power Banks
- Mobile Routers

## Benefits and Features

- Up to 16V Protection
- 13.4V Maximum Input Operating Voltage
- 3.15A Maximum Charging Current
- 6A Discharge Current Protection
  - No Firmware or Communication Required
  - Integrated CC Detection for USB Type-C
  - Integrated BC1.2 Detection for Legacy SDP, DCP, CDP, and DCD Timeout
  - Integrated USB Detection for Common Proprietary Charger Types
  - Automatic Input Current Limit Configuration
  - Input Voltage Regulation with Adaptive Input Current Limit (AICL)
- 5.1V, 1.5A OTG Mode and BYP Reverse Boost
- Safety
  - Charge Safety Timer
  - JEITA Compliance with NTC Thermistor Monitor
  - Thermal Shutdown
- Pin Control of all Functions
  - Resistor Configurable Fast-Charge Current/Input Current Limit/Termination Voltage
  - ENBST Pin to Enable and Disable Reverse Boost
  - STAT Pin to Indicate Charging Status
  - INOKB Pin to Indicate Input Power-OK
  - CHGENB Pin to Enable and Disable Charging
  - STBY Pin to Support Suspend Mode
  - THM Pin to Monitor Thermistor
- Integrated Power Path
- Integrated Battery True-Disconnect FET
- 2.758mm x 2.758mm, 6 x 6 WLP

*USB Type-C is a registered trademark of USB Implementers Forum.*
*Smart Power Selector is a trademark of Maxim Integrated Products, Inc.*

*19-101433; Rev 1; 5/23*

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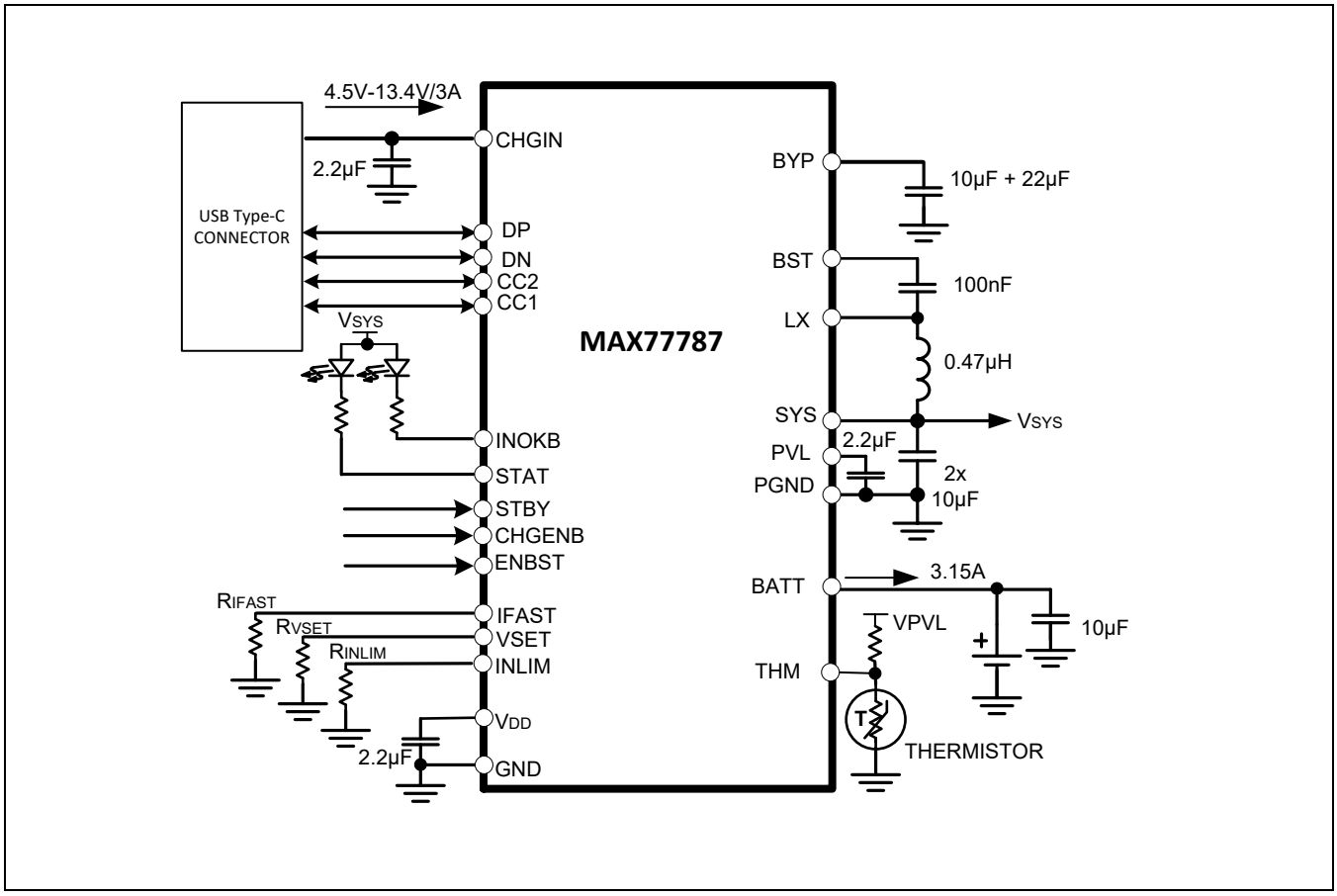
## Simplified Block Diagram



## Absolute Maximum Ratings

CHGIN to GND ..... -0.3V to +16.0V

BYP, LX to PGND ..... -0.3V to +16.0V

BATT, SYS, INOKB, STAT, ENBST, CHGENB, STBY to GND ..... -0.3V to +6.0V

BST to PVL ..... -0.3V to +16.0V

BST to LX ..... -0.3V to +2.2V

DN, DP to GND ..... -0.3V to +6.0V

CC1, CC2 to GND ..... -0.3V to +6.0V

THM, IFAST, VSET to GND ..... -0.3V to $V_{DD}$ + 0.3V

$V_{DD}$, PVL, INLIM to GND ..... -0.2V to +2.2V

$V_{CHGIN}$, BYP Continuous Current ..... $3.2A_{RMS}$

LX, PGND Continuous Current ..... $3.5A_{RMS}$

SYS, BATT Continuous Current ..... $4.5A_{RMS}$

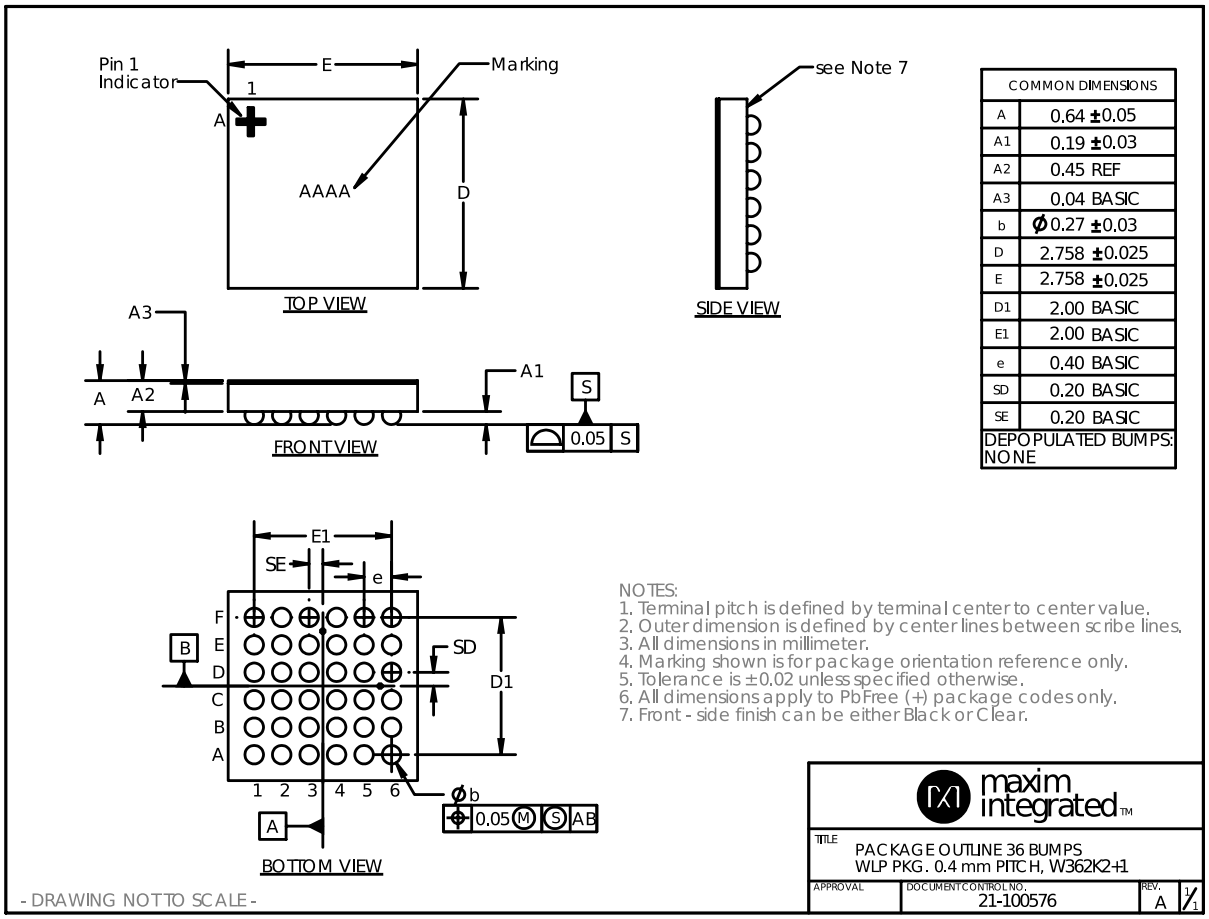
Operating Temperature Range ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| | |
|---|---|
| Package Code | W362K2+1 |
| Outline Number | 21-100576 |
| Land Pattern Number | Refer to *Application Note 1891* |
| **Thermal Resistance, Four-Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | 45.72°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | NA |




| COMMON DIMENSIONS | |
|---|---|
| A | 0.64 ±0.05 |
| A1 | 0.19 ±0.03 |
| A2 | 0.45 REF |
| A3 | 0.04 BASIC |
| b | ϕ0.27 ±0.03 |
| D | 2.758 ±0.025 |
| E | 2.758 ±0.025 |
| D1 | 2.00 BASIC |
| E1 | 2.00 BASIC |
| e | 0.40 BASIC |
| SD | 0.20 BASIC |
| SE | 0.20 BASIC |
| DEPOPULATED BUMPS: NONE | |

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ±0.02 unless specified otherwise.
6. All dimensions apply to Pb-Free (+) package codes only.
7. Front - side finish can be either Black or Clear.

maxim integrated™

TITLE: PACKAGE OUTLINE 36 BUMPS
WLP PKG. 0.4 mm PITCH, W362K2+1

APPROVAL | DOCUMENT CONTROL NO. 21-100576 | REV. A | 1/1

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

($V_{CHGIN}$ = 5.0V, Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **GENERAL ELECTRICAL CHARACTERISTICS** | | | | | | |
| Battery Only Quiescent Current | $I_{BATT\_Q}$ | USBC as UFP and BATT = SYS = 3.6V | | 30 | 50 | µA |
| **SWITCHING MODE CHARGER** | | | | | | |
| CHGIN Voltage Range | $V_{CHGIN}$ | Operating voltage (*Note 1*) | $V_{CHGIN\_UVLO}$ | | $V_{CHGIN\_OVLO}$ | V |
| CHGIN Overvoltage Threshold | $V_{CHGIN\_OVLO}$ | $V_{CHGIN}$ rising | 13.4 | 13.7 | 14 | V |
| CHGIN Overvoltage Threshold Hysteresis | $V_{CHGINH\_OVLO}$ | $V_{CHGIN}$ falling | | 300 | | mV |
| CHGIN to GND Minimum Turn-On Threshold Accuracy | $V_{CHGIN\_UVLO}$ | $V_{CHGIN}$ rising | 4.6 | 4.7 | 4.8 | V |
| CHGIN to SYS Minimum Turn-On Threshold | $V_{CHGIN2SYS}$ | $V_{CHGIN}$ rising | $V_{SYS}$ + 0.12 | $V_{SYS}$ + 0.20 | $V_{SYS}$ + 0.28 | V |
| CHGIN Adaptive Voltage Regulation Threshold Accuracy | $V_{CHGIN\_REG}$ | | 4.4 | 4.5 | 4.6 | V |
| CHGIN Current Limit Range | CHGIN_ILIM | Automatically configured after charger type detection | 0.5 | | 3.0 | A |
| | | Externally configured by $R_{INLIM}$ when charger type detected as unknown | 0.5 | | 3.0 | |
| CHGIN Minimum Current Threshold | $I_{ULO}$ | | | 65 | | mA |
| CHGIN Supply Current | $I_{IN}$ | $V_{CHGIN}$ = 5.0V, charger enabled, $V_{SYS}$ = $V_{BATT}$ = 4.5V, (No switching, battery charged) | | 2.7 | 4 | mA |
| | $I_{IN\_STBY}$ | DCDC off, STBY = H, $V_{CHGIN}$ = 5V | | 0.2 | | |
| | $I_{IN\_CHGENB}$ | CHGENB = H, $V_{CHGIN}$ = 5V | | 2.7 | | |
| $V_{CHGIN}$ Input Current Limit | $I_{INLIMIT}$ | Charger enabled, 500mA input current setting, $T_A$ = 0°C to +85°C | 423 | 460 | 500 | mA |
| | | Charger enabled, 1500mA input current setting, $T_A$ = 0°C to +85°C | 1300 | 1400 | 1500 | |
| | | Charger enabled, 3000mA input current setting, $T_A$ = 0°C to +85°C | 2600 | 2800 | 3000 | |
| CHGIN Self-Discharge Down to UVLO Time | $t_{INSD}$ | Time required for the charger input to cause CHGIN capacitor to decay from 6.0V to 4.3V | | 100 | | ms |
| CHGIN Input Self-Discharge Resistance | $R_{INSD}$ | | | 44 | | kΩ |
| CHGIN to BYP Resistance | $R_{CHGIN2BYP}$ | Bidirectional | | 20 | | mΩ |
| LX High Side Resistance | $R_{HS}$ | | | 41 | | mΩ |
| LX Low Side Resistance | $R_{LS}$ | | | 41 | | mΩ |
| BATT to SYS Dropout Resistance | $R_{BAT2SYS}$ | | | 13 | | mΩ |

($V_{CHGIN}$ = 5.0V, Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| CHGIN to BATT Dropout Resistance | $R_{CHGIN2BAT}$ | Calculation estimates a 0.04Ω inductor resistance ($R_L$)<br>$R_{CHGIN2BAT} = R_{CHGIN2BYP} + R_{HS} + R_L + R_{BAT2SYS}$ | | 114 | | mΩ |
| LX Leakage Current | | LX = PGND or BYP, $T_A$ = +25°C | | 0.01 | 10 | µA |
| | | LX = PGND or BYP, $T_A$ = +85°C | | 1 | | |
| BST Leakage Current | | BST = PGND or 1.8V, $T_A$ = +25°C | | 0.01 | 10 | µA |
| | | BST = PGND or 1.8V, $T_A$ = +85°C | | 1 | | |
| BYP Leakage Current | | $V_{BYP}$ = 5V, $V_{CHGIN}$ = 0V, LX = 0V, charger Disabled, $T_A$ = +25°C | | 0.01 | 10 | µA |
| | | $V_{BYP}$ = 5V, $V_{CHGIN}$ = 0V, LX = 0V, charger disabled, $T_A$ = +85°C | | 1 | | |
| SYS Leakage Current | | $V_{SYS}$ = 0V, $V_{BATT}$ = 4.2V, charger disabled, $T_A$ = +25°C | | 0.01 | 10 | µA |
| | | $V_{SYS}$ = 0V, $V_{BATT}$ = 4.2V, charger disabled, $T_A$ = +85°C | | 1 | | |
| Minimum ON Time | $t_{ON-MIN}$ | | | 75 | | ns |
| Minimum OFF Time | $t_{OFF-MIN}$ | | | 75 | | ns |
| Buck Current Limit | $I_{LIM}$ | | 5.16 | 6.0 | 6.84 | A |
| Reverse Boost Quiescent Current | | Non-switching: output forced 200mV above its target regulation voltage | | 2000 | | µA |
| Reverse Boost BYP Voltage in OTG Mode | $V_{BYP.OTG}$ | | 4.94 | 5.1 | 5.26 | V |
| CHGIN Output Current Limit | $I_{CHGIN.OTG.LIM}$ | 3.4V < $V_{BATT}$ < 4.5V, $T_A$ = 0°C to +85°C | 1500 | | 1725 | mA |
| Reverse Boost Output Voltage Ripple | | Discontinuous inductor current (i.e., skip mode) | | ±150 | | mV |
| | | Continuous inductor current | | ±150 | | |
| BATT Regulation Voltage Accuracy | | $T_A$ = +25°C, BATT regulation voltage (See *Table 5*) | -0.9 | -0.3 | +0.3 | % |
| BATT Regulation Voltage | $V_{BATREG}$ | Externally programmable by $R_{VSET}$ | 3.6 | | 4.55 | V |
| BATT Regulation Voltage Accuracy | | $T_A$ = 0°C to +85°C, BATT regulation voltage (See *Table 5*) | -1 | -0.3 | +0.5 | % |
| Fast-Charge Current Program Range | | External resistor programmable | 0.5 | | 3.15 | A |
| Fast-Charge Currents | $I_{FC}$ | $T_A$ = 0°C to +85°C, $V_{BATT}$ > $V_{SYSMIN}$, programmed for 3.0A | 2850 | 3000 | 3150 | mA |
| | | $T_A$ = 0°C to +85°C, $V_{BATT}$ > $V_{SYSMIN}$, programmed for 2.0A | 1900 | 2000 | 2100 | |
| | | $T_A$ = 0°C to +85°C, $V_{BATT}$ > $V_{SYSMIN}$, programmed for 0.5A | 465 | 500 | 535 | |
| Trickle Charge Threshold | $V_{TRICKLE}$ | $V_{BATT}$ rising | 3.0 | 3.1 | 3.2 | V |
| Precharge Threshold | $V_{PRECHG}$ | $V_{BATT}$ rising | 2.4 | 2.5 | 2.6 | V |
| Prequalification Threshold Hysteresis | $V_{PQ-H}$ | Applies to both $V_{TRICKLE}$ and $V_{PRECHG}$ | | 100 | | mV |

($V_{CHGIN}$ = 5.0V, Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Trickle Charge Current | $I_{TRICKLE}$ | $I_{TRICKLE}$ for termination voltage from 4.1V to 4.5V option; trickle charge is disabled for 3.6V option | 270 | 300 | 330 | mA |
| Precharge Charge Current | $I_{PRECHG}$ | | 40 | 55 | 80 | mA |
| Charger Restart Threshold | $V_{RSTRT}$ | | 50 | 100 | 150 | mV |
| Charger Restart Deglitch Time | | 10mV overdrive, 100ns rise time | | 130 | | ms |
| Top-Off Current Program Range | $I_{TO}$ | See *Table 6* | 50 | | 150 | mA |
| Top-Off Current Accuracy | $I_{TO}$ | $T_A$ = 0°C to +85°C, programmed for 150mA | 130 | 150 | 170 | mA |
| | | $T_A$ = 0°C to +85°C, programmed for 50mA | 25 | 50 | 75 | |
| Charge Termination Deglitch Time | $t_{TERM}$ | 2mV overdrive, 100ns rise/fall time | | 30 | | ms |
| Charger Soft-Start Time | $t_{SS}$ | | | 1.5 | | ms |
| BATT to SYS Reverse Regulation Voltage | $V_{BSREG}$ | $I_{BATT}$ = 10mA | | 70 | | mV |
| | | Load regulation during the reverse regulation mode | | 1 | | mV/A |
| Minimum SYS Voltage | $V_{SYSMIN}$ | For termination voltage from 4.1V to 4.5V | | 3.5 | | V |
| | | For 3.6V termination voltage | | 3.0 | | |
| Minimum SYS Voltage Accuracy | $V_{SYSMIN}$ | | -3 | | +3 | % |
| Prequalification Time | $t_{PQ}$ | Applies to both low-battery precharge and trickle modes | | 30 | | min |
| Fast-Charge Constant Current Plus Fast-Charge Constant Voltage Time | $t_{FC}$ | | | 6 | | hours |
| Top-Off Time | $t_{TO}$ | | | 30 | | s |
| Timer Accuracy | | | -20 | | +20 | % |
| Thermal Shutdown | $T_{SHDN}$ | $T_J$ rising (*Note 2*) | | 165 | | °C |
| Thermal Shutdown Hysteresis | | $T_J$ failing | | 15 | | °C |
| Junction Temperature Thermal Regulation Loop Setpoint Program Range | $T_{REG}$ | Junction temperature when charge current is reduced | | 130 | | °C |
| Thermal Regulation Gain | $AT_{JREG}$ | $I_{FC}$ = 3.15A | | -157.5 | | mA/°C |
| THM Threshold, COLD | THM_COLD | $V_{THM}/V_{PVL}$ rising, 1% hysteresis (thermistor temperature falling) | 72.5 | 74 | 75.5 | % |
| THM Threshold, COOL | THM_COOL | $V_{THM}/V_{PVL}$ rising, 1% hysteresis (thermistor temperature falling) | 63.5 | 65 | 66.5 | % |
| THM Threshold, WARM | THM_WARM | $V_{THM}/V_{PVL}$ falling, 1% hysteresis (thermistor temperature rising) | 31 | 32.5 | 34 | % |
| THM Threshold, HOT | THM_HOT | $V_{THM}/V_{PVL}$ falling, 1% hysteresis (thermistor temperature rising) | 21.5 | 23 | 24.5 | % |

($V_{CHGIN}$ = 5.0V, Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Charger Disable Threshold | $V_{CHGR\_EN}$ | $V_{THM}$/$V_{PVL}$ falling, 1% hysteresis (charger is disabled below this threshold) | 4.5 | 6 | 7.5 | % |
| THM Input Leakage Current | | $V_{THM}$ = GND or $V_{PVL}$; $T_A$ = +25°C | | 0.1 | 1 | µA |
| | | $V_{THM}$ = GND or $V_{PVL}$; $T_A$ = +85°C | | 0.1 | | |
| Battery Overcurrent Threshold | $I_{BOVCR}$ | | | 6.0 | | A |
| Battery Overcurrent Debounce Time | $t_{BOVRC}$ | | 6 | | | ms |
| Battery Overcurrent Retry | $t_{OCP\_RETRY}$ | | | 0.15 | | sec |
| Battery Overcurrent Protection Quiescent Current | $I_{BOVRC}$ | | | 3+$I_{BATT}$ /18040 | | µA |
| System Power-Up Current | $I_{SYSPU}$ | | 35 | 50 | 80 | mA |
| System Power-Up Voltage | $V_{SYSPU}$ | $V_{SYS}$ rising, 100mV hysteresis | 1.9 | 2.0 | 2.1 | V |
| **INOKB, STAT** | | | | | | |
| Logic Input Leakage Current | | | | 0.1 | 1 | µA |
| Output Low Voltage INOKB, STAT | | $I_{source}$ = 5mA, $T_A$ = +25°C | | | 0.4 | V |
| Output High Leakage INOKB, STAT | | $V_{SYS}$ = 5.5V, $T_A$ = +25°C | -1 | 0 | +1 | µA |
| | | $V_{SYS}$ = 5.5V, $T_A$ = +85°C | | 0.1 | | |
| **ENBST** | | | | | | |
| Logic Input Low Threshold | $V_{IL}$ | | | | 0.4 | V |
| Logic Input High Threshold | $V_{IH}$ | | 1.4 | | | V |
| Logic Input Leakage Current | $I_{ENBST}$ | V = 5.5V (including current through pulldown resistor) | | 24 | 60 | µA |
| Pulldown Resistor | $R_{ENBST}$ | | | 235 | | kΩ |
| **STBY** | | | | | | |
| Logic Input Low Threshold | $V_{IL}$ | | | | 0.4 | V |
| Logic Input High Threshold | $V_{IH}$ | | 1.4 | | | V |
| Logic Input Leakage Current | $I_{STBY}$ | V = 5.5V (including current through pulldown resistor) | | 24 | 60 | µA |
| Pulldown Resistor | $R_{STBY}$ | | | 235 | | kΩ |
| **CHGENB** | | | | | | |
| Logic Input Low Threshold | $V_{IL}$ | | | | 0.4 | V |
| Logic Input High Threshold | $V_{IH}$ | | 1.4 | | | V |
| Logic Input Leakage Current | $I_{CHGENB}$ | V = 5.5V (including current through pulldown resistor) | | 24 | 60 | µA |
| Pulldown Resistor | $R_{CHGENB}$ | | | 235 | | kΩ |
| **CHARGER DETECTION** | | | | | | |

($V_{CHGIN}$ = 5.0V, Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| BC1.2 State Timeout | $t_{TMO}$ | | 180 | 200 | 220 | ms |
| Data Contact Detect Time-Out | $t_{DCDtmo}$ | | 700 | 800 | 900 | ms |
| Proprietary Charger Debounce | $t_{PRDeb}$ | | 5 | 7.5 | 10 | ms |
| Primary to Secondary Timer | $t_{PDSDWait}$ | | 27 | 35 | 39 | ms |
| Charger Detection Debounce | $t_{CDDeb}$ | | 45 | 50 | 55 | ms |
| $V_{BUS64}$ Threshold | $V_{BUS64}$ | DP and DN pins. Threshold in percent of $V_{BUS}$ voltage; 3V < $V_{BUS}$ < 5.5V | 57 | 64 | 71 | % |
| $V_{BUS64}$ Hysteresis | $V_{BUS64\_H}$ | | | 0.015 | | V |
| $V_{BUS47}$ Threshold | $V_{BUS47}$ | DP and DN pins. Threshold in percent of $V_{BUS}$ voltage; 3V < $V_{BUS}$ < 5.5V | 43.3 | 47 | 51.7 | % |
| $V_{BUS47}$ Hysteresis | | | | 0.015 | | V |
| $V_{BUS31}$ Threshold | $V_{BUS31}$ | DP and DN pins. Threshold in percent of $V_{BUS}$ voltage; 3V < $V_{BUS}$ < 5.5V | 26 | 31 | 36 | % |
| $V_{BUS31}$ Hysteresis | | | | 0.015 | | V |
| $I_{WEAK}$ Current | $I_{WEAK}$ | | 0.01 | 0.1 | 0.5 | µA |
| $R_{DM\_DWN}$ Resistor | $R_{DM\_DWN}$ | | 14.25 | 20 | 24.8 | kΩ |
| $I_{DP\_SRC}$ Current | $I_{DP\_SRC}/I_{DCD}$ | Accurate over 0V to 2.5V | 7 | 10 | 13 | µA |
| $I_{DM\_SINK}$ Current | $I_{DM\_SINK}/I_{DAT\_SINK}$ | Accurate over 0.15V to 3.6V | 45 | 80 | 125 | µA |
| $V_{LGC}$ Threshold | $V_{LGC}$ | | 1.62 | 1.7 | 1.9 | V |
| $V_{LGC}$ Hysteresis | $V_{LGC\_H}$ | | | 0.015 | | V |
| $V_{DAT\_REF}$ Threshold | $V_{DAT\_REF}$ | | 0.25 | 0.32 | 0.4 | V |
| $V_{DAT\_REF}$ Hysteresis | $V_{DAT\_REF\_H}$ | | | 0.015 | | V |
| $V_{DN\_SRC}$ Voltage | $V_{DN\_SRC}/V_{SRC06}$ | Accurate over $I_{LOAD}$ = 0 to 200µA | 0.5 | 0.6 | 0.7 | V |
| $V_{DP\_SRC}$ Voltage | $V_{DP\_SRC}/V_{SRC06}$ | Accurate over $I_{LOAD}$ = 0 to 200µA | 0.5 | 0.6 | 0.7 | V |
| COMP2 Load Resistor | $R_{USB}$ | Load resistor on DP/DN | 3 | 6.1 | 12 | MΩ |
| **CC DETECTION** | | | | | | |
| CC Pin Voltage in DFP 1.5A Mode | $V_{CC\_PIN}$ | Measured at CC pins with 126kΩ load. IDFP1.5_CC enable and $V_{AVL}$ ≥ 2.5V | 1.85 | | | V |
| CC Pin Clamp Voltage | $V_{CC\_CLAMP}$ | 60µA ≤ $I_{CC\_}$ ≤ 600µA | | 1.1 | 1.32 | V |
| CC Pin Clamp Voltage (5.5V) | | $I_{CC\_}$ < 2mA | | 5.25 | 5.5 | V |
| CC UFP Pulldown Resistance | $R_{PD\_UFP}$ | | -10% | 5.1k | +10% | Ω |
| CC DFP 1.5A Current Source | $I_{DFP1.5\_CC}$ | | -8% | 180 | +8% | µA |
| CC RA RD Threshold | $V_{RA\_RD0.5}$ | | 0.15 | 0.2 | 0.25 | V |
| CC UFP 0.5A RD Threshold | $V_{UFP\_RD0.5}$ | | 0.61 | 0.66 | 0.7 | V |
| CC UFP 0.5A RD Hysteresis | $V_{UFP\_RD0.5\_H}$ | | | 0.015 | | V |

($V_{CHGIN}$ = 5.0V, Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| CC UFP 1.5A RD Threshold | $V_{UFP\_RD1.5}$ | | 1.16 | 1.23 | 1.31 | V |
| CC UFP 1.5A RD Hysteresis | $V_{UFP\_RD1.5\_H}$ | | | 0.15 | | V |
| CC Pin Power-Up Time | $t_{ClampSwap}$ | Max time allowed from removal of voltage clamp till 5.1k resistor attached | | | 15 | ms |
| CC Detection Debounce | $t_{CCDeb}$ | | 100 | 119 | 200 | ms |
| USB Type-C Debounce | $t_{PDDeb}$ | | 10 | 15 | 20 | ms |
| USB Type-C Quick Debounce | $t_{QDeb}$ | | 0.9 | 1 | 1.1 | ms |

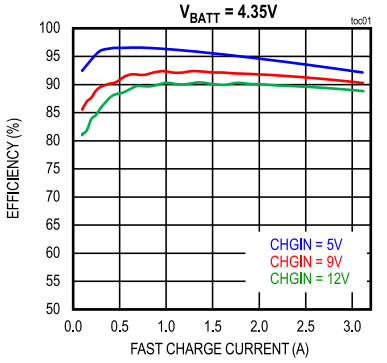
**Note 1:** The CHGIN input must be less than $V_{CHGIN\_OVLO}$ and greater than both $V_{CHGIN\_UVLO}$ and $V_{CHGIN2SYS}$ for the charger to turn on.

**Note 2:** $T_{SHDN}$ only sets charger from charging to buck mode, $T_{SHDN}$ is invalid in reverse-boost mode

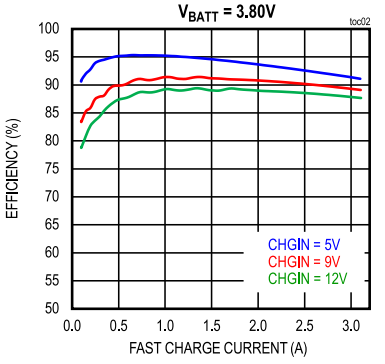
## Typical Operating Characteristics

($V_{CHGIN}$ = 5V, $V_{BATT}$ = 3.8V, $T_A$ = +25°C, unless otherwise noted.)

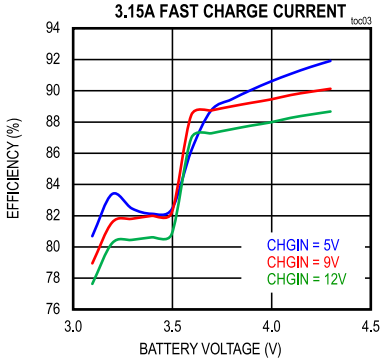
EFFICIENCY vs. FAST CHARGE CURRENT
$V_{BATT}$ = 4.35V



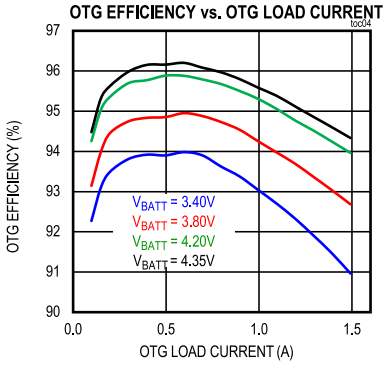

EFFICIENCY vs. FAST CHARGE CURRENT
$V_{BATT}$ = 3.80V



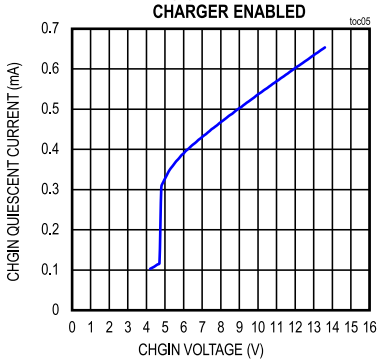

EFFICIENCY vs. BATTERY VOLTAGE
3.15A FAST CHARGE CURRENT



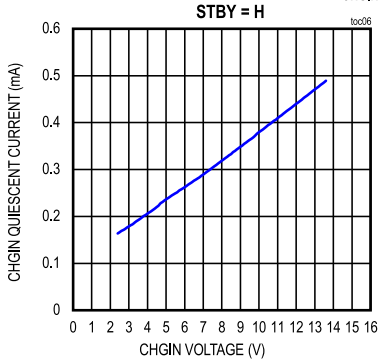

OTG EFFICIENCY vs. OTG LOAD CURRENT



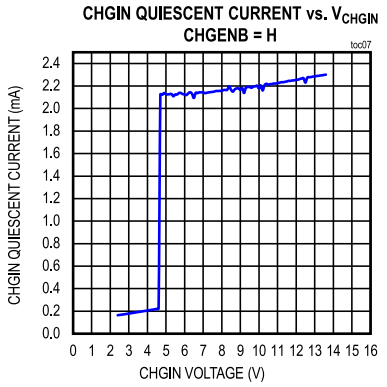

CHGIN QUIESCENT CURRENT vs. $V_{CHGIN}$
$V_{SYS}$ = $V_{BATT}$ = 4.5V
CHARGER ENABLED



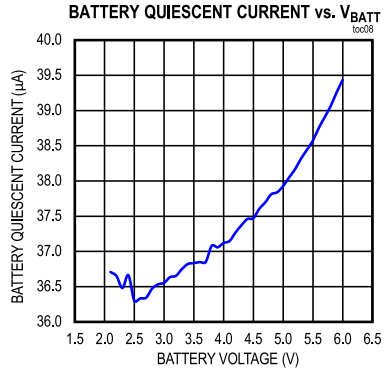

CHGIN QUIESCENT CURRENT vs. $V_{CHGIN}$
STBY = H



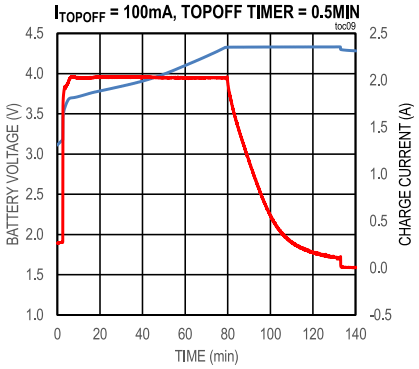

CHGIN QUIESCENT CURRENT vs. $V_{CHGIN}$
CHGENB = H




BATTERY QUIESCENT CURRENT vs. $V_{BATT}$

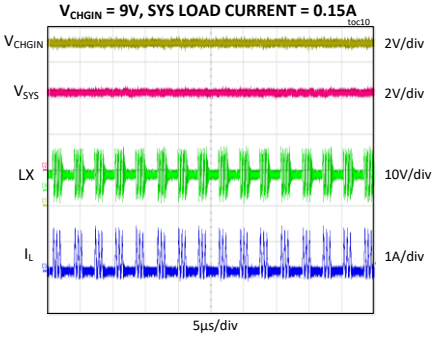



CHARGE PROFILE
$V_{CHGIN}$ = 5V, $I_{FAST}$ = 2A, $V_{TERM}$ = 4.35V
$I_{TOPOFF}$ = 100mA, TOPOFF TIMER = 0.5MIN

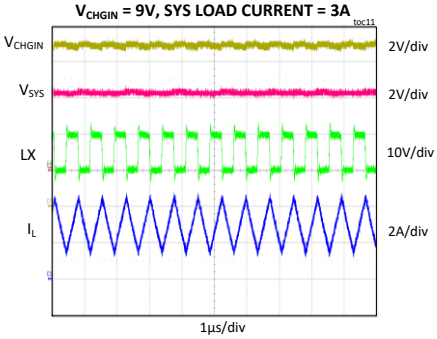


($V_{CHGIN}$ = 5V, $V_{BATT}$ = 3.8V, $T_A$ = +25°C, unless otherwise noted.)

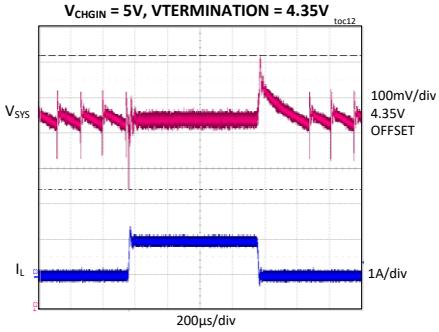
**SWITCHING WAVEFORM**
**$V_{CHGIN}$ = 9V, SYS LOAD CURRENT = 0.15A**



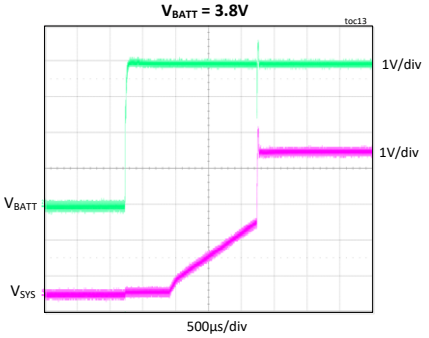

**SWITCHING WAVEFORM**
**$V_{CHGIN}$ = 9V, SYS LOAD CURRENT = 3A**



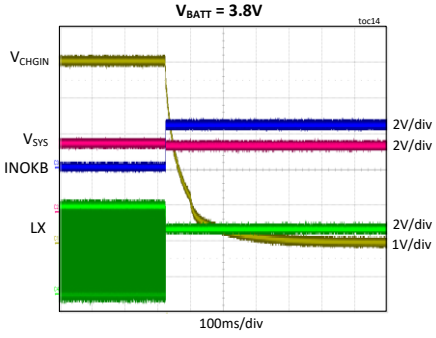

**SYS LOAD TRANSIENT RESPONSE**
**$V_{CHGIN}$ = 5V, VTERMINATION = 4.35V**



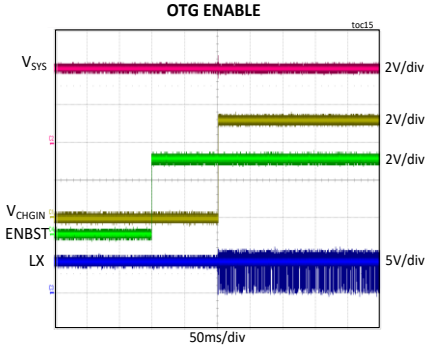

**INPUT INSERTION**
**$V_{BATT}$ = 3.8V**



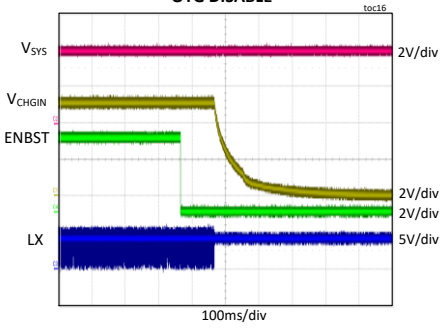

**CHGIN REMOVAL WHILE CHARGING**
**$V_{BATT}$ = 3.8V**



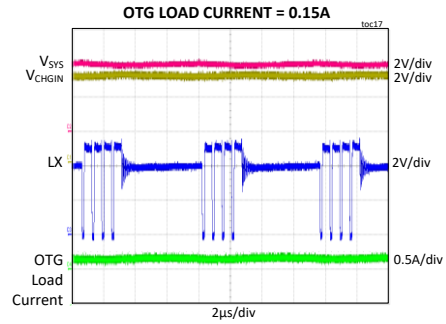

**OTG ENABLE**



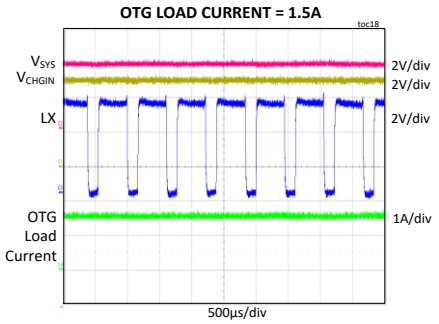

**OTG DISABLE**




**BOOST SWITCHING WAVEFORM**
**OTG LOAD CURRENT = 0.15A**

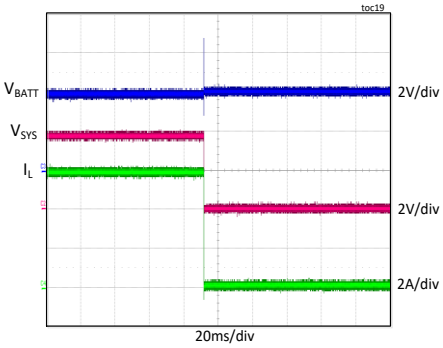



**BOOST SWITCHING WAVEFORM**
**OTG LOAD CURRENT = 1.5A**

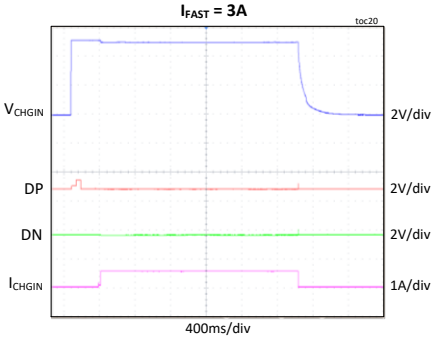


($V_{CHGIN}$ = 5V, $V_{BATT}$ = 3.8V, $T_A$ = +25°C, unless otherwise noted.)

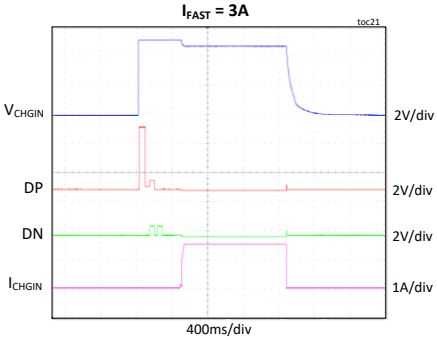
**6A OVERCURRENT PROTECTION**



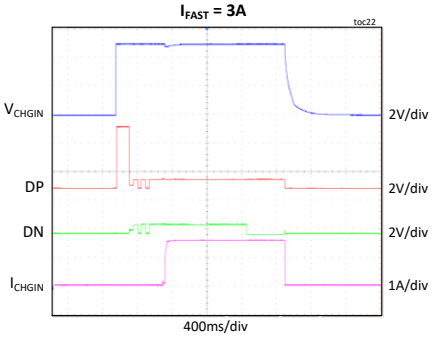

**CHARGER DETECTION**
**STANDARD DOWNSTREAM PORT (SDP)**
**$I_{FAST}$ = 3A**



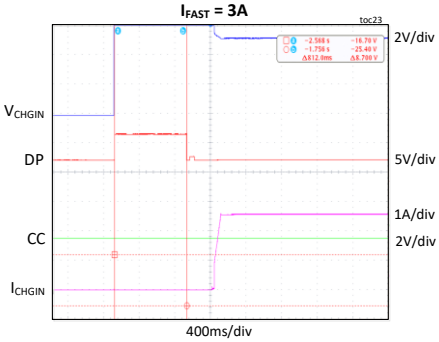

**CHARGER DETECTION**
**CHARGING DOWNSTREAM PORT (CDP)**
**$I_{FAST}$ = 3A**



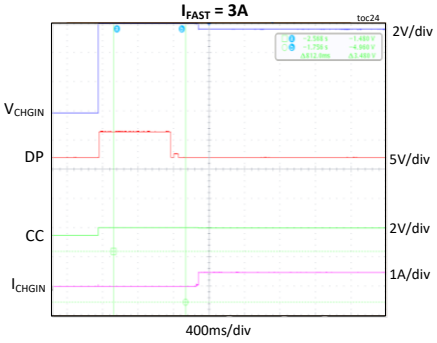

**CHARGER DETECTION**
**DEDICATED CHARGING PORT (DCP)**
**$I_{FAST}$ = 3A**



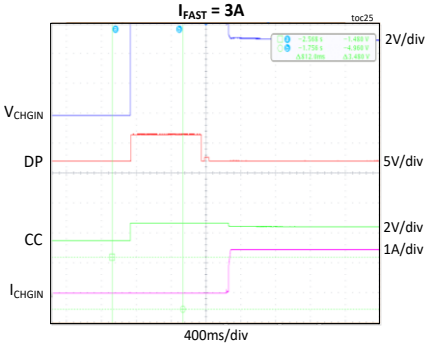

**CHARGER DETECTION**
**DATA CONTACT DETECT TIMEOUT**
**$I_{FAST}$ = 3A**



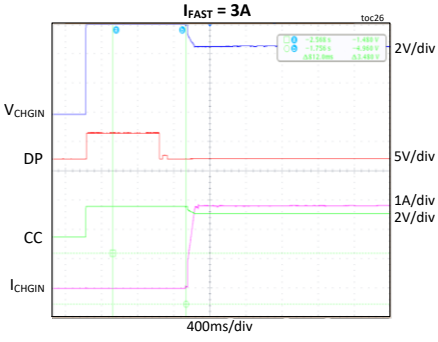

**USB TYPE-C DETECTION**
**SOURCE CAPABILITY 500mA**
**$I_{FAST}$ = 3A**



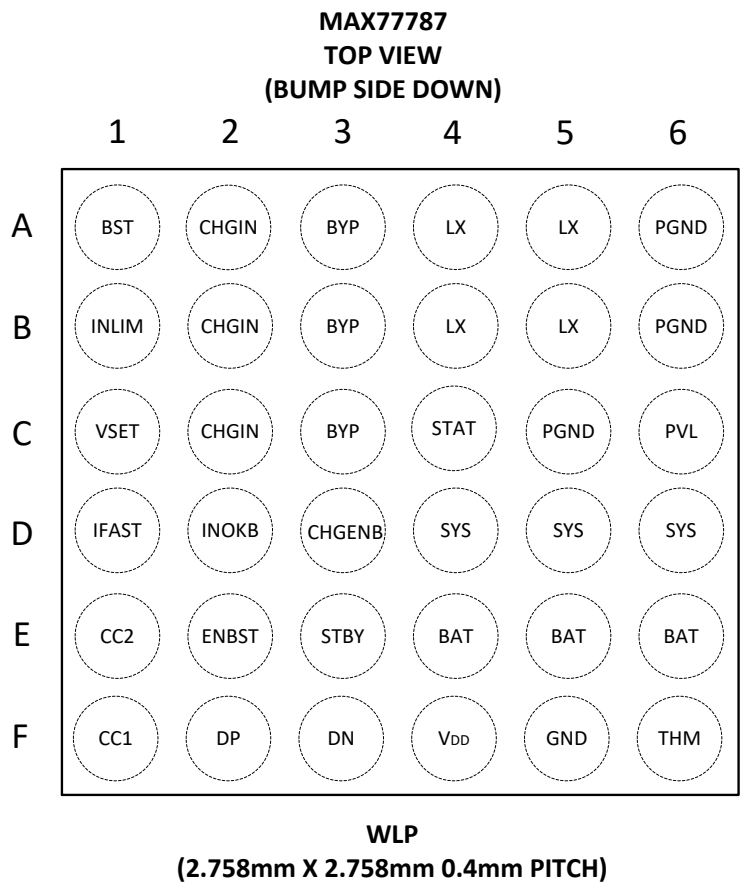

**USB TYPE-C DETECTION**
**SOURCE CAPABILITY 1500mA**
**$I_{FAST}$ = 3A**




**USB TYPE-C DETECTION**
**SOURCE CAPABILITY 3000mA**
**$I_{FAST}$ = 3A**



## Pin Configuration

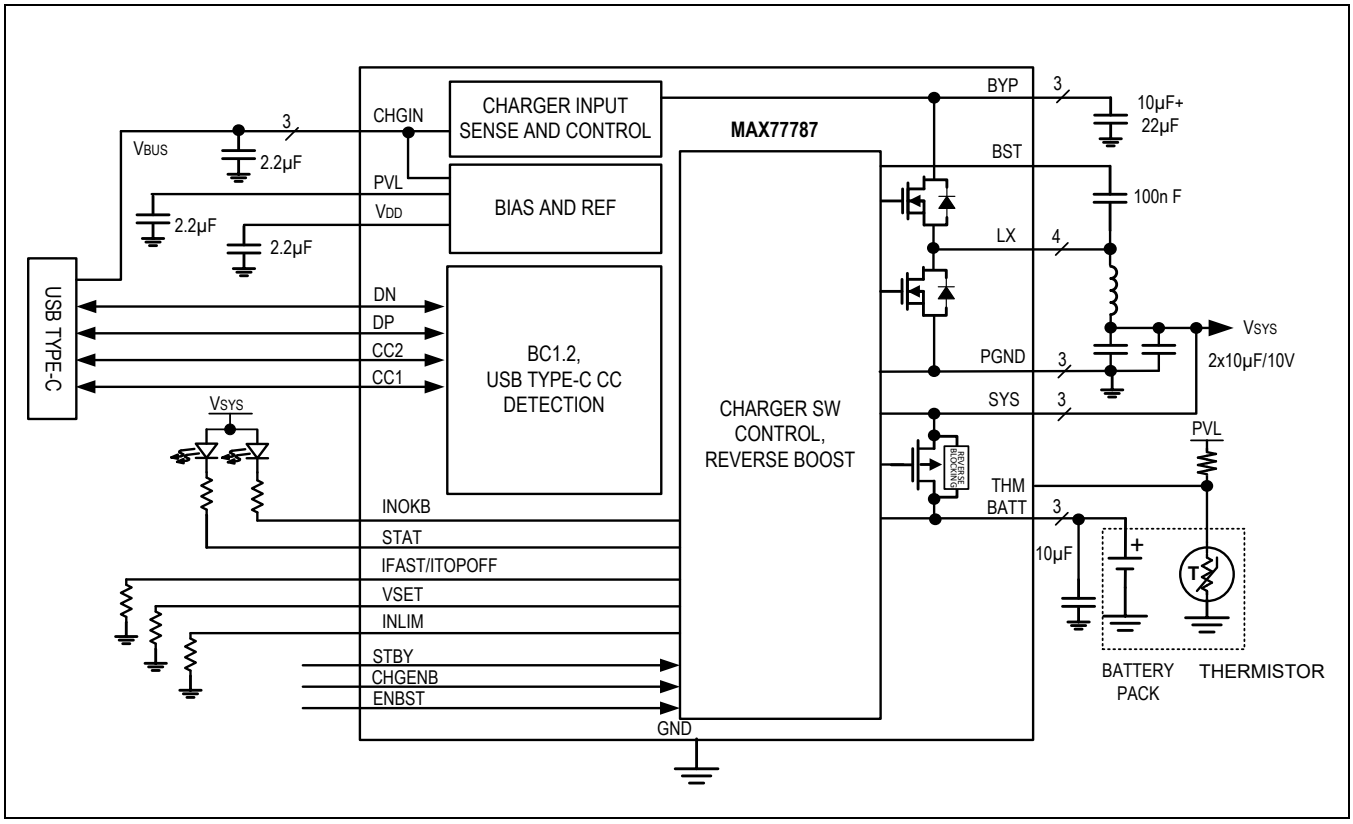



## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| A1 | BST | Provides Drive to High-Side Internal nMOS. Connect a 100nF/6.3V bootstrap capacitor between this pin and the LX node. |
| D2 | INOKB | Charger Input Valid, Active-Low Logic Output Flag. The open-drain output indicates when a valid voltage is present at CHGIN. |
| C4 | STAT | Open-Drain Charge Status Indication Output. STAT is toggling low and high impedance during charge. STAT becomes low when a top-off threshold is detected and in a done state. STAT becomes high impedance when charge faults happen. |
| E1 | CC2 | USB Type-C CC2 Connection |
| F1 | CC1 | USB Type-C CC1 Connection |
| F2 | DP | Positive Line of the USB Data Line Pair. Connect to D+ on USB Type-C or micro USB connector. |
| F3 | DN | Negative Line of the USB Data Line Pair. Connect to D- on USB Type-C or micro USB connector. |
| E2 | ENBST | Active-High Logic Input. Enable/disable the reverse-boost converter. |
| F5 | GND | Analog Ground. Short to ground plane. |

| | | |
|---|---|---|
| F4 | $V_{DD}$ | Output of On-Chip LDO Used to Power On-Chip, Low-Noise Circuits. Bypass with a 2.2µF/10V ceramic capacitor to GND. Powering external loads from $V_{DD}$ is not recommended other than pullup resistors. |
| F6 | THM | Thermistor Connection. Connect an external negative temperature coefficient (NTC) thermistor from THM to GND. Connect a resistor equal to the thermistor +25°C resistance from THM to PVL. See the *JEITA Compliance* for details. |
| D1 | IFAST | Fast-Charge Current Setting Pin. Connect a resistor ($R_{IFAST}$) from IFAST to GND to program the fast-charge current. Use 24.9kΩ for 3.15A fast-charge current. |
| E4,E5,E6 | BATT | Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li-ion battery. Bypass BATT to PGND ground plane with a 10µF ceramic capacitor. |
| D4,D5,D6 | SYS | System Power Node. Bypass SYS to PGND with a 2x10µF/10V ceramic capacitor. |
| C6 | PVL | Output of On-Chip LDO, Noisy Rail due to Bootstrap Operation. Bypass with a 2.2µF/10V ceramic capacitor to PGND. Powering external loads from PVL is not recommended. |
| A6,B6,C5 | PGND | Power Ground. Connect the return of the buck output capacitor close to these pins. |
| A4,A5,B4, B5 | LX | Switching Node. Connect an inductor between LX and SYS. When the buck converter is enabled, LX switches between BYP and PGND to control the input current, battery current, battery voltage, and die temperature. |
| A3,B3,C3 | BYP | System Power Connection. Output of OVP adapter input block and input to switching charger. Bypass with a 22µF/16V ceramic capacitor from BYP to PGND. |
| A2,B2,C2 | CHGIN | Charger Input. Up to 13.4V operating, 16VDC withstand input pin connected to an adapter or USB power source. Connect a 2.2µF/16V ceramic capacitor from CHGIN to GND. |
| C1 | VSET | Charge Termination Voltage Setting Input. Connecting a resistor ($R_{VSET}$) from VSET to GND programs the charge termination voltage. |
| D3 | CHGENB | Active-Low Input. Battery charging is enabled when CHGENB connects to low. |
| E3 | STBY | Active-High Input. Connect high to disable the DCDC between CHGIN input and SYS output. CHGIN supply current reduces to $I_{CHGIN\_STBY}$. The battery supplies the system power. Connect low to control the DCDC with the power path-state machine |
| B1 | INLIM | Charger Input Current Limit Setting Input. Connecting a resistor ($R_{INLIM}$) from INLIM to GND programs the charger input current limit. The input current limit setting through a resistor is valid only when the adaptor is detected as unknown. Else, the input current limit is programmed by D+/D- detection and CC detection result. |

## Functional Diagram




## Detailed Description

The MAX77787 is a highly integrated USB Type-C charger with autonomous configuration. The IC can operate input range from 4.5V to 13.4V to support 5V, 9V, and 12V AC adapter and USB input. The fast-charge current is up to 3.15A and the max input current limit is 3.0A.

The IC can run BC1.2 and USB Type-C CC detection upon input insertion and configure input source to max power option and charger input current limit to max power.

Fast-charge current and top-off current threshold can be programmed with an external resistor. Input voltage regulation feature (AICL) even allows users to use weak AC adapters without preventing charge.

Power path design provides system power even when the battery is fully discharged and it supplements current from the battery and charge input automatically when the system demands higher current.

Reverse boost from the battery can be enabled by the ENBST and STBY pins to allow 5.1V/1.5A OTG to $V_{BUS}$ or BYP.

### Switching Mode Charger

#### Features

- Complete Li+/LiPoly/LiFePO$_4$ Battery Charger
  - Prequalification, Constant Current, Constant Voltage
  - 55mA Pre-charge Current
  - 300mA Trickle Charge Current for MAX77787J Version. For the MAX77787H version, the trickle charge current is disabled.
  - Resistor Adjustable Constant Current Charge
    - 500mA to 3.15A (See *Table 6*)
  - Resistor Adjustable Battery Regulation Voltage
    - 3.6V to 4.55V (See *Table 5*)

  - -0.9/+0.3% Accuracy at +25°C
  - -1/+0.5% Accuracy from 0°C to +85°C
- Synchronous Switch-Mode Based Design
- Smart Power Selector
  - Optimally Distributes Power Between the Charge Adapter, System, and Main Battery
  - When Powered by a Charge Adapter, the Main Battery can Provide Supplemental Current to the System
  - The Charge Adapter can Support the System without the Main Battery
- No External MOSFETs Required
- Single Input Operation
  - Reverse Leakage Protection Prevents the Battery Leaking Current to the Inputs
  - $V_{CHGIN\_OVLO}$ = 13.4V
  - Supports AC-to-DC Wall Adapters
  - Automatic Input Current Limit Selection after Charger Type Detection
    - 500mA, 1A, 2A, 2.5A, 3A
  - External Programmable Input Current Limit when Unknown Charger Type is detected
    - 500mA to 3A (See *Table 4*)
- Charge Safety Timer
  - 6 Hour
- Die Temperature Monitor with Thermal Foldback Loop
  - Die Temperature Thresholds (°C): 130°C
- Input Voltage Regulation allows Operation from High-Impedance Sources (AICL)
- BATT to SYS Switch is 13mΩ Typical
  - Capable of 4.5A Steady-State Operation from BATT to SYS
- Short Circuit Protection
  - BATT to SYS Overcurrent Threshold: 6A
  - SYS Short-to-Ground
    - Buck Operates with Input Current Limit to 200mA when $V_{SYS} < V_{SYSPU}$

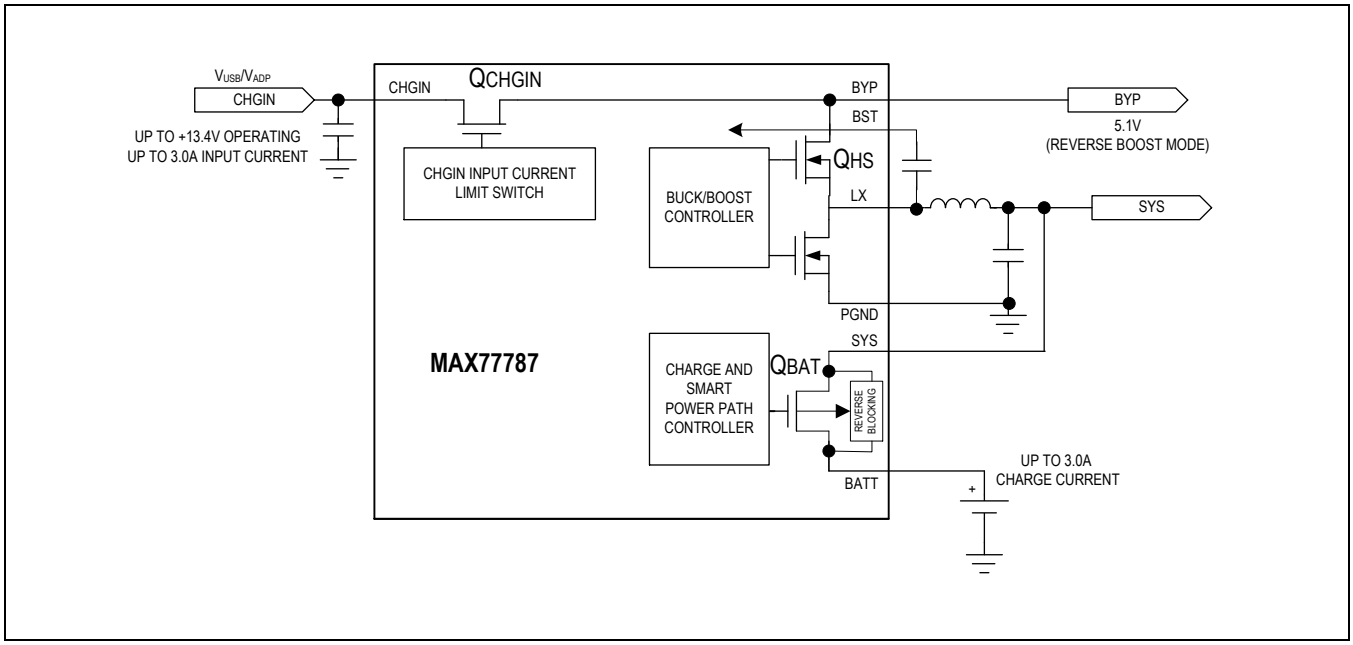



*Figure 1. Simplified Functional Diagram*

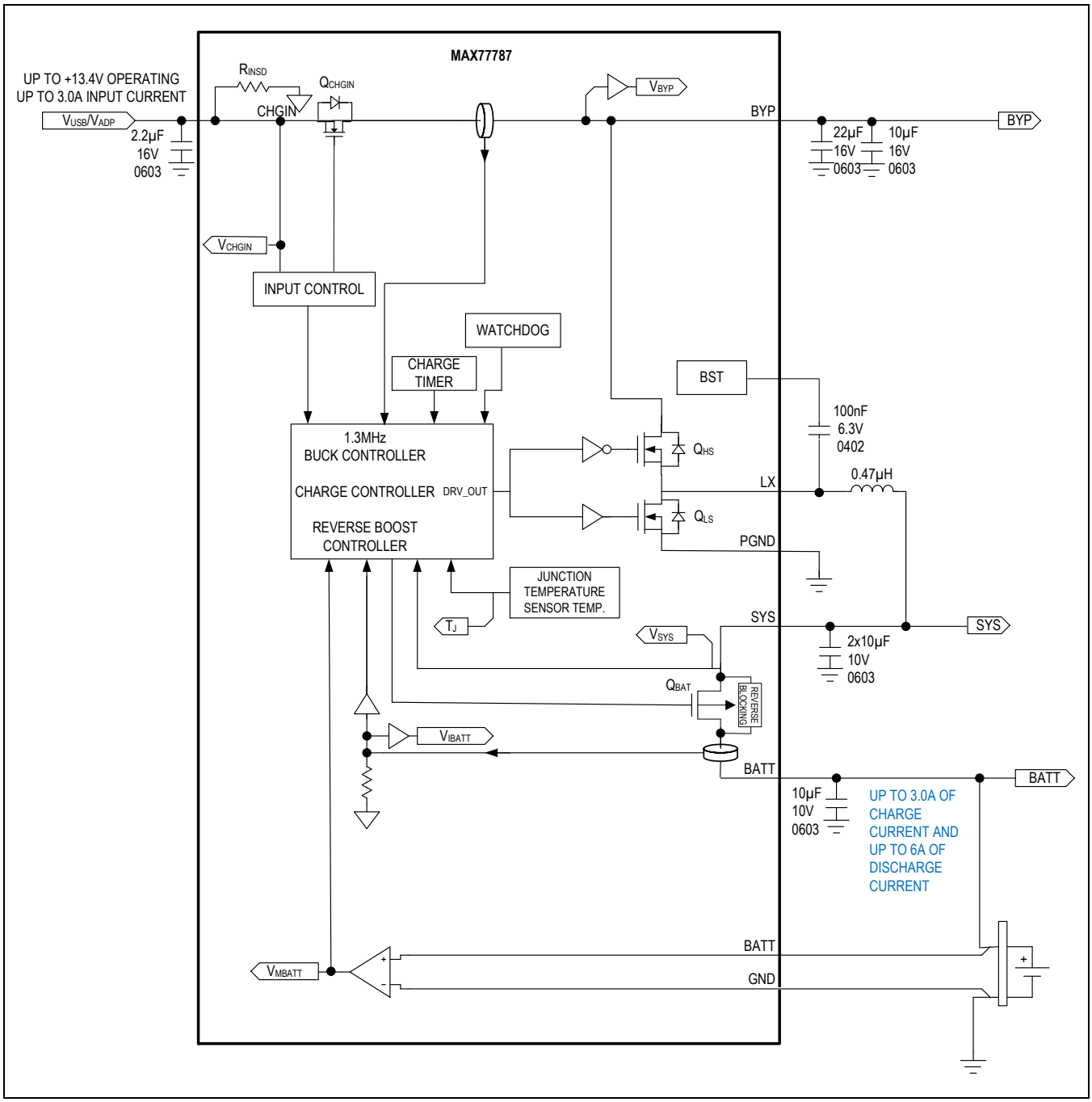



*Figure 2. Main Battery Charger Detailed Functional Diagram*

## Detailed Description

The IC is a switch-mode charger for a one-cell lithium-ion (Li+), lithium polymer (Li-polymer) battery, or $LiFePO_4$ battery. As shown in *Figure 2*, the current limit for CHGIN input is automatically configured allowing the flexibility for connection to either an AC-to-DC wall charger or a USB port.

The synchronous switch-mode DC-DC converter utilizes a high 1.3MHz switching frequency which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When charging the main battery the converter operates as a buck. The DC-DC buck operates from a 4.5V to 13.4V source and delivers up to 3.15A to the battery. The battery charge current is programmable from 500mA to 3.15A with an external resistor.

As a boost converter, the DC-DC uses energy from the main battery to boost the voltage at BYP. The boosted BYP voltage is useful to supply the USB OTG voltage which is fixed to 5.1V.

Maxim's Smart Power Selector architecture makes the best use of the limited adapter power and the battery's power at all times to supply up to Buck Current Limit from the buck to the system. (Additionally, supplement mode provides additional current from the battery to the system up to B2SOVRC.) Adapter power that is not used for the system goes to charging the battery. All power switches for charging and switching the system load between the battery and adapter power are included on-chip—no external MOSFETs are required.

Maxim's proprietary process technology allows for low-$R_{DSON}$ devices in a small solution size. The total dropout resistance from adapter power input to the battery is 114mΩ (typ) assuming that the inductor has 0.04Ω of ESR. This 114mΩ typical dropout resistance allows for charging a battery up to 3.0A from a 5V supply. The resistance from the BATT-to-SYS node is 13mΩ, allowing for low power dissipation and long battery life.

A multitude of safety features ensures reliable charging. Features include a charge timer, junction thermal regulation, over/undervoltage protection, and short circuit protection.

The BATT-to-SYS switch has overcurrent protection (see the *Main Battery Overcurrent Protection* section for more information).

### Smart Power Selector (SPS)

The SPS architecture is a network of internal switches and control loops that distributes energy between an external power source CHGIN, BYP, SYS, and BATT.

*Figure 1* shows a simplified arrangement for the Smart Power Selector's power steering switches. *Figure 2* shows a more detailed arrangement of the Smart Power Selector switches and gives them the following names: $Q_{CHGIN}$, $Q_{HS}$, $Q_{LS}$, and $Q_{BAT}$.

#### Switch and Control Loop Descriptions

- CHGIN Input Switch: $Q_{CHGIN}$ provides the input overvoltage protection of +16V. The input switch is either completely on or completely off. As shown in *Figure 2*, there are SPS control loops that monitor the current through the input switches as well as the input voltage.
- DC-DC Switches: $Q_{HS}$ and $Q_{LS}$ are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is moved from BYP to SYS. When operating as a boost, energy is moved from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.
- Battery-to-System Switch: $Q_{BAT}$ controls the battery charging and discharging. Additionally, $Q_{BAT}$ allows the battery to be isolated from the system (SYS). An SPS control loop monitors the $Q_{BAT}$ current.

#### SYS Regulation Voltage

- When the DC-DC is enabled as a buck and the charger is enabled but in a non-charging state such as done, thermal shutdown, or timer fault, $V_{SYS}$ is regulated to $V_{BATTREG}$, and $Q_{BAT}$ is off.
- When the DC-DC is enabled as a buck and charging in trickle-charge, fast-charge, or top-off modes, $V_{SYS}$ is regulated to $V_{SYSMIN}$ when the $V_{PRECHG} < V_{BATT} < V_{SYSMIN}$. And, when the DC-DC is enabled as a buck and charging in precharge mode ($V_{BATT} < V_{PRECHG}$), $V_{SYS}$ is regulated to $V_{BATTREG}$. In these modes, the $Q_{BAT}$ switch acts as a linear regulator and dissipates power [$P = (V_{SYS} - V_{BATT}) \times I_{BATT}$]. When $V_{BATT} > V_{SYSMIN}$, then $V_{SYS} = V_{BATT} + I_{BATT} \times R_{BAT2SYS}$. In this mode, the $Q_{BAT}$ switch is closed.

In all of the above modes, if the combined SYS loading exceeds the input current limit, then $V_{SYS}$ drops to $V_{BATT} – V_{BSREG}$, and the battery provides supplemental current.

### Input Validation

The charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following three characteristics to be valid:

- CHGIN must be above $V_{CHGIN\_UVLO}$ to be valid. Once CHGIN is above the UVLO threshold, the information (together with LIN2SYS, described below) is latched and can only be reset when the charger is in the adaptive input current loop (AICL) and the input current is lower than the IULO threshold of 60mA. Note that $V_{CHGIN\_REG}$ is lower than their UVLO falling threshold, respectively.
- CHGIN must be below its overvoltage lockout threshold ($V_{CHGIN\_OVLO}$)
- CHGIN must be above the system voltage by $V_{CHGIN2SYS}$

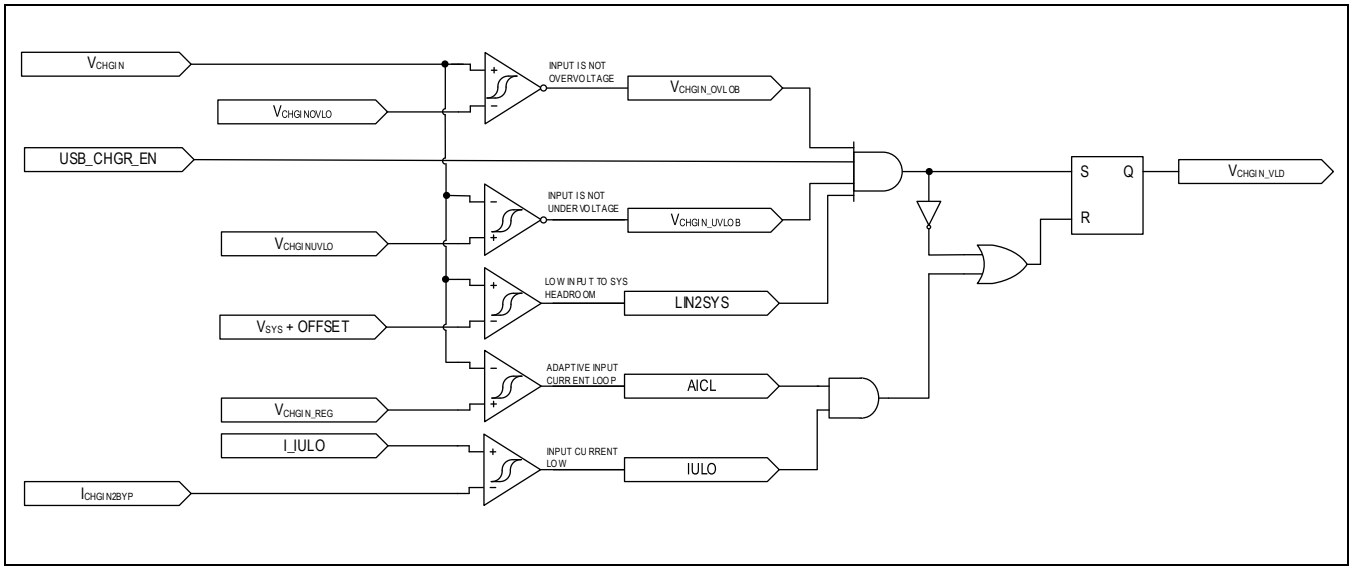



*Figure 3. CHGIN Valid Signal Generation Logic*

The INOKB pin is pulled down when CHGINOK = 1 and the switcher starts.

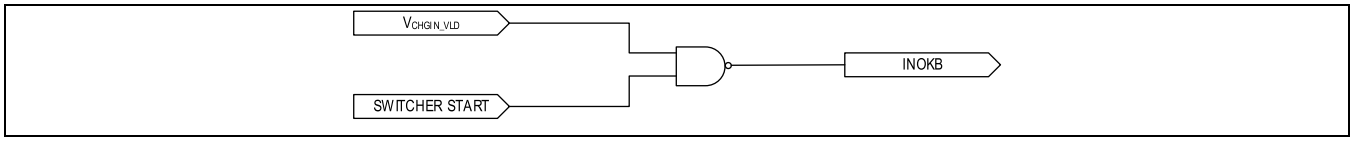



*Figure 4. INOKB Signal Generation Logic*

### Input Current Limit

The IC has two ways to control the input current limit. After the charger-type detection is done, the IC automatically configures the input current limit to the highest settings that the source can provide. If the input source is not a standard power source described by BC1.2, USB Type-C, or proprietary charger type that the IC can detect, the IC sets the input current limit according to $R_{INLIM}$. In the case of floating $R_{INLIM}$, the IC input current limit is set to 500mA when an unknown proprietary charger is detected.

### Input Voltage Regulation Loop

An input voltage regulation loop allows the charger to be well behaved when it is attached to a poor-quality charge source. The loop improves performance with relatively high resistance charge sources that exist when long cables are used or devices are charged with non-compliant USB hub configurations.

The input voltage regulation loop automatically reduces the input current limit to keep the input voltage at $V_{CHGIN\_REG}$. If the input current limit is reduced to $I_{ULO}$ (65mA typ) and the input voltage is below $V_{CHGIN\_REG}$, then the charger input is turned off.

### Input Self-Discharge

To ensure that a rapid removal and reinsertion of a charge source always results in a charger input interrupt, the charger input presents loading to the input capacitor to ensure that when the charge source is removed the input voltage decays below the UVLO threshold in a reasonable time ($t_{INSD}$). The input self-discharge is implemented with a 44kΩ resistor ($R_{INSD}$) from CHGIN input to ground.

### Charger States

#### Li+/Li-Poly Battery

The MAX77787J utilizes several charging states to safely and quickly charge Li+/Li-Poly batteries as shown in *Figure 5* and *Figure 6*. *Figure 5* shows an exaggerated view of the Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and battery is close to room temperature: precharge → trickle → fast-charge → top-off → done.

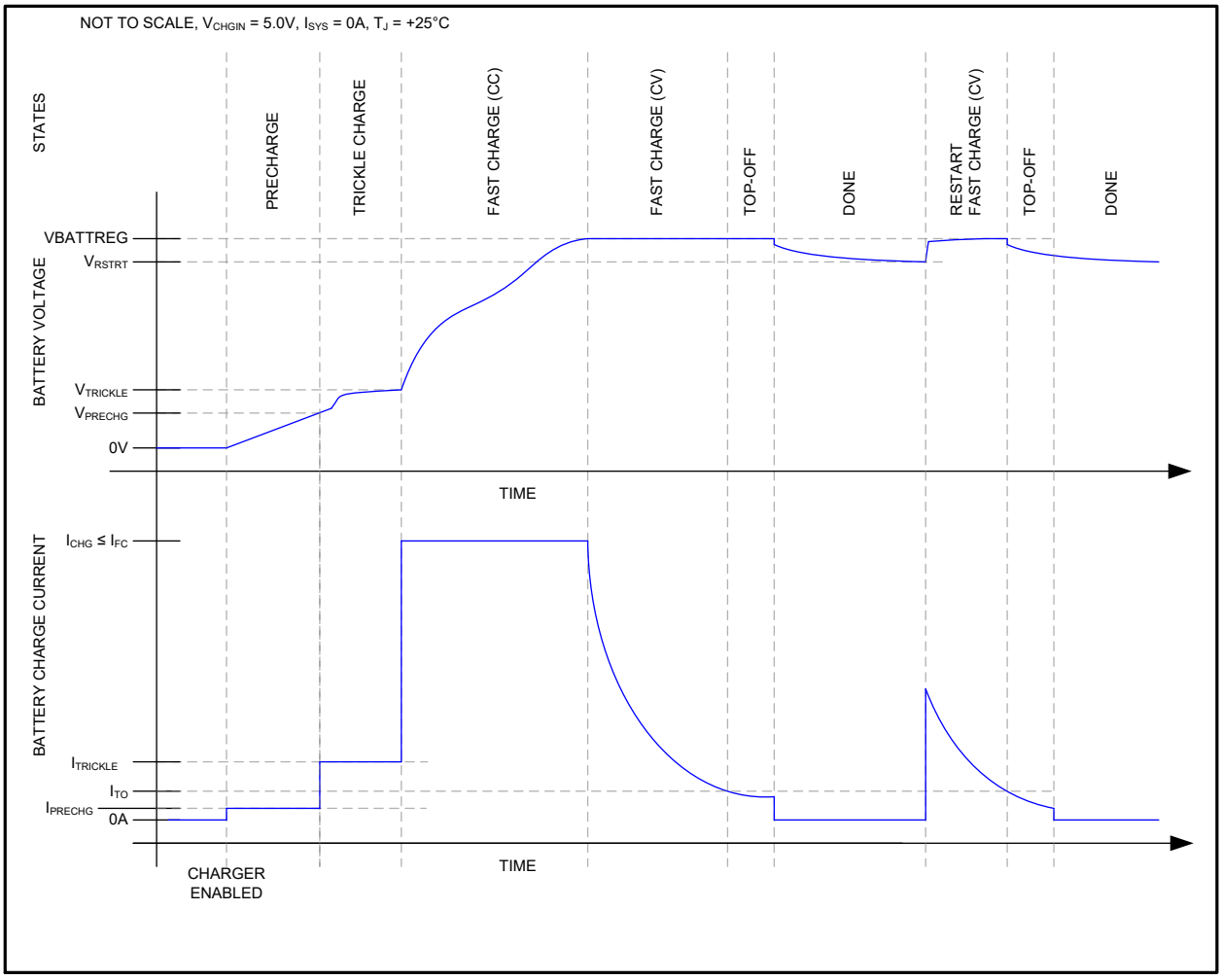



*Figure 5. Li+/Li-Poly Charge Profile*

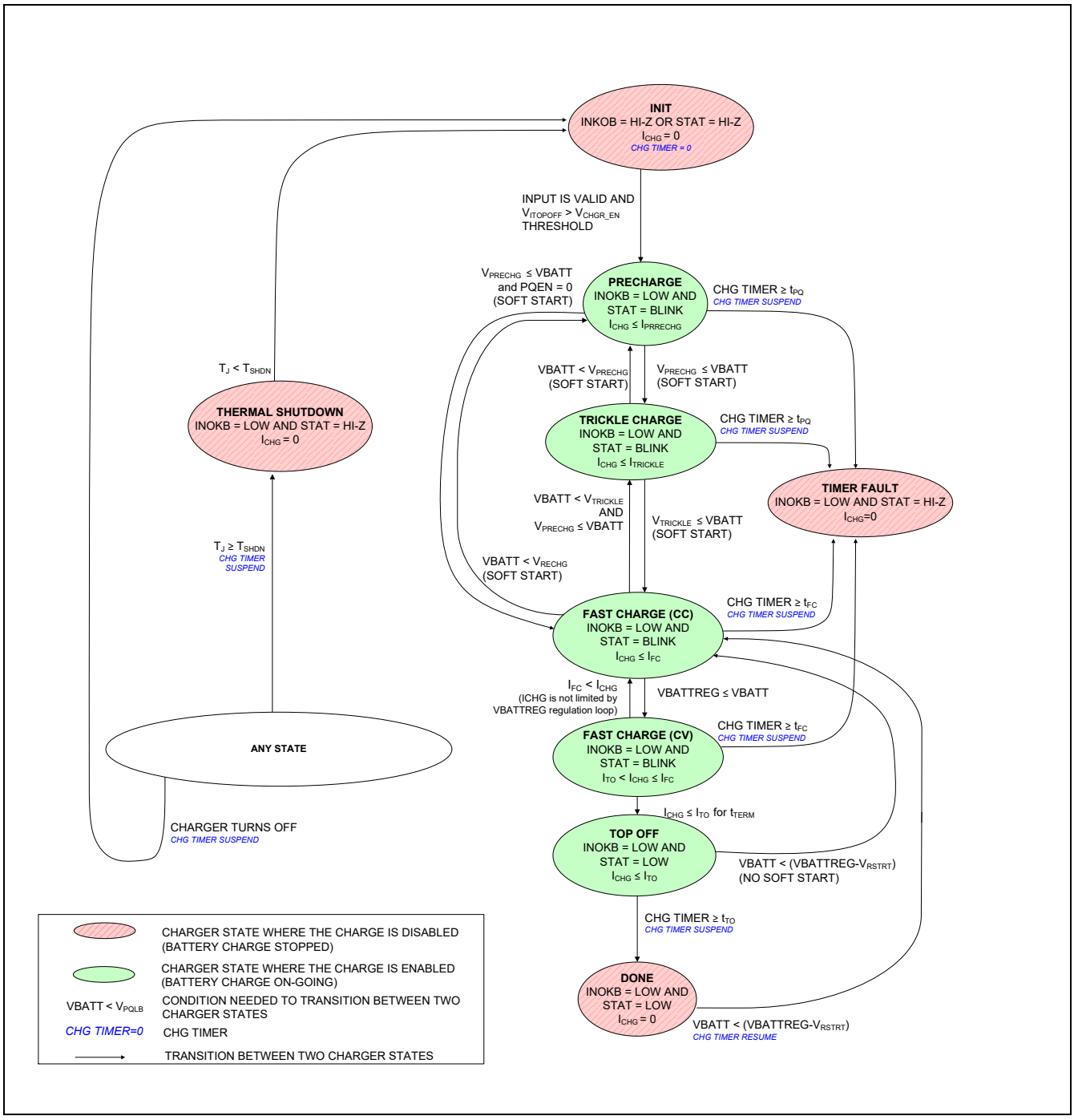



*Figure 6. Li+/Li-Poly Charger State Diagram*

### $LiFePO_4$ Battery

As for the $LiFePO_4$ battery, the MAX77787H skips the trickle charge state and directly enters the fast-charge state after the precharge state. *Figure 7* and *Figure 8* presents the $LiFePO_4$ battery charge profile and state machine: precharge → fast-charge → top-off → done.

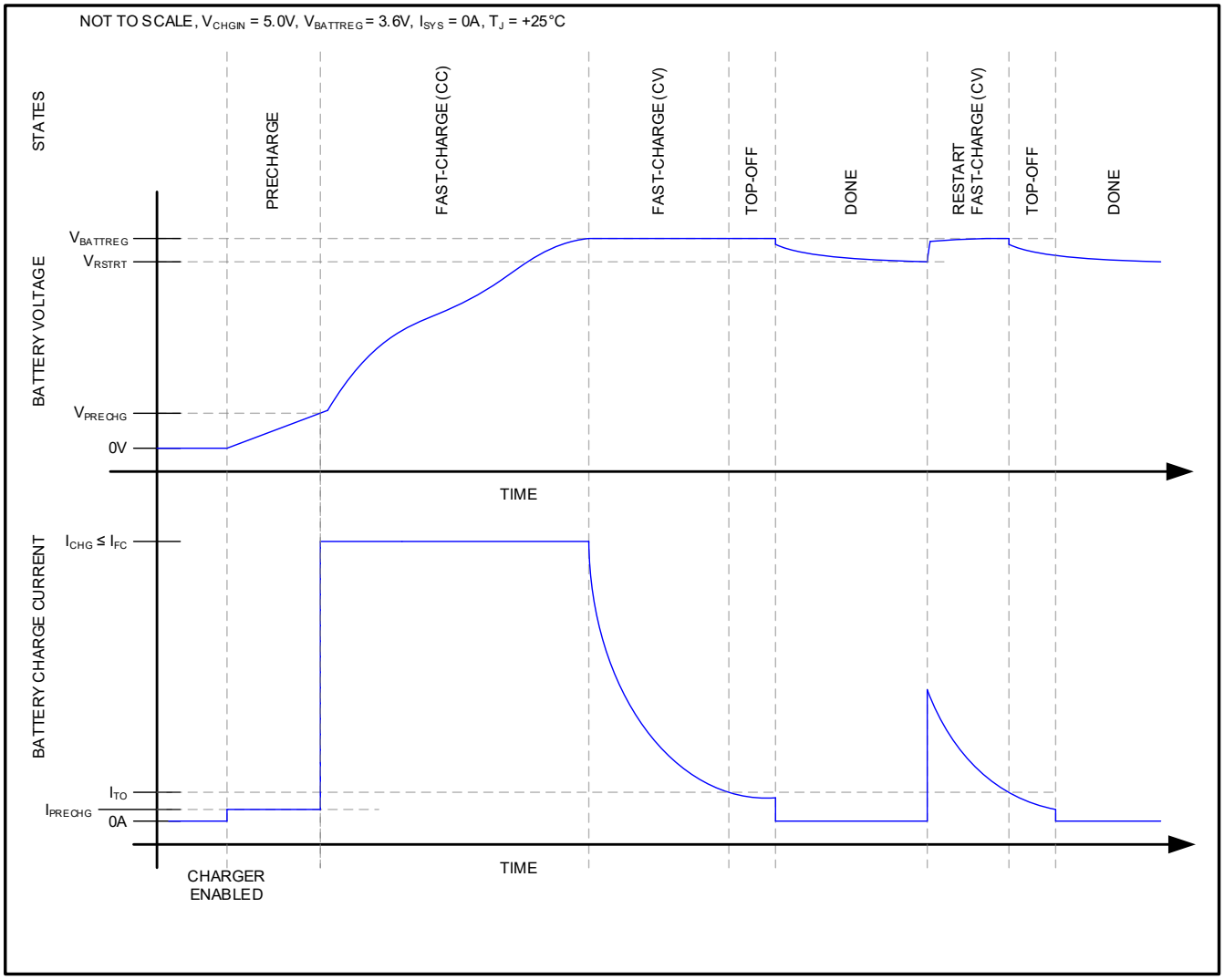



*Figure 7. $LiFePO_4$ Battery Charge Profile*

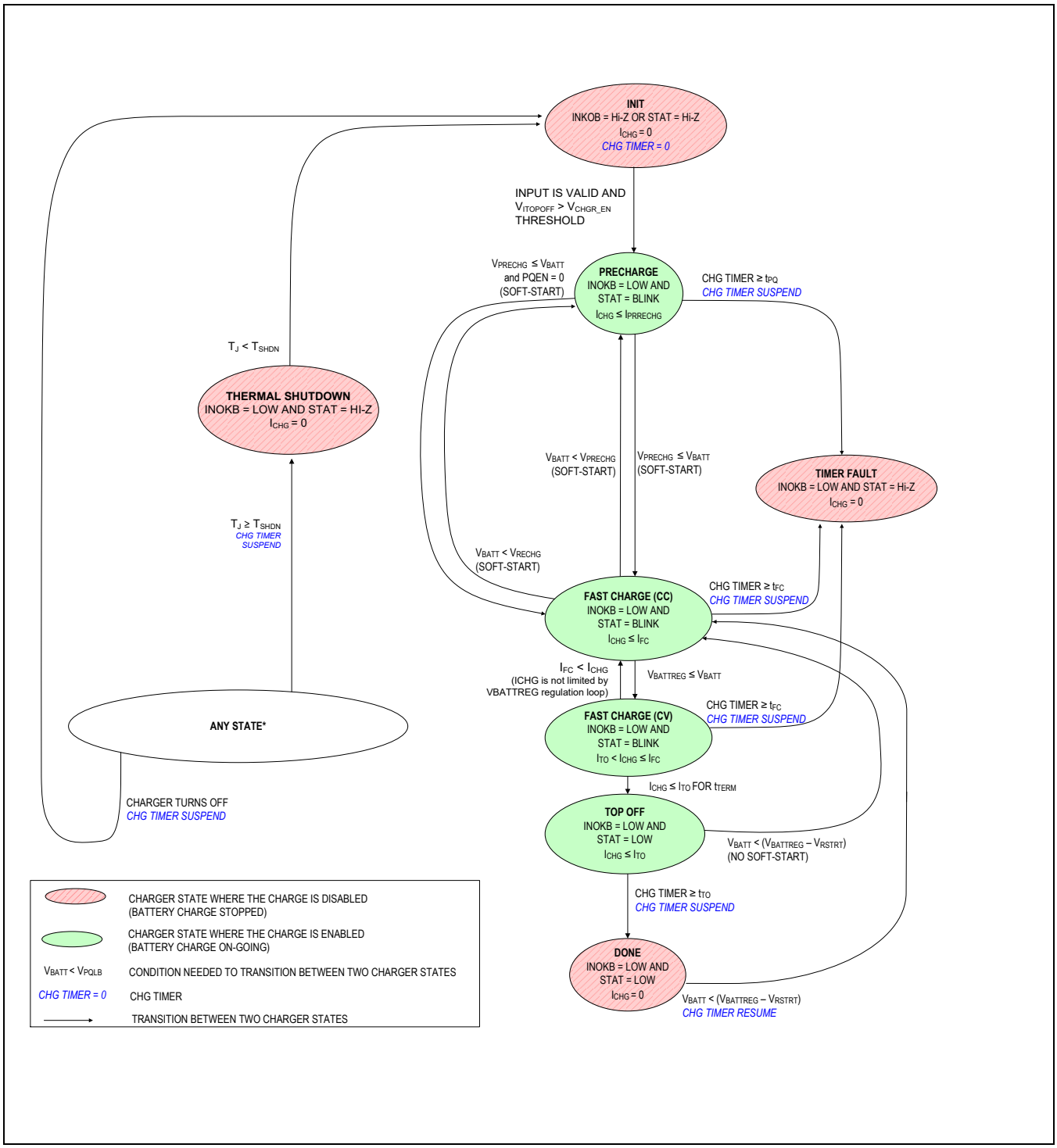



*Figure 8. LiFePO$_4$ State Machine*

### INIT State

From any state shown in *Figure 6* except thermal shutdown, the “INIT” state is entered whenever the charger inputs CHGIN is invalid or the charger timer is suspended.

While in the “INIT” state, the charger current is 0mA, the charge timer is forced to 0, and the power to the system is provided by the battery.

To exit the “INIT” state the charger input must be valid.

### Pre-Charge State

As shown in *Figure 6*, the pre-charge state occurs when the main battery voltage is less than $V_{PRECHG}$. In the pre-charge state, the charge current into the battery is $I_{PRECHG}$.

The following events cause the state machine to exit this state:

- The main battery voltage rises above $V_{PRECHG}$ and the charger enters the next state in the charging cycle, trickle charge.
- If the battery charger remains in this state for longer than $t_{PQ}$, the charger state machine transitions to the timer fault state.

Note that the pre-charge state works with battery voltages down to 0V. The low 0V operation typically allows the battery charger to recover batteries that have an “open” internal pack protector. Typically, a pack internal protection circuit opens if the battery has seen an overcurrent, undervoltage, or overvoltage. When a battery with an “open” internal pack protector is used with this charger, the pre-charge mode current flows into the 0V battery—this current raises the pack’s terminal voltage to the point where the internal pack protection switch closes.

Note that a normal battery typically stays in the pre-charge state for several minutes or less. Therefore, a battery that stays in the pre-charge state for longer than $t_{PQ}$ might be experiencing a problem.

### Trickle Charge State

The trickle charge mode described below is for Li-ion and Li-poly batteries only, with charge termination voltage from 4.1V to 4.5V.

As shown in *Figure 6*, the trickle charge state occurs when $V_{BATT} > V_{PRECHG}$ and $V_{BATT} < V_{TRICKLE}$.

When the MAX77787J is in its trickle charge state, the charge current in the battery is less than or equal to $I_{TRICKLE}$.

Charge current might be less than $I_{TRICKLE}$ for the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above $V_{TRICKLE}$, the charger enters the next state in the charging cycle, fast charge (CC).
- If the battery charger remains in this state for longer than $t_{PQ}$, the charger state machine transitions to the timer fault state.

Note that a normal battery typically stays in the trickle charge state for several minutes or less. Therefore, a battery that stays in trickle charge for longer than $t_{PQ}$ might be experiencing a problem.

Based on the characteristic of the LiFePO4 battery, the trickle charge state of MAX77787H is disabled. After the pre-charge state, when $V_{PRECHG} < V_{BATT} < V_{BATTREG}$, MAX77787H enters the fast-charge constant current state to improve the charger efficiency.

### Fast-Charge Constant Current (CC) State

As shown in *Figure 6*, the fast-charge constant current (CC) state occurs when the main-battery voltage is greater than the trickle threshold and less than the battery regulation threshold ($V_{TRICKLE} < V_{BATT} < V_{BATTREG}$).

In the fast-charge CC state, the current into the battery is less than or equal to $I_{FC}$. Charge current can be less than $I_{FC}$ for the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above $V_{BATTREG}$, the charger enters the next state in the charging cycle, fast charge (CV).
- If the battery charger remains in this state for longer than $t_{FC}$, the charger state machine transitions to the timer fault state.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds $T_{REG}$, $I_{FC}$ is reduced. See the *Thermal Foldback* section for more information.

### Fast-Charge Constant Voltage (CV) State

As shown in *Figure 6*, the fast-charge constant voltage (CV) state occurs when the battery voltage rises to $V_{BATTREG}$ from the fast-charge CC state.

In the fast-charge CV state, the battery charger maintains $V_{BATTREG}$ across the battery and the charge current is less than or equal to $I_{FC}$. As shown in *Figure 5*, charger current decreases exponentially in this state as the battery becomes fully charged.

The Smart Power Selector control circuitry might reduce the charge current lower than the battery can otherwise consume for the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the charger current is below $I_{TO}$ for $t_{TERM}$, the charger enters the next state in the charging cycle, top off.
- If the battery charger remains in this state for longer than $t_{FC}$, the charger state machine transitions to the timer fault state.

### Top-Off State

As shown in *Figure 6*, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below $I_{TO}$ for $t_{TERM}$. In the top-off state, the battery charger tries to maintain $V_{BATTREG}$ across the battery, and typically the charge current is less than or equal to $I_{TO}$.

The Smart Power Selector control circuitry might reduce the charge current lower than the battery can otherwise consume for the following reasons:

- The charger input is in the input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the top-off time ($t_{TO}$), the charger enters the next state in the charging cycle, done.
- If $V_{BATT} < V_{BATTREG} - V_{RSTRT}$, the charger goes back to the fast charge (CC) state

### Done State

As shown in *Figure 6*, the battery charger enters its done state after the charger has been in the top-off state for $t_{TO}$.

The following event causes the state machine to exit this state:

- If $V_{BATT} < V_{BATTREG} - V_{RSTRT}$, the charger goes back to the fast charge (CC) state

In the done state, the charge current into the battery ($I_{CHG}$) is 0A. In the done state, the charger presents a very low quiescent current to the battery. If the system load presented to the battery is low (<<100µA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold ($V_{RSTRT}$), and the charger state machine transitions back into the fast-charge CC state. There is no soft-start (di/dt limiting) during the done to fast-charge state transition.

### Timer Fault State

The battery charger provides both a charge timer to ensure safe charging. As shown in *Figure 6*, the charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of its prequalification states is $t_{PQ}$. The time that the charger is allowed to remain in the fast-charge CC and CV states is $t_{FC}$. Finally, the time that the charger is in the top-off state is $t_{TO}$. Upon entering the timer fault state, STAT becomes Hi-Z.

In the timer fault state, the charger is off. The charger input can be removed and re-inserted to exit the timer fault state (see the “any state” bubble in the lower left of *Figure 6*).

### Thermal Shutdown State

As shown in *Figure 6*, the thermal shutdown state occurs when the battery charger is in any state and the junction temperature ($T_J$) exceeds the device’s thermal shutdown threshold ($T_{SHDN}$). When $T_J$ is close to $T_{REG}$, the charger folds back the input current limit to 0A so that the charger and inputs are effectively off.

In the thermal shutdown state, the charger is off.

### Reverse Boost Mode

The DC-DC converter topology of the IC allows it to operate as a buck converter or as a reverse-boost converter. The modes of the DC-DC converter are controlled by ENBST. When ENBST = high, the DC-DC converter operates in reverse boost mode allowing it to source current to BYP and CHGIN, this mode allows current to be sourced from CHGIN and is commonly referred to as OTG mode or a source role. When the OTG mode is enabled, the unipolar CHGIN transfer function measures the current going out of CHGIN. The BYP to CHGIN switch automatically tries to retry after 300ms if CHGIN loading exceeds the 1.5A current limit. If the overload at CHGIN persists, then the CHGIN switch toggles ON and OFF with approximately 60ms ON and approximately 300ms OFF.

The IC also allows it to be sourced from BYP with ENBST = high and STBY = high.

The current through the BYP to CHGIN switch is limited to 1.5A minimum.

Note that injecting the higher $V_{CHGIN}$ than 5.1V in case of reverse boost mode enabled causes reverse boost function to be abnormal.

### Main Battery Overcurrent Protection During System Power-Up

The main battery overcurrent protection during the system power-up feature limits the main battery to system current to $I_{SYSPU}$ as long as $V_{SYS}$ is less than $V_{SYSPU}$. This feature limits the surge current that typically flows from the main battery to the device's low-impedance system bypass capacitors during a system power-up. System power-up is anytime that energy from the battery is supplied to SYS when $V_{SYS} < V_{SYSPU}$. This "system power-up" condition typically occurs when a battery is hot-inserted into an otherwise unpowered device.

When "system power-up" occurs due to hot-insertion into an otherwise unpowered device, a small delay is required for this feature's control circuits to activate. A current spike over $I_{SYSPU}$ might occur during this time.

### Main Battery Overcurrent Protection Due to Fault

The IC protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current can occur for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit.

When the main battery (BATT)-to-system (SYS) discharge current ($I_{BATT}$) exceeds 6A for at least $t_{BOVRC}$, then the IC disables the BATT-to-SYS discharge path ($Q_{BAT}$ switch) and turns off the buck. Under OCP fault condition, when SYS is low ($V_{SYS} < V_{SYSUP}$) for tocp_retry, the IC restarts on its own and attempts to pull up SYS again. If the fault condition remains, the whole cycle repeats until this fault condition is removed.

### Thermal Management

The IC charger uses several thermal management techniques to prevent excessive battery and die temperatures.

### Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the IC junction temperature. As shown in *Figure 9*, when the die temperature exceeds the REGTEMP ($T_{JREG}$), a thermal limiting circuit reduces the battery charger's target current by 5% of the fast-charge current per 1°C ($A_{TJREG}$), which corresponds to 157.5mA/°C when the fast-charge current is 3.15A. For lower programmed charge currents such as 480mA, this slope is valid for charge current reductions down to 80mA; below 100mA the slope becomes shallower but the charge current is still reduced to 0A if the junction temperature is 20°C above the programmed loop set point. The target charge current reduction is achieved with an analog control loop (i.e., not a digital reduction in the input current).

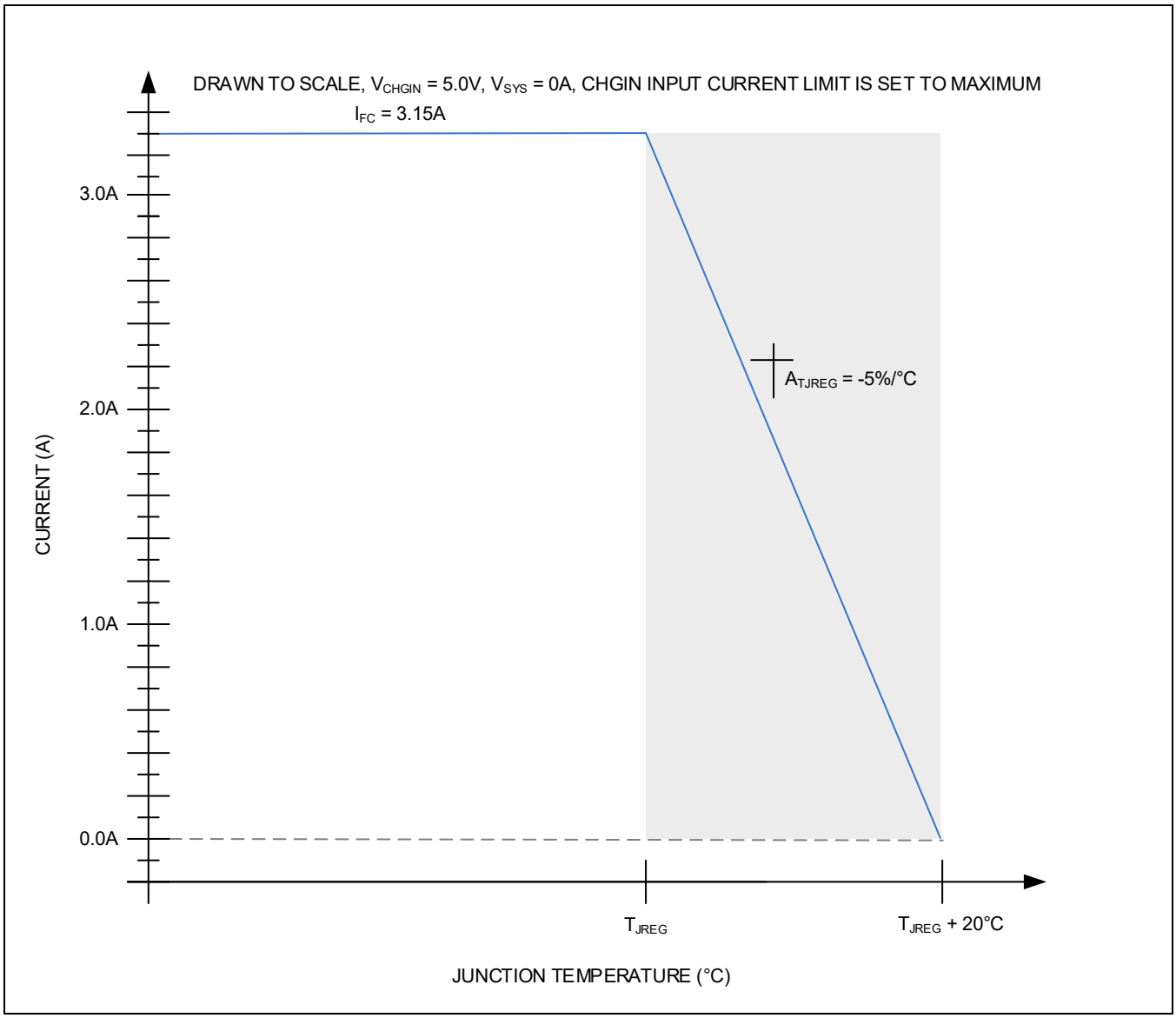



*Figure 9. Charge Currents vs. Junction Temperature*

### Thermistor Input (THM)

The thermistor input can be utilized to achieve functions including charge suspension and JEITA-compliant charging.

### JEITA Compliance

The MAX77787J version safely charges batteries in accordance with JEITA specifications. The MAX77787J version monitors the battery temperature with an NTC thermistor connected at the THM pin and automatically adjusts the fast-charge current or charge termination voltage as the battery temperature varies.

The JEITA controlled fast-charge current is reduced to 50% of the detected fast-charge current for $T_{COLD} < T < T_{COOL}$.

The charge termination voltage for $T_{WARM} < T < T_{HOT}$ is reduced to programmed termination voltage -150mV, as shown in *Figure 10*. Charging is suspended when the battery temperature is too cold or too hot ($T < T_{COLD}$ or $T_{HOT} < T$).

The MAX77787H version disables the JEITA under warm and cool conditions and stops charging when the temperature is too hot or cold. See the *Ordering Information* for details.

Temperature thresholds ($T_{COLD}$, $T_{COOL}$, $T_{WARM}$, and $T_{HOT}$) depend on the thermistor selection. See *Table 1* for more details.

Since the thermistor monitoring circuit employs an external bias resistor from THM to PVL, the thermistor is not limited only to 10kΩ (at +25ºC); any resistance thermistor can be used if the value is equivalent to the thermistors +25ºC resistance. The thermistor installed on the evaluation kit is 10kΩ with a beta of 3435.

The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{[\beta \times (\frac{1}{T+273} - \frac{1}{298})]}$$

where

$R_T$ = The resistance in Ω of the thermistor at temperature T in Celsius

$R_{25}$ = The resistance in Ω of the thermistor at +25ºC

β = The material constant of the thermistor, which typically ranges from 3000k to 5000k

T = The temperature of the thermistor in Celsius

## Table 1. Temperature Threshold for Different Thermistors

| THERMISTOR PART NUMBER | BETA (β) | R25 (Ω) | EXTERNAL BIAS RESISTOR FROM THM TO PVL, RTB (Ω) | JEITA TEMPERATURE THRESHOLD (TYPICAL) | | | |
|---|---|---|---|---|---|---|---|
| | | | | $T_{COLD}$ (°C) | $T_{COOL}$ (°C) | $T_{WARM}$ (°C) | $T_{HOT}$ (°C) |
| TX04F103F3380ER | 3380 | 10000 | 10000 | -0.2 | 9.6 | 45.5 | 60.5 |
| NCP15XH103F03 | 3435 | 10000 | 10000 | 0.2 | 9.8 | 45.2 | 59.9 |
| TH05-3N333FR | 3725 | 33000 | 33000 | 2 | 10.9 | 43.5 | 56.9 |
| TH05-4B473FR | 4057 | 47000 | 47000 | 3.7 | 12 | 41.9 | 54 |
| NTCG104EF104FT1X | 4308 | 100000 | 100000 | 4.9 | 12.8 | 40.9 | 52.2 |

**Note:**

- Thermistor resistance tolerance, pullup resistance tolerance, and parasitics are not considered in this table.
- Listed part numbers are for reference only.

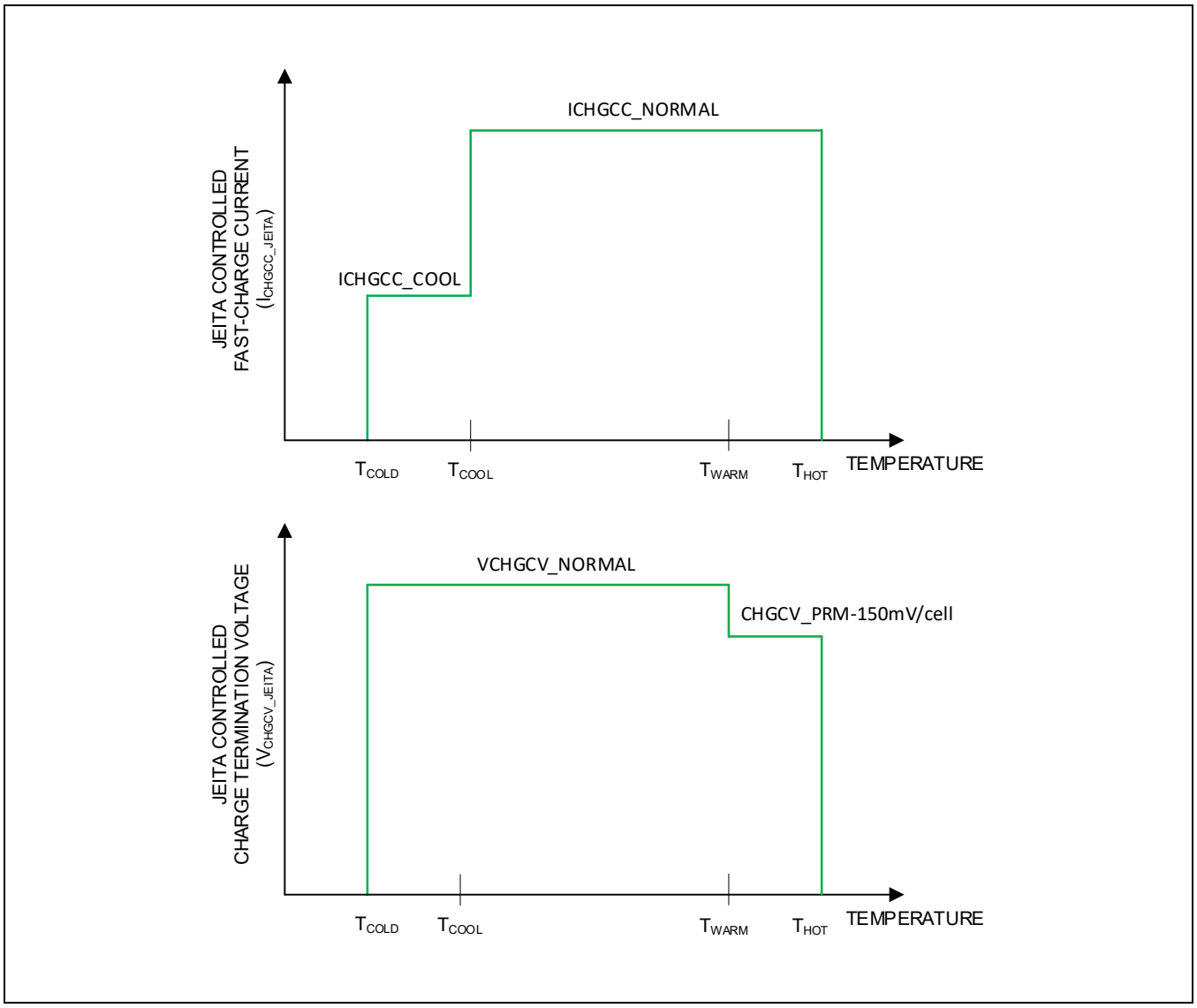



*Figure 10. MAX77787J Version JEITA Compliance*

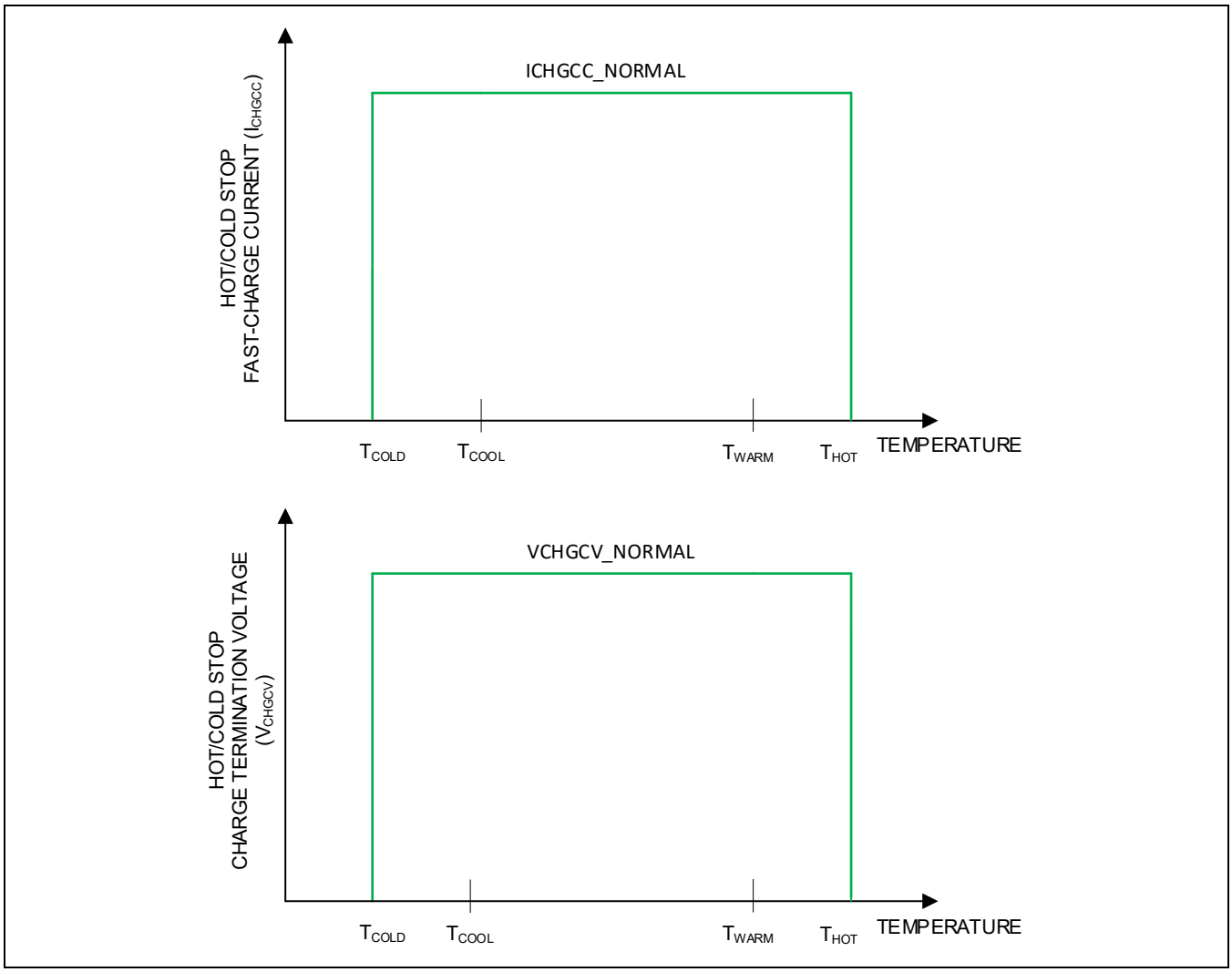



*Figure 11. MAX77787H Version Hot/Cold Stop*

### $V_{DD}$ Internal Supply

$V_{DD}$ is the 1.8V power for the IC charger's analog circuit. $V_{DD}$ is generated from an internal regulator which uses the higher of BATT and internal high voltage regulator as a power input source. $V_{DD}$ has a bypass capacitance of 2.2µF.

### CHGENB for Enable and Disable Charging

CHGENB is an input control signal for battery charging with an external logic signal. If CHGENB is driven by high when CHGIN is valid, the battery charging is disabled. CHGENB has an internal 235kΩ pulldown resistor.

### STBY for USB Suspend Mode

The host can reduce the IC's CHGIN supply current by driving the STBY pin to high. STBY has an internal 235kΩ pulldown resistor. When STBY is pulled high, the DCDC turns off. When STBY is pulled low, the DCDC is controlled by the power path state machine.

### ENBST for OTG Reverse Boost

ENBST is an input control signal for the reverse boost mode with an external logic signal. If ENBST is driven by high, the reverse boost is enabled and the BYP to CHGIN path is closed. It has an internal 235kΩ pulldown resistor. When ENBST sets to high, the IC disconnects Rd from the CC line and provides a 180µA current source to advertise 1.5A OTG current capability to the devices connected.

### ENBST and STBY for BYP Reverse Boost

If ENBST and STBY are driven by high, the reverse boost is enabled and delivers power from the battery to the BYP path. The BYP to CHGIN path is open.

## Mode Configuration by External Pins

The IC features an operating mode configuration by the combination of external pins when CHGIN is valid. *Table 2* lists each mode that the IC is supporting according to the CHGENB, ENBST, and STBY pin's status.

The OTG Reverse Boost Mode and BYP Reverse Boost Mode can only be enabled with the pin configurations in *Table 2*, when there is no power source connected to the CHGIN pin and when a battery is present.

## Table 2. Mode Configuration

| CHGENB | ENBST | STBY | CHGIN FET | $Q_{BAT}$ | MODE |
|---|---|---|---|---|---|
| 1 | 0 | 0 | ON | OFF | Buck = ON, Charging = OFF |
| 1 | 0 | 1 | OFF | OFF | Buck = OFF, Charging = OFF |
| 1 | 1 | 0 | ON | OFF | Both Buck, Boost = OFF, Charging = OFF |
| 1 | 1 | 1 | OFF | OFF | Both Buck, Boost = OFF, Charging = OFF |
| 0 | 0 | 0 | ON | ON | Buck = ON, Charging = ON |
| 0 | 0 | 1 | OFF | ON | Suspend Mode |
| 0 | 1 | 0 | ON | ON | OTG Reverse Boost Mode |
| 0 | 1 | 1 | OFF | ON | BYP Reverse Boost Mode |

### USB BC1.2 Charger Detection

#### Features

- D+/D- Charging Signature Detector
- USB BC1.2 Compliant
- SDP, DCP, and CDP Detection
- Detect Proprietary Charger Types
  - Apple 500mA, 1A, 2A, 12W
  - Samsung 2A

#### Description

The USB charger detection is USB BC1.2 compliant with the ability to automatically detect some common proprietary charger types.

The charger detection state machine follows USB BC1.2 requirements and detects SDP, CDP, and DCP types. The charger detection state machine indicates if D+/D- were found as open then the input current limit is set by $R_{INLIM}$.

In addition to the USB BC1.2 state machine, the IC also detects a limited number of proprietary charger types (Apple, Samsung, and generic 500mA). The BC1.2 detection block automatically sets the CHGIN input current limiting based on the charger type detection results. If charger type detection results are an unknown charger type, the input current limits are set by $R_{INLIM}$.

## Table 3. BC1.2 Charger Type

| USB BC1.2 DETECTED CHARGER TYPE | |
|---|---|
| INPUT CURRENT LIMIT | CHARGER DETECTED |
| 500mA | No CHGIN |
| 500mA | SDP |
| 1.5A | CDP |
| 1.5A | DCP |

## Table 4. Proprietary Charger Type

| DETECTED PROPRIETARY CHARGER TYPE | |
|---|---|
| **INPUT CURRENT LIMIT** | **CHARGER DETECTED** |
| 500mA | Apple |
| 1A | Apple |
| 2A | Apple |
| 2.4A | Apple 12W |
| 2A | Samsung |
| Programed by $R_{INLIM}$ | Unknown |

### USB Type-C CC Detection

#### Features

- USB Type-C sink and source support
- CC source detection and automatically sets the input current limit according to source capability
- Source role is supported by the ENBST pin.

#### CC Description

The IC works as a Sink compliant to USB Type-C rev1.2. The USB Type-C functions are controlled by a logic state machine that follows the USB Type-C requirements. The IC sets the CHGIN input current limit based on the current advertised on the CC wires. Source role is enabled by the ENBST pin. When the source role is enabled, Rd is removed and a 180µA current source is connected to advertise its current capability.

#### Detecting Connected Source

When a source is detected, the USB Type-C state machine auto-detects the active CC line. The state machine also auto-detects the source advertised current (500mA, 1.5A, and 3.0A). Upon detection of advertised current through the CC pin, the IC automatically sets the input current limit.

#### Enable Source Role

ENBST = high enables the IC's source role. The IC disconnects Rd from the CC line and connects a 180µA current source to advertise the 5V/1.5A power source. The IC enables the reverse boost and supply 5.1V/1.5A through the CHGIN pin.

## Applications Information

The MAX77787 reads in the resistor values ($R_{IFAST}$, $R_{VSET}$, and $R_{INLIM}$) once upon power up. It cannot read the values from the potentiometer at run-time. Depending on the use case, customers should populate the resistor values provided in the *Table 5* to *Table 7*. Using any other value can result in an incorrect setting due to tolerances.

### Input Current Limit Setting

A resistor ($R_{INLIM}$) from INLIM to GND programs the charger input current limit. The input current limit setting through a resistor is valid only when the adaptor is detected as unknown. Else, the input current limit is programmed by D+/D- detection and CC detection results.

## Table 5. Input Current Limit Setting

| $R_{INLIM}$ (kΩ) | INLIM (mA) |
|---|---|
| Unconnected | 500 |
| 24.9 | 500 |
| 22.6 | 600 |
| 20.5 | 700 |
| 18.7 | 800 |
| 16.9 | 900 |
| 15.4 | 1000 |
| 14 | 1150 |
| 12.4 | 1300 |
| 11 | 1500 |
| 9.53 | 1750 |
| 8.2 | 2000 |
| 6.65 | 2250 |
| 5.23 | 2500 |
| 3.6 | 2700 |
| 2.4 | 3000 |

### Termination Voltage Setting

The default charge termination voltage is programmed with the resistance from VSET to GND. See *Table 6*.

## Table 6. Charge Termination Voltage Setting Input (VSET) Setting

| $R_{VSET}$ (kΩ) | CV (V) |
|---|---|
| Unconnected | 3.60 |
| 24.9 | 3.60 |
| 22.6 | 3.70 |
| 20.5 | 3.80 |
| 18.7 | 3.90 |
| 16.9 | 4.00 |
| 15.4 | 4.10 |
| 14 | 4.15 |

| $R_{VSET}$ (kΩ) | CV (V) |
|---|---|
| 12.4 | 4.20 |
| 11 | 4.25 |
| 9.53 | 4.30 |
| 8.2 | 4.35 |
| 6.65 | 4.40 |
| 5.23 | 4.45 |
| 3.6 | 4.50 |
| 2.4 | 4.55 |

### Fast-Charge Current and TOPOFF Current Setting

While a valid input source is present, the battery charger attempts to charge the battery with a fast-charge current determined by the resistance from $I_{FAST}$ to GND. The top-off current is matched to the fast-charge current, *Table 7* shows resistance values which correspond to target $I_{FAST}$ and $I_{TOPOFF}$ values.

## Table 7. Fast-Charge Current and Top-off Current Setting

| RESISTANCE (kΩ) | $I_{FAST}$ (mA) | $I_{TOPOFF}$ (mA) |
|---|---|---|
| Unconnected | 3150 | 150 |
| 24.9 | 3150 | 150 |
| 22.6 | 3000 | 150 |
| 20.5 | 2800 | 125 |
| 18.7 | 2500 | 125 |
| 16.9 | 2400 | 125 |
| 15.4 | 2200 | 100 |
| 14 | 2000 | 100 |
| 12.4 | 1800 | 75 |
| 11 | 1500 | 75 |
| 9.53 | 1400 | 75 |
| 8.2 | 1200 | 50 |
| 6.65 | 1000 | 50 |
| 5.23 | 800 | 50 |
| 3.6 | 600 | 50 |
| 2.4 | 500 | 50 |

### Charger Status Outputs

#### Input Status (INOKB)

INOKB is an open-drain and active-low output that indicates input status. If a valid input source is inserted and the buck converter starts switching, INOKB pulls low. When the reverse boost is enabled, INOKB pulls low to indicate 5V output from CHGIN.

INOKB can be used as a logic output for the system processor by adding a 200kΩ pullup resistor to the system IO voltage.

INOKB can be also used as a LED indicator driver by adding a current limit resistor and a LED to SYS.

**Charging Status (STAT)**

STAT is an open-drain and active-low output that indicates charge status. STAT status changes as shown in *Table 8*.

## Table 8. STAT Output Per Charging Status

| CHARGING STATUS | STAT | LOGIC STATE | CHARGE STATUS LED |
|---|---|---|---|
| No input | High impedance | High | Off |
| Trickle, pre-charge, fast charge | Repeat low and high impedance with 1Hz, 50% duty cycle | After an external diode and a capacitor rectifier, high | Blinking with 1Hz, 50% duty cycle |
| Top-off and done | Low | Low | Solid on |
| Faults | High impedance | High | Off |

STAT can be used as a logic output for the system processor by adding a 200kΩ pullup resistor to system IO voltage and a rectifier (a diode and a capacitor).

STAT also can be used as a LED indicator driver by adding a current limit resistor and a LED to SYS.

### D+/D- Multiplexer (Optional)

USB D+/D- lines, which are used for the detection of BC1.2 and proprietary TA (Travel Adaptor)s, can be used for data communication. If an MCU handles this communication in the target system, the D+/D- lines can be connected to the IC and the MCU like *Figure 12*. As shown in *Figure 12*, switchers are required for each D+ and D- lines to guarantee Hi-Z for the connections to MCU to avoid the wrong detections of TAs. It is recommended to connect the INOKB of the IC to the MCU in this configuration so that the IC can signal the completion of the detection to the MCU. Once the MCU receives a valid INOKB signal, it can switch the D+/D- lines from the IC to the MCU for data communication.

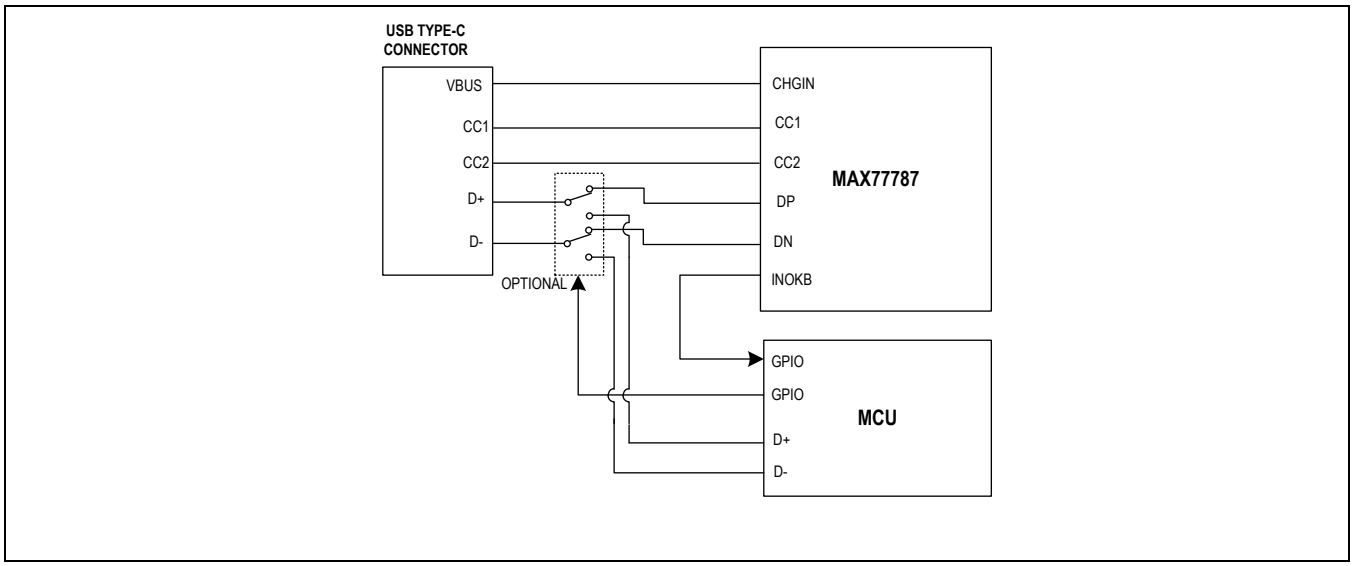



*Figure 12. D+/D- Connections in a Reference System*

### Non-USB Type Power Source

In an application where the power source is not USB, all the USB-related pins such as CC1, CC2, DP, and DN should be left NC (not connected). In this case, the input current to the IC is limited by the $R_{INLIM}$ setting

### Recommended PCB Layout and Routing

Place all bypass capacitors for CHGIN, BYP, SYS, $V_{DD}$, and BATT as close as possible to the IC. Connect the battery to BATT as close as possible to the IC to provide accurate battery voltage sensing. Provide a large copper ground plane to allow the PGND pad to sink heat away from the device. Use wide and short traces for high current connections such as CHGIN, BYP, SYS, and BATT to minimize voltage drops. The IC has two kinds of ground pins, which are PGND and

GND. Care should be taken to connect PGND since it is a switching node ground of the charger buck. It should be tied to the ground of the SYS capacitor and BYP capacitor and connected to the ground plane directly without sharing other ground. The GND can be connected to the ground plane.

*Figure 13* is a recommended placement and layout guide.

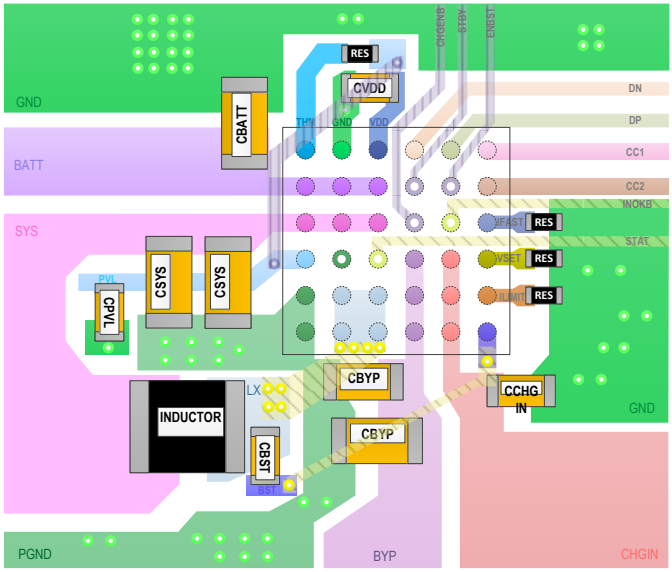



*Figure 13. Recommended Placement and Layout*

### Inductor Selection

The IC's control scheme requires an external inductor from 0.47µH to 1µH for proper operation.

## Table 9. Recommended Inductors

| MANUFACTURER | PART NUMBER | INDUCTANCE (µH) | $I_{SAT(TYP)}$ (A) | $I_{RMS(TYP)}$ (A) | DCR (TYP) (mΩ) | SIZE (L x W x T) (mm) |
|---|---|---|---|---|---|---|
| SEMCO | CIGT252008LMR47MNE | 0.47 | 5.5 | 4.5 | 24 | 2.5 x 2.0 x 0.8 |
| SEMCO | CIGT252010LMR47MNE | 0.47 | 6 | 4.5 | 24 | 2.5 x 2.0 x 1.0 |
| SEMCO | CIGT201610EHR47MNE | 0.47 | 5.9 | 5 | 18 | 2.0 x 1.6 x 1.0 |
| CYNTEC | HTGH25201T-R47MSR-68 | 0.47 | 6.6 | 5.6 | 16.5 | 2.5 x 2.0 x 1.0 |

### Capacitor Selection

All capacitors should be X5R dielectric or better. Be aware that multi-layer ceramic capacitors have large-voltage coefficients. Before selecting capacitors, check sufficient voltage rating and derated capacitance at max operating voltage condition. *Table 10* shows proper capacitors after considering the derating and operating voltage.

## Table 10. Capacitor Selections

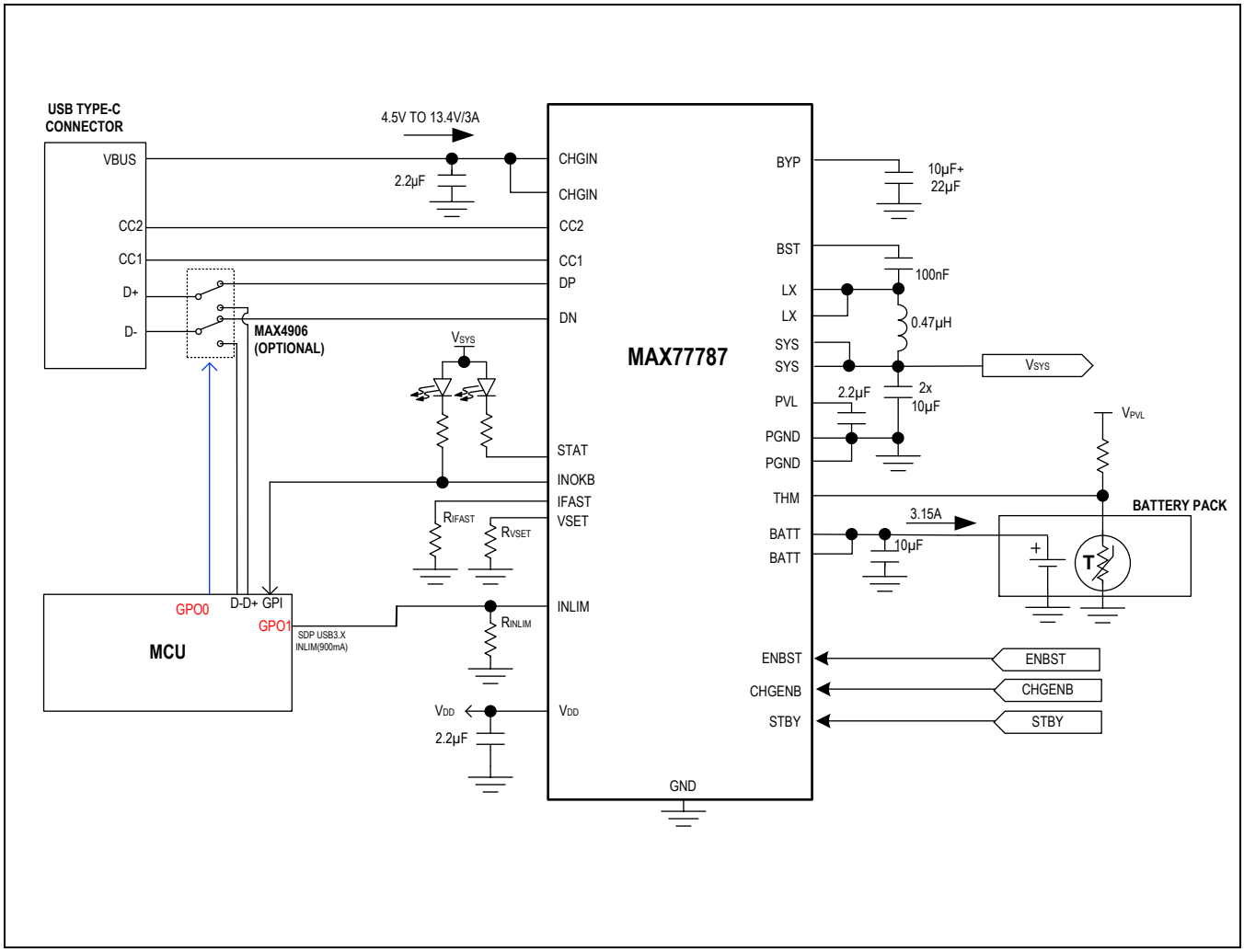
| PIN | TYPE |
|---|---|
| CHGIN Capacitor | 2.2µF/16V |
| BYP Capacitor | 10µF + 22µF/16V |
| SYS Capacitor | 2x10µF/10V |
| BATT Capacitor | 10µF/10V |
| $V_{DD}$ Capacitor | 2.2µF/10V |
| PVL Capacitor | 2.2µF/10V |
| BST Capacitor | 100nF/6.4V |

## Typical Application Circuit

A typical application circuit consists of the device as a single cell battery charger for Li-Ion battery used in a wide range of portable devices. External USB switch is optional for the USB2.0 and USB3.x communication between MCU and the devices in the system. To set the input current limit to SDP 900mA which is the USB3.x device $V_{BUS}$ current capability, MCU shall send in a pulse on the INLIM pin with a pulse width greater than 123µs to set the 900mA option, so that the IC configures input current limit to 900mA.

The procedure for the SDP 900mA INLIM setting is as follows:

- INOKB pulls low when detection is done as SDP.
- MCU controls USB Switch.
- MCU starts enumeration to the USB device attached.
- MCU sends a pulse signal through GPIO1 to the INLIM pin when USB3.x device is recognized.



## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE | THM | BATTERY CHEMISTRY |
|---|---|---|---|---|
| MAX77787JEWX+ | -40°C to +85°C | WLP | JEITA | Li-ion<br>Li-polymer |
| MAX77787JEWX+ T | -40°C to +85°C | WLP | JEITA | Li-ion<br>Li-polymer |
| MAX77787HEWX+ | -40°C to +85°C | WLP | HOT/COLD STOP | LiFePO4 |
| MAX77787HEWX+ T | -40°C to +85°C | WLP | HOT/COLD STOP | LiFePO4 |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape and reel.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 4/22 | Release for Market Intro | — |
| 1 | 5/23 | Added RIFAST, RVSET, and RINLIM read in information in the Applications Information section | 35 |

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