*Click **here** to ask an associate for production status of specific part numbers.*

MAX66301

DeepCover Secure Authenticator with SHA-3 and RFID Reader

General Description

DeepCover® embedded security solutions cloak sensitive data under multiple layers of advanced physical security to provide the most secure key storage possible.

The MAX66301 DeepCover secure authenticator combines a highly integrated RFID reader for contactless communication at 13.56MHz and a SHA-3 secure authenticator coprocessor. The RFID IC reader covers both the ISO 14443 Type A and ISO 15693 standards. The authenticator coprocessor's engine is based on the FIPS 202 standard and supports secure challenge-and-response authentication when paired with peripherals such as the MAX66250 transponder. An embedded host processor can easily interface with the MAX66301 using its UART or SPI interface.

Applications

- Secure Access Control
- Asset-Tracking Readers
- Authentication of Consumables
  - Readers in Printers (Ink Cartridge)
  - Blood Glucose Meters/Monitors
- Handheld Reader Modules

Request MAX66301 Security User Guide

Benefits and Features

- Secure, Contactless Host Authenticator
  - ISO/IEC 15693 and 14443 Type A Standard Compliant
  - SHA-3 Engine to Run a Symmetric Key-Based Bidirectional Secure Authentication
  - Four 32-Byte Pages of User Memory
  - Four Main Secrets with Multiple Programmable Protection Options
  - 76-Byte Scratchpad in SRAM
  - True Hardware Random-Number Generator
  - Unique 64-Bit Serial Number
- Design Flexibility Supports Diverse Applications
  - UART and SPI Interface Ports
  - Power-Down Mode Selectable by an Input Pin (Low, Standby Power)
  - Antenna Short-Circuit Protection
  - Compatible with 3.3V or 5V Supply Voltages
  - ±2kV HBM ESD Protection
- Scalable 13.56MHz Analog Front-End Provides Support for Multiple Antenna Configurations
  - Single- or Double-Antenna Driver Using On-Off Keying (OOK) Modulation
  - User-Selectable ASK Uplink Modulations Index Adjustable from 7% to 30%
  - High-Output RF Power of up to 200mW
  - Multiple Receiver Inputs for High-Communication Reliability
  - Built-In Receiver Lowpass-Filter Cutoff Frequencies Selectable Between 400kHz and 1MHz
  - Selectable Built-In Receiver Highpass-Filter Cutoff Frequency: 100kHz, 200kHz, and 300kHz
  - Selectable Receive Gain from 0dB up to 40dB
  - Multiple Subcarrier Receiving Compatibility
  - (212kHz and 424kHz)
- Antenna Short-Circuit Protection Enhances System Ruggedness

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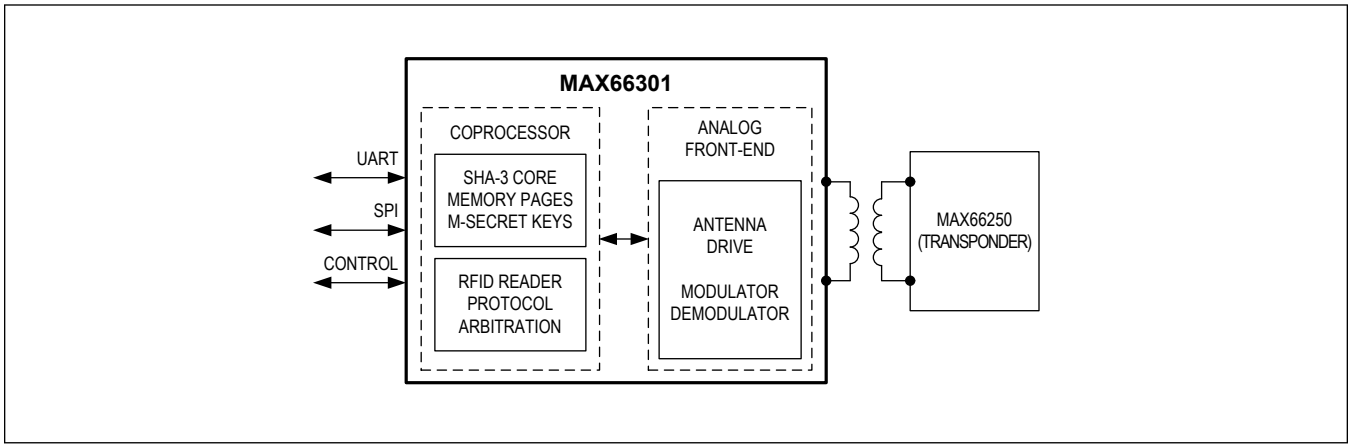
***Ordering Information** appears at end of data sheet.*

19-101476; Rev 0; 6/22

Typical Application Circuit



Absolute Maximum Ratings

Continuous Power Dissipation (T_A = +70°C)
TQFN (multilayer board) .....
(derate 47.6mW/°C above +70°C) 1.9W
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range (*Note 1*) ..... -55°C to +120°C
Maximum Junction Temperature ..... +110°C
Lead Temperature (soldering, 10s) ..... +300°C
ESD Protection per Method 3015 ..... ±2kV
(Applies to Pins 1–32 and 52–56)
Voltage Range on V_{DD}_CORE, V_{DDQ} ..... -0.3V to +3.6V
Voltage Range on Any Input
or Bidirectional Pin ..... -0.3V to the lesser of ((V_{DD_CORE} +3.6V), 5.5V) for the max
Voltage Range on HFXIN ..... -0.3V to (V_{DD_CORE} + 0.5V)
Continuous Output Current on Any Single I/O Pin 25mA
(Applies to Pins 33–51)
Voltage Range on V_{DDA1}, V_{DDA2},
and $V_{DD\_AFE\_DIG}$ ..... -0.3V to +6V
Maximum Voltage Range on Any Input
or Bidirectional Pin ..... $V_{DD\_AFE\_DIG}$ + 0.3V
Minimum Voltage Range on
Any Input or Bidirectional Pin ..... V_{SS} - 0.3V
Maximum Output Current on
Any Single I/O Pin except ANT1 and ANT2 ..... 10mA
Maximum AC Peak Current on ANT1 and ANT2 ..... 100mA
ESD Protection per Method 3015 on ANT1 and ANT2 ..... ±4kV

Note 1: Storage temperature is defined as the temperature of the device when all supply voltages are 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56 TQFN-EP

Package Code	T5688M+3
Outline Number	21-0135
Land Pattern Number	90-0047
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	21°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Digital limits are 100% tested at T_A = +25°C and T_A = +85°C. Analog front-end limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. V_{DDQ} = V_{DD_CORE}; V_{DD} = V_{DDA1} = V_{DDA2} = $V_{DD\_AFE\_DIG}$; V_{SS} = V_{SSA1} = V_{SSA2} = 0V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL (APPLIES TO PINS 1–32 AND 52–56)						
Operating Supply Voltage	V_{DD_CORE}		V_{RST}	3.3	3.6	V
Power-Fail Warning Voltage	V_{RST}	Brownout detection	2.8		3.0	V
Reset Mode Current ($\overline{RESET}$)	I_{DD1}	External 24MHz clock source generates system clock; device in reset		12	20	mA

Electrical Characteristics (continued)

(Digital limits are 100% tested at T_A = +25°C and T_A = +85°C. Analog front-end limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. V_{DDQ} = V_{DD_CORE}; V_{DD} = V_{DDA1} = V_{DDA2} = $V_{DD\_AFE\_DIG}$; V_{SS} = V_{SSA1} = V_{SSA2} = 0V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, External Clock Source	I_{DD2}	External 24MHz clock source generates system clock; code running from data memory; CSAM subcommand loop		14.4		mA
Sleep Mode Current (SLEEP)	I_{SLEEP}	T_A = +25°C, V_{DD_CORE} = 3.6V, SLEEP = GND, all other pins disconnected		2.3		mA
I/O Supply Output High Voltage	V_{DDIOH}	V_{DDIOH} current is the sum of V_{DDIO} current and I_{OH1} of all I/O, I_{OH1} = 20mA	V_{DD_CORE} -0.4		V_{DD_CORE}	V
Input Low Voltage (HFXIN)	V_{IL1}		V_{GND}		0.4	V
Input Low Voltage (Any I/O)	V_{IL2}		V_{GND}		0.2 x V_{DD_CORE}	V
Input High Voltage (HFXIN)	V_{IH1}		0.7 x V_{DDIO}		V_{DD_CORE}	V
Input High Voltage (Any I/O)	V_{IH2}		0.7 x V_{DDIO}		5.5	V
Input Hysteresis (Schmitt)	V_{IHYS}			0.5		V
Output Low Voltage	V_{OL1}	I_{OL1} = 4mA, V_{DDIO} = 3.0V	V_{GND}		0.4	V
Output High Voltage	V_{OH1}	I_{OH1} = -4mA, V_{DDIO} = 3.0V	V_{DDIO} - 0.6		V_{DDIO}	V
Input Crystal Capacitance	C_{IN}	Not production tested		6		pF
Input Leakage Current	I_{LEAK}	$V_{GND} \le V_{IN} \le 5.5V$ (*Note 2*)	-10		+10	µA
Input Pull-up Current (Any I/O)	I_{PU}			-85		µA
Pull-up Resistor ($\overline{RESET}$	R_{PU}		20	40	55	kΩ
VOLTAGE SENSOR						
V_{VDD_CORE} High Reset Overvoltage Threshold	$V_{DD\_CORE\_OV}$		4.0		4.6	V
REG18 Overvoltage Reset Threshold	V_{REG18_OV}			2.6		V
CLOCK SOURCE						
External-Crystal Frequency Between HFXIN and HFXOUT	f_{HFXIN}		23.95	24	24.05	MHz
External-Clock Oscillator Frequency on HFXIN	f_{HFXIN}		23.95	24	24.05	MHz
External-Clock Period Duty Cycle	t_{CLDC}		45		55	%

Electrical Characteristics (continued)

(Digital limits are 100% tested at T_A = +25°C and T_A = +85°C. Analog front-end limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. V_{DDQ} = V_{DD_CORE}; V_{DD} = V_{DDA1} = V_{DDA2} = $V_{DD\_AFE\_DIG}$; V_{SS} = V_{SSA1} = V_{SSA2} = 0V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Rise Time	t_{CR}				3	ns
MEMORY CHARACTERISTICS						
t_{PROG}				27		ms
Write/Erase Cycles				20,000		cycles
Data Retention		T_A = +25°C		100		years
SPI ELECTRICAL CHARACTERISTICS (Figure 5)						
SPI Peripheral Operating Frequency	$1/t_{SCK}$	f_{CK} = f_{HFXIN}			$f_{CK}/4$	MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, pull-up = 560Ω	8.3		23.6	ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSEL Active to First Shift Edge	t_{SSE}		t_{SPI_RF}			ns
MOSI Input to SCLK Sample Edge Rise Setup	t_{SIS}		t_{SPI_RF}			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		t_{SPI_RF}			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				$2t_{SPI\_RF}$	ns
SSEL Inactive	t_{SSH}	f_{CK} = $1/f_{HFXIN}$	t_{CK} + t_{SPI_RF}			ns
SCLK Inactive to SSEL Rising	t_{SD}		t_{SPI_RF}			ns
MISO Output Disabled After SSEL Edge Rise	t_{SLH}	f_{CK} = $1/f_{HFXIN}$			$2t_{CK}$ + $2t_{SPI\_RF}$	ns
SSEL Rising to Active BUSY	t_{SAB}		2			µs
SCLK Delay Between Bytes	t_{SDLY}			3		µs
SHA-3 ENGINE						
Computation Time	t_{CSHA}			80		ms
ANALOG FRONT-END (APPLIES TO PINS 33–51)						
Supply Voltage	V_{DD}	3.3V	3.3	3.45	3.6	V
		5.0V (Note 3)	4.5	5.0	5.5	
Sleep Mode Current (SLEEP)	I_{PD}			1	5	µA
Supply Current Excluding Antenna Driver Current	I_{ON}	3.3V (Note 4)		8.5	12	mA
		5.0V		12	20	

Electrical Characteristics (continued)

(Digital limits are 100% tested at T_A = +25°C and T_A = +85°C. Analog front-end limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. $V_{DDQ} = V_{DD\_CORE}$; $V_{DD} = V_{DDA1} = V_{DDA2} = V_{DD\_AFE\_DIG}$; $V_{SS} = V_{SSA1} = V_{SSA2}$ = 0V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AGD Level	V_{AGD}	3.3V (*Note 4*)	0.7	1.3	1.6	V
		5.0V	2.3	2.5	2.7	
Power-On Reset Level	V_{POR}	3.3V		2.1		V
		5.0V	1.4	2.1	3.6	
ANTENNA DRIVERS						
Driver Output Impedance (ANT1 or ANT2)	R_{AD}	3.3V, I_{ANT} = 100mA, 100% modulation index	4	9.3	15	Ω
		3.3V, I_{ANT} = 30mA, 10% modulation index	5	11	20	
		5.0V, I_{ANT} = 100mA, 100% modulation index	3	7	12	
		5.0V, I_{ANT} = 100mA, 10% modulation index	5	10	15	
SPECIAL-PURPOSE PINS (SYSAOUT, SYSBOUT, SYSCOUT, SYSDOUT, SYSEOUT)						
Input Low Voltage	V_{IL}				0.2 x V_{DD}	V
Input High Voltage	V_{IH}		0.8 x V_{DD}			V
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.1 x V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	0.9 x V_{DD}			V
Interface Clock Rate Frequency (SYSCOUT)	f_{MAX}				1	MHz
AM DEMODULATION						
RF Amplitude of RFIN Inputs	V_{RFIN}	3.3V		1.65		V_{P-P}
		5.0V		2.5		
RFIN Input Resistance	R_{RFIN}	3.3V, 5.0V	5	15.5	20	kΩ
Receiver Sensitivity at 212kHz	V_{SENS}	3.3V		0.75		mV_{P-P}
		5.0V		1.5		
Receiver Sensitivity at 24kHz	V_{SENS}	3.3V		0.8		mV_{P-P}
		5.0V		2.2		
Receiver Sensitivity at 848kHz	V_{SENS}	3.3V		1.95		mV_{P-P}
		5.0V		3.5		
Recovery Time of Reception after Antenna Modulation	t_{REC}				100	µs

Electrical Characteristics (continued)

(Digital limits are 100% tested at T_A = +25°C and T_A = +85°C. Analog front-end limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. V_{DDQ} = V_{DD_CORE}; V_{DD} = V_{DDA1} = V_{DDA2} = $V_{DD\_AFE\_DIG}$; V_{SS} = V_{SSA1} = V_{SSA2} = 0V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
XTAL OSCILLATOR (OSCIN, OSCOUT)						
Transconductance	g_M	3.3V, normal mode		0.45		mS
		3.3V, high-oscillator mode		2		
		5.0V, normal mode (*Note 5*, *Note 6*)		0.9		
		5.0V, high-oscillator mode (*Note 6*)		2.7		
Set-Up Time after Power Down	t_{SET}			5	15	ms
Input Crystal Capacitance	C_{INPUT}	Not production tested		22		pF

Note 2: Any tolerant I/O pin, when an input with no internal weak pull-up, can reach a peak static current of 45µA (typ) at V_{DD_CORE} + 0.4V.

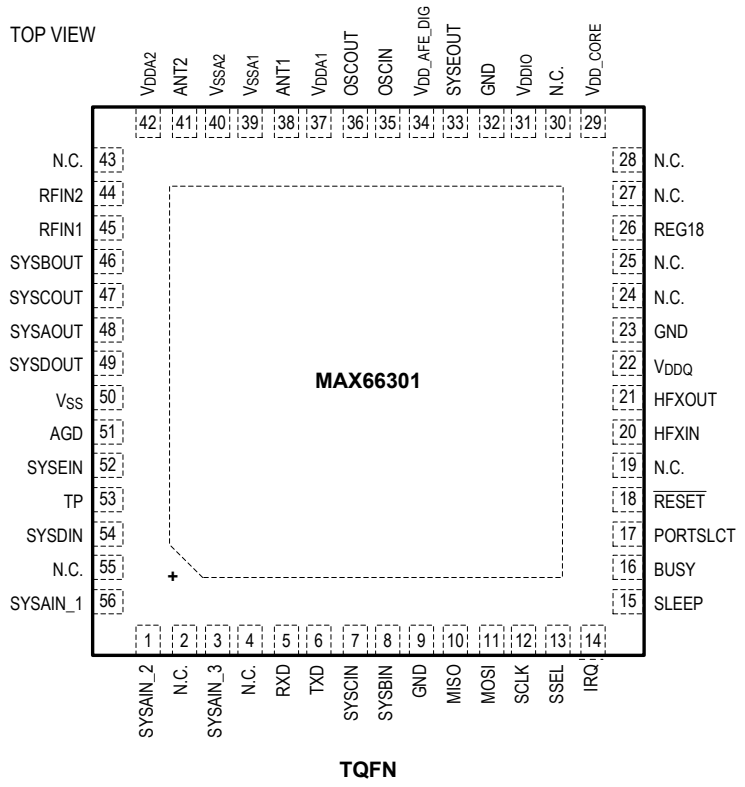
Note 3: Due to the 10kΩ ±5% resistor pull-ups on pins SYSBIN, SYSCIN, and SYSEIN in 5V operation, V_{DD_CORE} needs to be present at or before $V_{DD\_AFE\_DIG}$.

Note 4: Includes external 1.8kΩ ±5% resistor connected on AGD output to fix a voltage on the pin of 1.3V.

Note 5: Recommended to use the high g_M transconductance (i.e., high oscillator mode).

Note 6: Recommended to use the following crystal electrical parameters: quality factor min of 26,000, series resistance typical of 20Ω, and a static capacitance typical of 2.8pF.

Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1	SYSAIN_2	Special-Purpose Pin. Must be connected to SYSAOUT. This pin is 5V tolerant.
2, 4, 19, 24, 25, 27, 28, 30, 43, 55	N.C.	No Connection
3	SYSAIN_3	Special-Purpose Pin. Must be connected to SYSAOUT. This pin is 5V tolerant.
5	RXD	UART Receive. Data input from host. This pin is 5V tolerant.
6	TXD	UART Transmit. Data output to host. This pin is 5V tolerant.
7	SYSCIN	Special-Purpose Pin. This pin must be connected to SYSCOUT. Also, this pin must be pulled up with a 10kΩ ±5% resistor to the same voltage potential as $V_{DD\_AFE\_DIG}$.
8	SYSBIN	Special-Purpose Pin. This pin must be connected to SYSBOUT. Also, this pin must be pulled up with a 10kΩ ±5% resistor to the same voltage potential as $V_{DD\_AFE\_DIG}$.
9	GND	Digital Ground
10	MISO	Controller In-Peripheral Out. The MISO pin is used to transfer data out of the MAX66301. During a read cycle, data bytes are shifted out on this pin after the falling edge of the serial clock. This pin is 5V tolerant.

Pin Description (continued)

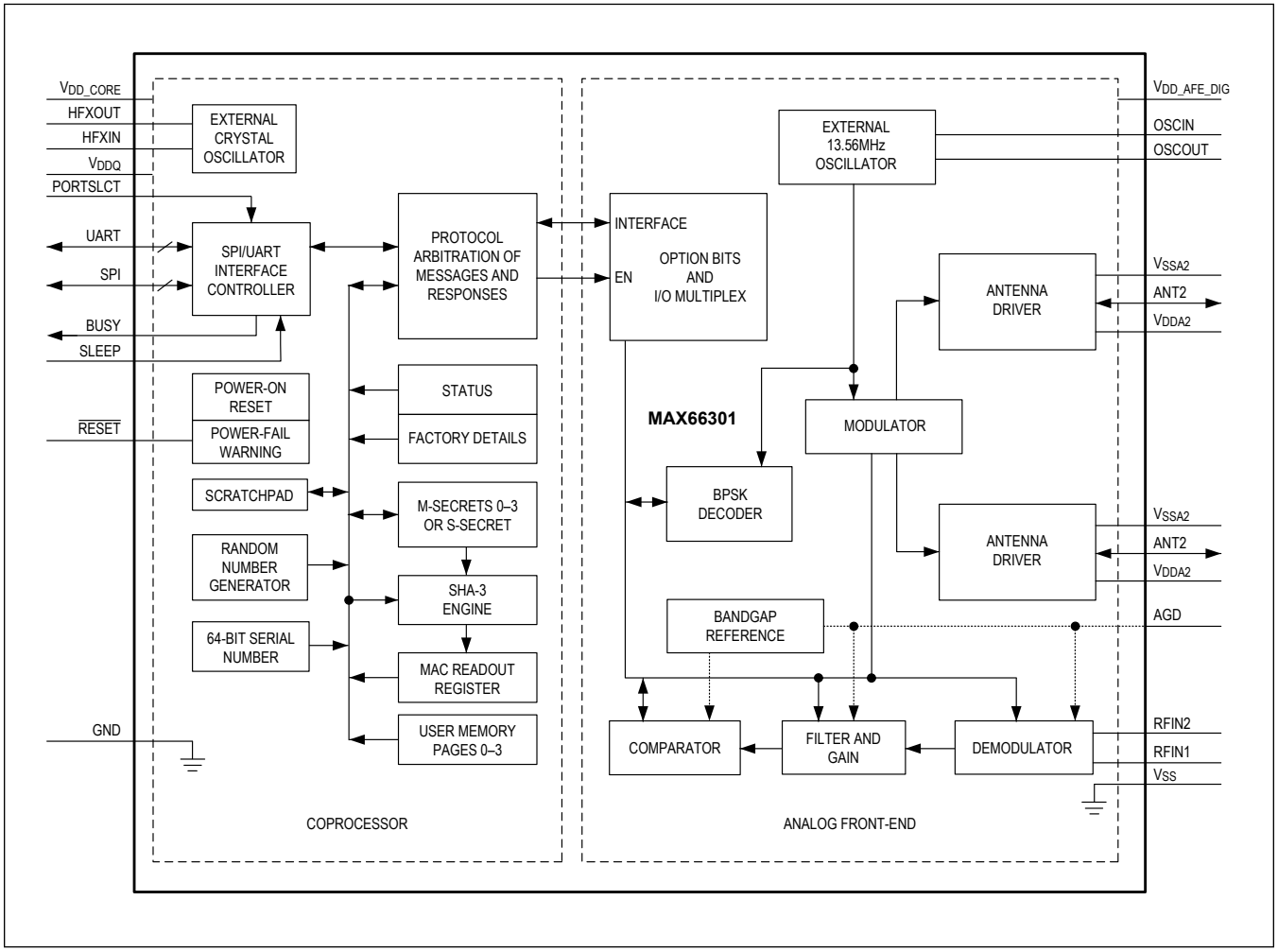
PIN	NAME	FUNCTION
11	MOSI	Controller Out-Peripheral In. The MOSI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock. This pin is 5V tolerant.
12	SCLK	Serial Clock. The SCLK pin is used to synchronize the communication between host processor (controller) and the MAX66301. Data bytes present on the MOSI pin are latched on the rising edge of the clock input, and data bytes on the MISO pin are updated after the falling edge of the clock input. This pin is 5V tolerant.
13	SSEL	Peripheral Select. A low level on the SSEL pin selects the device; a high level deselects the device. When the MAX66301 is deselected, MISO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. This pin is 5V tolerant.
14	IRQ	Interrupt Out. This pin drives low when an interrupt has occurred. Otherwise, the pin is in high impedance. This pin is 5V tolerant.
15	SLEEP	Sleep Mode In. This pin is used to put the device into low-power mode when set low. This device comes out of low-power mode and into normal operation within 20ms of transition from low to high logic state. This pin is 5V tolerant.
16	BUSY	Busy Out. This pin indicates a transaction is in progress when driving high and that no messages should be sent to the device. When driving low, the device is ready to accept new messages. Note that, in UART mode, BUSY is not required since communication is asynchronous.
17	PORTSLCT	Port Select In. After a reset, this pin is sampled within 20ms. If the sample detects logic-low, the UART port is enabled and the SPI port is disabled. If the sample detects logic-high, the SPI port is enabled and the UART port is disabled. This pin is 5V tolerant.
18	$\overline{\text{RESET}}$	Active-Low Reset. This bidirectional pin recognizes external active-low reset inputs and uses an internal pull-up resistor to allow for a combination of wired-OR external reset sources. An RC is not required for power-up, as this function is provided internally. This pin also acts as an output when the source of the reset is internal to the device (such as the exception handling of an incorrect message). In this case, the pin is low while the processor is in a reset state and returns high as the processor exits this state. This pin is 5V tolerant.
20	HFXIN	High-Frequency Crystal Input. Connect an external 24MHz crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, if a more accurate external system clock is available, HFXIN can be the input for a 24MHz clock source.
21	HFXOUT	High-Frequency Crystal Output. Connect an external 24MHz crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, if a more accurate external system clock is available, HFXOUT can be left unconnected.
22	V_{DDQ}	Digital Supply. Connect to V_{DDIO} through a 50Ω 1µF capacitor filter.
23	GND	Digital Ground
26	REG18	Regulator Capacitor. This pin must be connected to ground through a 1.0µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin. No devices other than the capacitor should be connected to this pin.
29	V_{DD_CORE}	Digital Core Supply Voltage. +3.3V nominal supply voltage.
31	V_{DDIO}	Switched I/O Power Supply (Internally Connected to V_{DD_CORE}). This output pin must be connected to ground through a 1.0µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin. No devices or power rail other than the capacitor and V_{DDQ} through a filter should be connected to this pin.
32	GND	Digital Ground
33	SYSEOUT	Special-Purpose Pin. This pin must be connected to SYSEIN.
34	$V_{DD\_AFE\_DIG}$	Digital Supply Voltage for the Analog Front-End. This pin can operate at 3.3V or 5V. This pin has to be the same voltage potential as V_{DDA1} and V_{DDA2}. This pin must be connected to ground through a 0.1µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin. No devices other than the capacitor should be connected to this pin.

Pin Description (continued)

PIN	NAME	FUNCTION
35	OSCIN	Quartz Oscillator Input. This pin receives a voltage from an external resonant crystal to drive an internal inverter to drive that crystal in order to generate the needed RF frequencies for the analog front-end. This pin requires a standard 13.56MHz ±7kHz quartz crystal. A CoG-rated capacitor should be used for loading with a typical value of 22pF for each pin.
36	OSCOUT	Quartz Oscillator Output. This pin drives an external resonant crystal in order to generate the needed RF frequencies for the analog front-end. This pin requires a standard 13.56MHz ±7kHz quartz crystal. A CoG-rated capacitor should be used for loading with a typical value of 22pF for each pin.
37	V_{DDA1}	Positive Supply for Antenna Driver. This pin is to be separately filtered from any of the digital supplies and lumped together with V_{DDA2}. Variations in this supply voltage directly modulate the antenna driver and effect the receiver's input. The power-supply sensitivity range, for frequency components that are in the receiving bandwidth, is the same as the RFIN sensitivity. The ground pins used for V_{DDA1} and V_{DDA2} of the antenna driver are V_{SSA1} and V_{SSA2}. Decouple V_{DDA1}/V_{DDA2} to V_{SSA1}/V_{SSA2} with the following types of capacitors; use C0D ceramic technology (±5%) for the 10nF capacitors, use X7R ceramic technology (±10%) for the 100nF capacitors, and use tantalum electrolytic technology for the 3.3µF capacitors.
38	ANT1	RF Output (10Ω Output Impedance). This pin is the output of the antenna driver. Connect to external antenna components.
39	V_{SSA1}	Negative Supply for Antenna Driver (0V). This pin is the ground pin for the antenna driver. This pin must be separately filtered from any of the digital supplies and lumped together with V_{SSA2}.
40	V_{SSA2}	Negative Supply for Antenna Driver (0V). See the V_{SSA2} pin description.
41	ANT2	RF Output (10Ω Output Impedance). This pin is the output of the antenna driver. Connect to external antenna circuit.
42	V_{DDA2}	Positive Supply for Antenna Driver. See the V_{DDA1} pin description. Decouple V_{DDA1}/V_{DDA2} to V_{SSA1}/V_{SSA2} with the following types of capacitors; use C0D ceramic technology (±5%) for the 10nF capacitors, use X7R ceramic technology (±10%) for the 100nF capacitors, and use tantalum electrolytic technology for the 3.3µF capacitors.
44	RFIN2	RF Input (DC-Coupled to AGD). One of two input pins to be connected with external components to detect the amplitude of load-modulated signals, preferably at two different points in antenna matching network.
45	RFIN1	RF Input (DC-Coupled to AGD). One of two input pins to be connected with external components to detect the amplitude of load-modulated signals, preferably at two different points in antenna matching network.
46	SYSBOUT	Special-Purpose Pin. This pin must be connected to SYSBIN.
47	SYSCOUT	Special-Purpose Pin. This pin must be connected to SYSCIN.
48	SYSAOUT	Special-Purpose Pin. Must be connected to SYSAIN_1, SYSAIN_2, and SYSAIN_3.
49	SYSDOUT	Special-Purpose Pin. Must be connected to SYSDIN.
50	V_{SS}	Ground (Analog Ground of RF AFE)
51	AGD	Reference Voltage Output 2.5V. This pin is to be connected to a 0.1µF X7R capacitor to ground when $V_{DD\_AFE\_DIG}$ is 5V. This pin is to be connected to an external resistor to ground to fix the voltage at 1.3V when $V_{DD\_AFE\_DIG}$ is 3.3V.
52	SYSEIN	Special-Purpose Pin. This pin must be connected to SYSEOUT. Also, this pin must be pulled up with a 10kΩ ±5% resistor to the same voltage potential as $V_{DD\_AFE\_DIG}$.
53	TP	Test Pin. This pin is to be pulled up for standard operation to V_{DD_CORE}.
54	SYSDIN	Special-Purpose Pin. Must be connected to SYSDOUT. This pin is 5V tolerant.
56	SYSAIN_1	Special-Purpose Pin. This pin must be connected to SYSAOUT. This pin is 5V tolerant.
—	EP	Exposed Pad

Functional Diagrams

Block Diagram



Detailed Description

The RFID reader's analog front-end (AFE) function is highly integrated into the MAX66301 to support contactless communication at 13.56MHz for compliancy with the ISO/IEC 15693 and ISO/IEC 14443 Type A standards. The host configures this reader with ease and flexibility. This is accomplished through single configuration byte writes to the AFE. The AFE operates at 3.3V or 5V. The reader's push-pull transmitter generates up to 200mW output RF power, depending on the antenna configuration design selected. The output stage drivers are capable of on-off keying (OOK) and amplitude shift keying (ASK) modulation from 7% up to 30% of AM modulation. See the *Block Diagram* for details.

The MAX66301 has a built-in SHA-3 engine and user memory space divided into four pages. Its core operates at 3.3V with 5V-tolerant I/O. The device's coprocessor computes a unique Secondary secret (S-Secret) from any one of four Main secrets (M-Secrets) and additional data. Once the S-Secret is computed, the coprocessor computes authentication MACs (to verify a transponder's authenticity). The same S-Secret in the coprocessor generates write MACs. For example, a write MAC permits writing to the memory and protection registers of a secure memory in a transponder. If the memory is not write-protected, a new M-Secret can be loaded directly, as well as additional data. In addition, the coprocessor can authenticate the MAX66250 by knowing its transponder UID with a single message and response, greatly relieving the host's burden. This only requires that both the MAX66301 and MAX66250 have been properly set up with secrets. This can be achieved by using Analog Devices' preprogramming service.

Functional Description

Coprocessor

The MAX66301 coprocessor analyzes command IDs and payload received from the host. Next, the coprocessor communicates with the AFE to send and capture data from a transponder. The coprocessor then returns the proper responses and payload to the host after it has analyzed the received data bytes. The ISO 15693 uplink encoding supported in the MAX66301 is the "1 out of 4" pulse position encoding scheme. The other encoding scheme supported on the ISO 15693 standard, "1 out of 256," is not supported in the MAX66301. In ISO 14443 Type A, the coprocessor generates modified Miller encoding and then decodes received responses of Manchester data at 106kbps. Additionally, the coprocessor also performs all of the SHA-3 computations necessary for all secure transactions. Doing so helps to reduce host processing time during a transponder authentication session. The coprocessor operates a 3.3V and requires a clock running at 24MHz with an external crystal for greater accuracy.

AFE Power-Supply Considerations

The MAX66301 AFE can operate at 3.3V or 5V. The supply voltages to power the AFE must be the same on both the analog and digital input lines ($V_{DD\_AFE\_DIG}$, V_{DDA1}, V_{DDA2}). It is strongly recommended to use a regulated supply. Power-supply ripples and noise inside the receiver frequency range degrade the overall performance of the system. An external resistor must be added to the AGD output to use the AFE at 3.3V. Doing so fixes the voltage level on AGD to 1.3V. For power efficiency reasons, the external resistor can be switched off (using for example a microcontroller I/O) when the MAX66301 is not used or is in sleep mode.

Power Management

There are two available power modes. The selection of these two modes is done by setting the PUF bit to logic-low. Here are the two modes:

- Reset the power-up flag in the configuration word (option bit 0), which turns off the AFE only. The coprocessor and UART/SPI interface continue to run.
- Apply a low level on the SLEEP pin input. In this case, the AFE goes to sleep and the coprocessor, including the UART/SPI, changes to sleep mode.

When the SLEEP pin input is changed to high (PUF is high), the MAX66301 goes immediately to the mode in which it was before the SLEEP pin went to a low level.

Bandgap Reference

A reference voltage (2.5V) is generated internally by a bandgap reference and uses an external capacitor for blocking.

Antenna Drivers

The antenna driver produces the RF signal from the oscillator output. The pMOS and nMOS driver sides are fed by nonoverlapping signals (3ns) to minimize the power consumption. The output resistance of each antenna driver is typically 7Ω. The two integrated antenna drivers can be used in three possible configurations, depending on the output power level desired. When a single driver configuration is selected, the output power level on the 50Ω load is 100mW. For an output power of 200mW, both drivers must be used in a parallel configuration fashion to double the output power (option bit 5). The drivers can operate in a push-pull configuration (option bit 6). This mode can used in case of a direct antenna connection configuration. In that configuration, the reader's antenna is connected to the output drivers through a resonant capacitor (LC tank adjusted to 13.56MHz). In the direct antenna configuration, the user can achieve an RF output power above 200mW. To be compliant with emissions regulation in certain countries (such as FCC in the U.S.), it could be necessary to add a filtering structure between the device output state drivers and the antenna. The short-protection circuit (option bit 4) prevents damage to the output driver when the ANT pin is shorted to ground or to the AFE's power supply.

Modulator

The modulator enables OOK or ASK modulation of the RF signal on the antenna outputs (ANT1 and ANT2). The reader can cause a low field (ASK modulation index as in Figure 2) or a field-stop (OOK modulation as in Figure 1). The selection between OOK and ASK modulation depth is done using configuration word (option bits 1, 2, and 3). The field modulation index can be adjusted from 7% up to 30% covering all the ISO standard air interface requirements. Before and after a modulation phase, the receiver input is disconnected from the antenna circuitry to preserve DC operating point setting. For high-quality factor systems, it may be necessary to prolong (option bit 24) the hold time after modulation to allow settling of the resonant circuit.

Receiver

The receiver senses the envelope of the signal present on the inputs RFIN1 or RFIN2 (option bit 13). These two inputs, used with external components, permit the detection of amplitude or phase modulated signals. Any RF frequency components still present in the envelope signal are removed by a second-order lowpass filter. The received signal DC component is removed by the highpass filter, which has selectable corner frequency (option bits 7 and 8). The signal is amplified and further processed by the lowpass filtering stage, which corner frequency is selectable (option bit 9). The gain selection (option bits 10, 11, and 12) should be chosen according to the reader system parameters. Modifying the signal bandwidth changes the noise level and results in different input sensitivity.

AGC System

The integrated AGC system can be activated by the configuration word (option bit 14). The AGC amplifier has a 40dB gain correction depth. The AGC system is adapted to all RFID communication protocols. Before the transponder starts to emit the data, the receiver gain is set to maximum (option bits 10, 11, and 12). When the reader detects a transponder signal that is above the attack threshold, the receiver gain is rapidly reduced (option bits 17 and 18) to fit the signal into the linear range of the receiver. The gain remains unchanged as long as the signal level is above the decay threshold. When the received signal falls below the decay threshold for a period of time set by option bits 19 and 20, the reader logic establishes that the communication with one transponder is finished and makes a fast decay to return to the maximum gain. The receiver is ready to demodulate the emission of the next transponder, which can be far away from the reader antenna. This feature is necessary for anticollision purposes. With transponders that have a modulation DC level shift significantly higher than the modulation subcarrier AC level, the AGC can react on DC shift and decrease the system gain too much. It is possible not to attack the first pulse (option bit 15) in a burst (for OOK modulation) to allow the DC level to settle before AGC action. The time after which the first pulse in a burst is not attacked (shortest subcarrier stop in OOK modulation is 1/10 of the time) is set as the decay wait time by option bits 19 and 20. It is also possible to use slow decay mode (option bit 16). The slow decay is started when the received signal falls below the decay threshold. The decay rate is one gain step per time defined by option bits 19 and 20. When the AGC system is disabled, the receiver gain is directly controlled by option bits 10, 11, and 12.

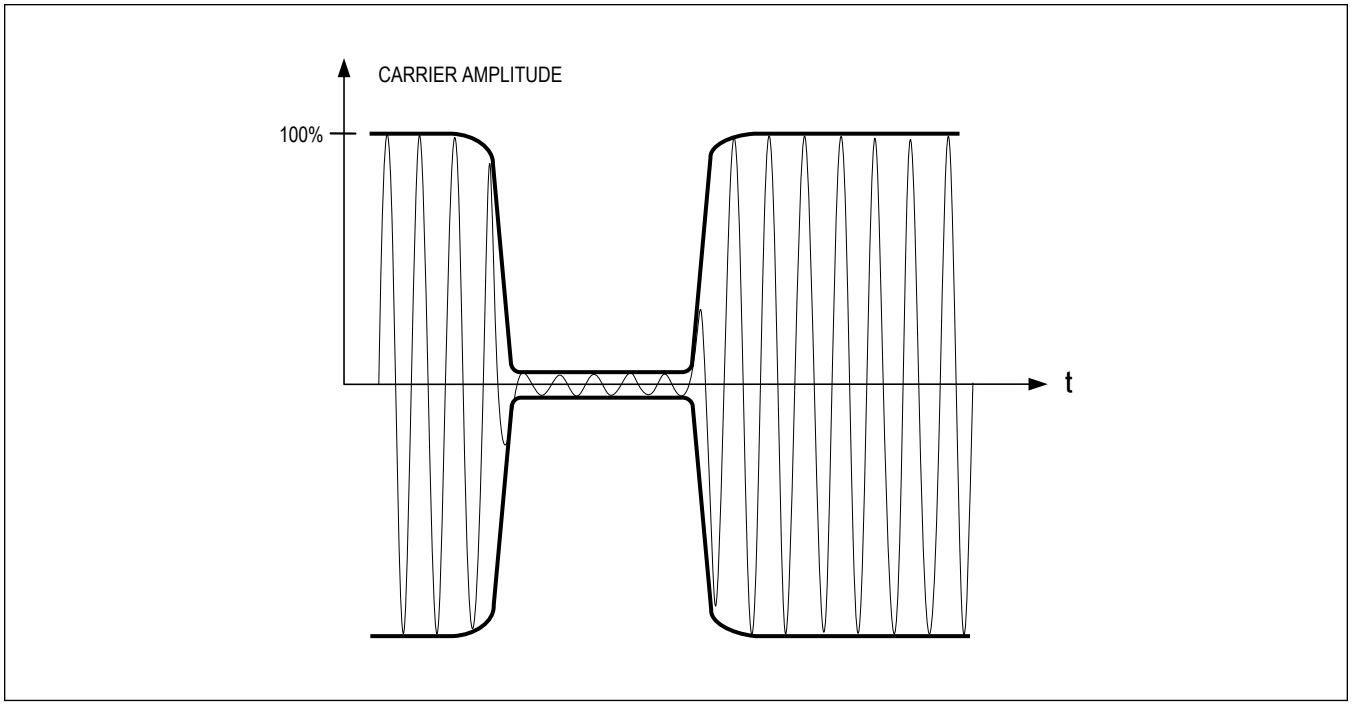


Figure 1. Transmitter Field on ANT1 for Modulation Set to OOK (100% AM)

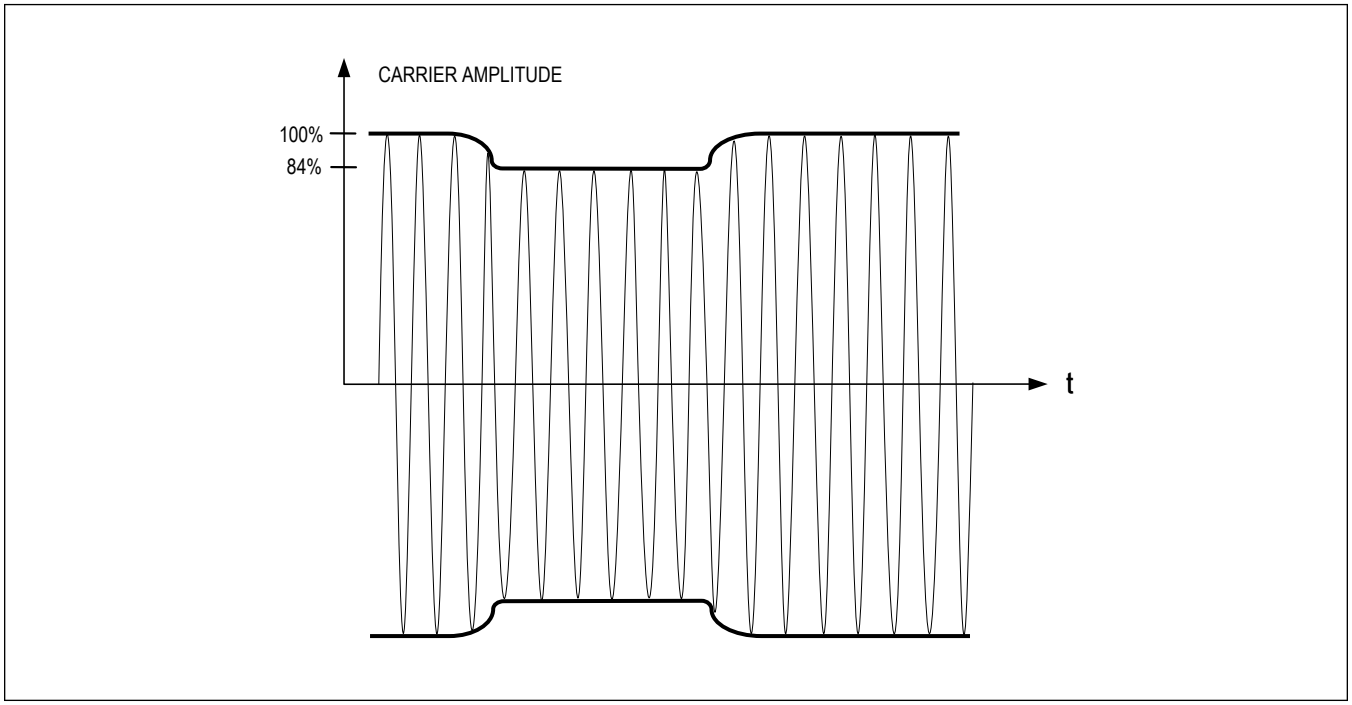


Figure 2. Transmitter Field for ANT1 for Modulation Set to ASK (16% AM)

UART

The universal asynchronous receiver-transmitter (UART) interface provides transmit and receive signals to communicate

with PCs, modems, and other similar interfaces when paired with an external RS-232 line driver/receive. This device provides asynchronous, full-duplex communication (i.e., baud rate: 38400, data: 8 bit, parity: none, stop: 1 bit, flow control: none).

SPI Interface

The MAX66301 is a peripheral device that communicates with its controller—a microcontroller—through the serial SPI interface. This interface uses the signals SSEL, SCLK, MOSI, and MISO. The SPI protocol defines communication in full bytes with the most significant bit being transmitted first. Every SPI communication sequence begins with at least 1 byte written to the peripheral device. The first byte that the peripheral receives from the controller is understood as the beginning of the message. Depending on the first few message bytes, the peripheral may need more bytes (more message data to complete the message), for a read function, after having received the beginning response message bytes, the peripheral starts sending data to the controller. The SPI protocol knows four communication modes, which differ in the polarity and phase of the SCLK signal. The MAX66301 supports MODE (0/0). See the timing specification in Figure 3.

The read timing of these graphics begins with the first bit that the MAX66301 transmits to the controller and ends when the controller ends the communication by deactivating SSEL (low to high transition). The data on the MOSI is latched (sampled) on the SCLK's rising edge, and the data on the MISO is updated (shifted out) on a falling edge of SCLK. Also, the first bit on the MOSI is latched on the first leading rising edge of SCLK. So data on the MOSI needs to be stable for at least a t_{SIS} before the first SCLK cycle for the MAX66301. Therefore, the first bit transmitted from the MISO is updated at least a half cycle before the first SCLK cycle to meet the controller's setup time.

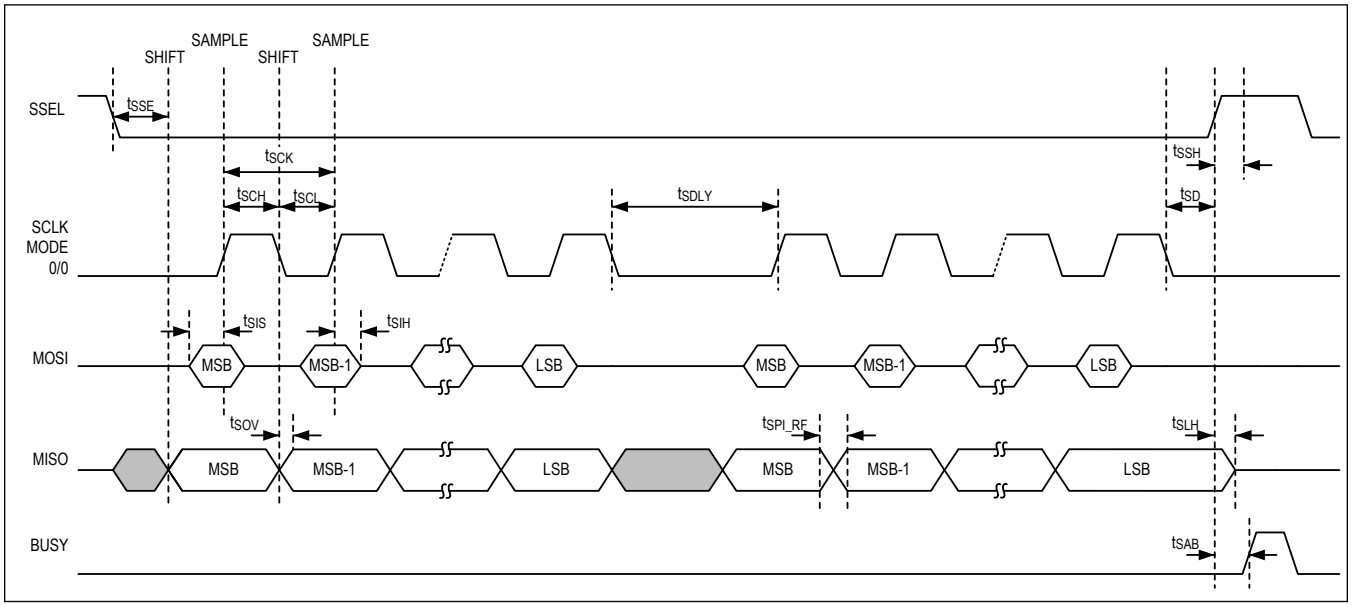


Figure 3. SPI Timing Specification

Applications Information

AFE Oscillator

The frequency range allowed by the regulations is 13.56MHz ±7kHz. The correct load capacitance has to be chosen according to the manufacturer's guideline. A temperature coefficent of type C0G capacitors should be used. It is not recommended to connect any components except quartz crystal and load capacitors to the oscillator's pins since any interference or noise injected into the oscillator corrupts the system performance. When an external clock source is used, the phase noise of the clock has to be kept low since it also corrupts the system performances.

Antenna Driver

The correct load impedance for a single output driver (100mW) is 7Ω resistive. The correct load impedance for a double parallel output driver (option bit 5, 200mW) is 3.5Ω resistive. The load impedance for a push-pull driver (option bits 5 and 6) must be at least 14Ω resistive. In this configuration, the consideration of chip power dissipation and junction temperature is necessary. It is also possible to use this configuration for low power systems with a direct antenna connection if a load impedance higher than 14Ω is used. Since the ASK modulation index is dependent on the load, it differs from those listed in Table 1.

Table 1. Configuration Word (Option Bits)

NAME	BIT [x:y]	DESCRIPTION
PUF	[0]	Power Up Flag 0 = Power down 1 = Power up
ODC	[3:1]	Output Driver Configuration
	[3:1]	Modulation Index 0 = 10% ASK, typ 1 = OOK 2 = ASK decrease 3% 3 = ASK decrease 1.5% 4 = ASK increase 3% 5 = ASK increase 6% 6 = ASK increase 12% 7 = ASK increase 20%
SCP	[4]	Short-Circuit Protection 0 = Short-circuit protection disabled 1 = Short-circuit protection enabled
SDRFDS	[5]	Single or Dual RF Driver Selection 0 = ANT1 only 1 = ANT1 and ANT2
DDPPO	[6]	Dual Driver in Phase or Phase Opposite 0 = In-phase driving 1 = Differential driving
RCC	[12:7]	Receiving Chain Configuration
	[8:7]	Filter Zero Selection 0 = High int. zero (~300kHz) 1 = Medium int. zero (~200kHz) 2 = Low int. zero (100kHz)
	[9]	Filter Lowpass Selection 400kHz 0 = High cutoff frequency (~1MHz) 1 = Low cutoff frequency (~400kHz)
	[12:10]	Receive Gain Selection 000b = Nominal gain 001b = Gain decreased for 5.7dB 010b = Gain decreased for 11.4dB 100b = Gain decreased for 22.8dB

Table 1. Configuration Word (Option Bits) (continued)

NAME	BIT [x:y]	DESCRIPTION
AGC	[20:13]	AGC System
	[13]	AM/PM Input Channel Selection 0 = RFIN1 input selected 1 = RFIN2 input selected
	[14]	AGC On/Off Selection 0 = AGC off 1 = AGC on
	[15]	AGC Attack Mode Selection 0 = Attack always 1 = First pulse not attacked
	[16]	AGC Decay Mode Selection 0 = Fast decay 1 = Slow decay
	[18:17]	AGC Attack Rate 00b = ~19dB/µs (average) 01b = ~9.5dB/µs (average) 10b = ~4.7dB/µs (average)
	[20:19]	AGC Decay Wait 00b = ~44µs 01b = ~88µs 10b = ~176µs
BPSKD	[22:21]	BPSK Decoder
	[21]	Output Selection Direct Subcarrier or BPSK 848kHz 0 = Subcarrier 1 = Enabled
	[22]	BPSK Automatic Frequency Adjust 0 = Disabled 1 = Enabled
OSA	[24:23]	Output Selection Analog
	[23]	Analog Disable or Enable 0 = Disabled 1 = Enabled
	[24]	Hold Delay After Modulation 0 = ~5µs 1 = ~15µs
OSC	[26:25]	Oscillator
	[25]	Oscillator Gain Selection 0 = Low g_M 1 = High g_M. The oscillator startup time can be decreased with the additional gain.
	[26]	External Oscillator Selection 0 = Internal quartz oscillator. OSCIN/OSCOUT require an external quartz crystal. 1 = External oscillator on. OSCIN input can be driven by an external clock source.
Reserved	[31:27]	Must be set to 0.
Note: It is recommended to set option bits 15 up to bit 20 and option bits 22, 24 to 0. Bit 25 should be set to 1.		

Receiver

Systems using a 212kHz sub-carrier modulation should use the medium filter selection, and systems using a 424kHz or 848kHz subcarrier should use the high frequency-filter selection. When a 424kHz or 848kHz system with on/off sub-carrier coding is used, the higher frequency zero enables very fast response of the receiver to the pulse burst with high DC level shift. When a BPSK system is used, lower frequency zero decreases phase distortion of the BPSK signal. System option bits control the receiver gain. Different receiver bandwidths result in different noise levels, therefore enabling different gain and sensitivity levels. The combination of filter selection and gain selection allows the system designer to choose the best combination for the RFID reader.

Configuration Word (Option Bits) Selection Depending on Transponder IC

The MAX66301 is compliant with almost all 13.56MHz transponder ICs by setting the AFE by the use of Table 1. The large combinations offered by the MAX66301 option bits permit adapting the reader IC to the transponder communication protocol. Table 2 gives the ISO typical suggested option bit configuration depending on the transponder IC used.

Table 2. Option Bit Configuration for ISO 15693 and 14443 Type A Standards

OPTION BIT	SUGGESTED VALUE	CONFIGURATION
0	1	Power up
1, 2, 3	1, 0, 0	OOK modulation
4	1	Short circuit enabled
5, 6	1, 1	Two drivers in differential
7, 8	0, 0	300kHz
9	0	1MHz
10, 11, 12	1, 0, 0	Gain decreased for 5.7dB
13	0	RFIN1 selected
14	1	AGC activated
15 to 20	0, 0, 0, 0, 0, 0	Standard configuration
21	0	Subcarrier mode
22	0	BPSK not used
23	0	Analog output disable
24	0	Hold delay set to 5µs
25	1	High g_M
26	0	Internal quartz
27 to 31	0, 0, 0, 0, 0	Normal IC mode

Transponder subcarrier: 424kHz or 484kHz (15693) and 848kHz (14443A)

Modulation index: 100%

Reception bandwidth: 300kHz to 1MHz

AGC: Nominal gain

Configuration word value: (MSB) 02h 00h 44h 73h (LSB)

Antenna Configurations and Decoupling

The theoretical antenna configurations and typical decoupling are shown in Figure 4, Figure 5, and Figure 6. The LC tank values needed for tuning of the antenna are subject to a larger dialogue; for details, refer to *Application Note 5921: Designing an Antenna for the MAX66300*.

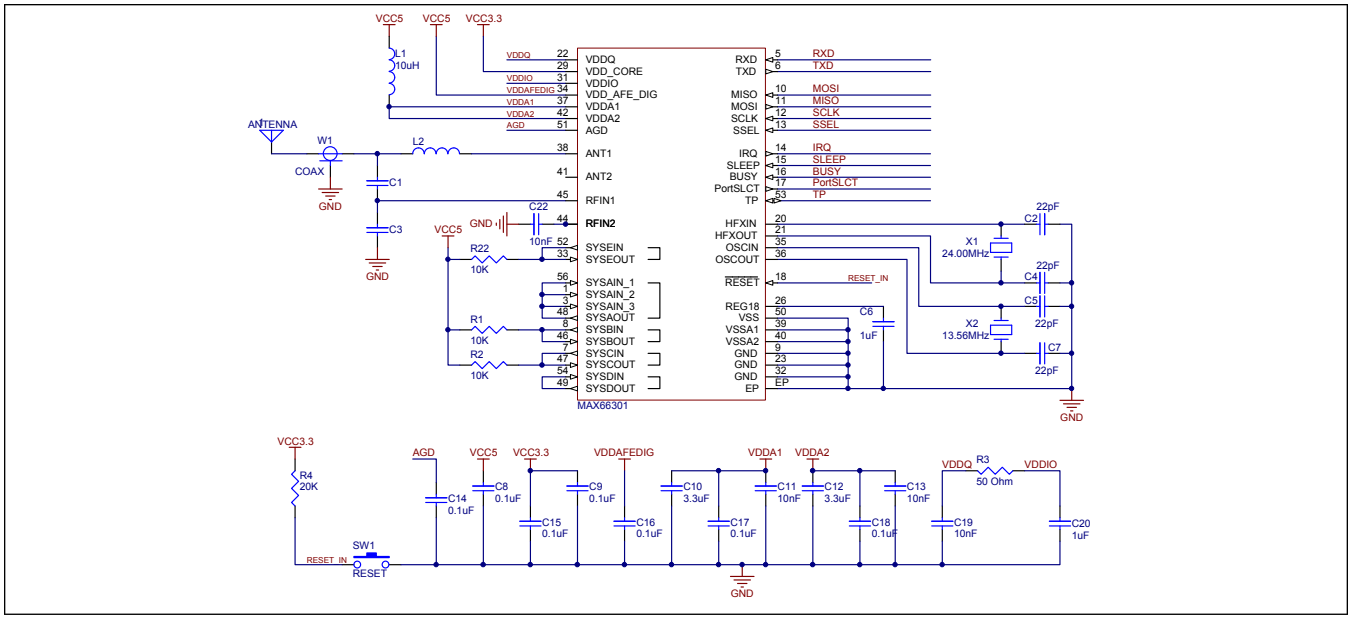


Figure 4. Single Output Driver (100mW)

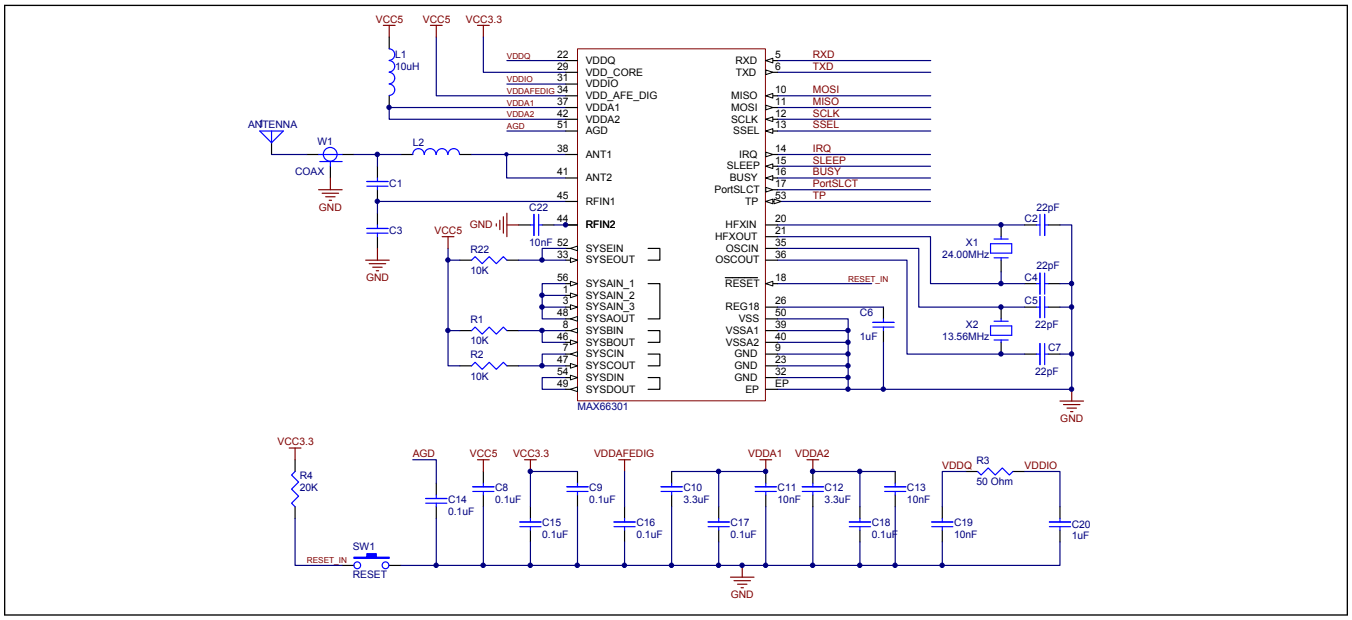


Figure 5. Double Parallel Output Driver (Options Bit 5, 200mW)

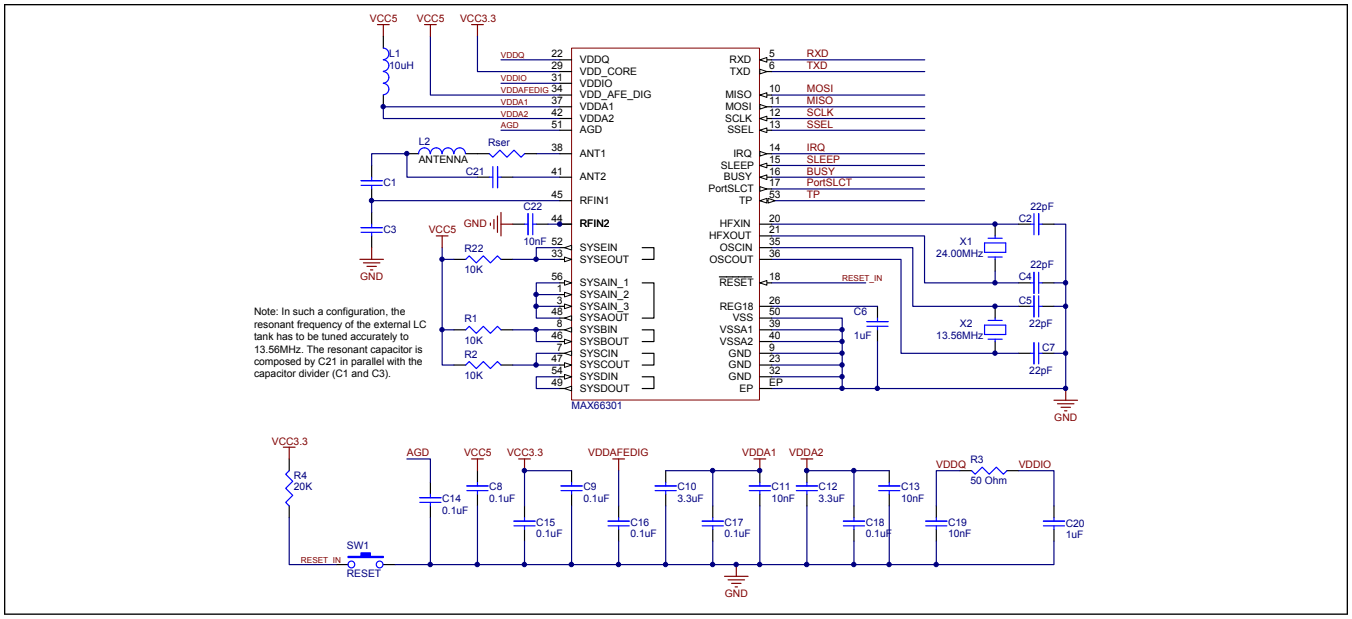


Figure 6. Configuration for Lower Power Systems with Direct Antenna Connections

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX66301ETN+	-40°C to +85°C	56 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/22	Initial release	—