*Click **here** for production status of specific part numbers.*

MAX38889

2.5V to 5.5V, 3A Reversible Buck/Boost Regulator for Backup Applications

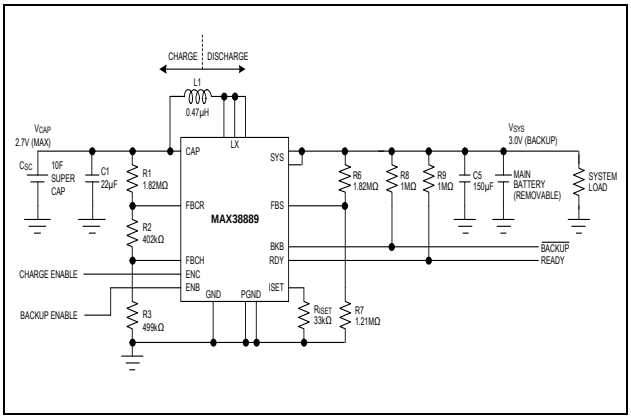
Product Highlights

- 2.5V to 5.5V System Output Voltage Range
- 0.5V to 5.5V Supercapacitor Voltage Range
- ±1% Threshold Accuracy
- 2.5% Hysteresis between Backup and Charging
- 1A to 3A Peak Inductor Current Limit
  - Peak Inductor Current Is Pin-Programmable over 1A to 3A through External Resistor
- 94% Peak Efficiency, Charging or Discharging Mode
- 4µA Quiescent Current in Ready State
  - After Supercapacitor Is Charged, Draws only 4µA of Quiescent Current
- Ready and Backup State Outputs
  - RDY and BKB Flags Provide Real-Time Status to System
- 3mm x 3mm, 16-Pin TQFN Package

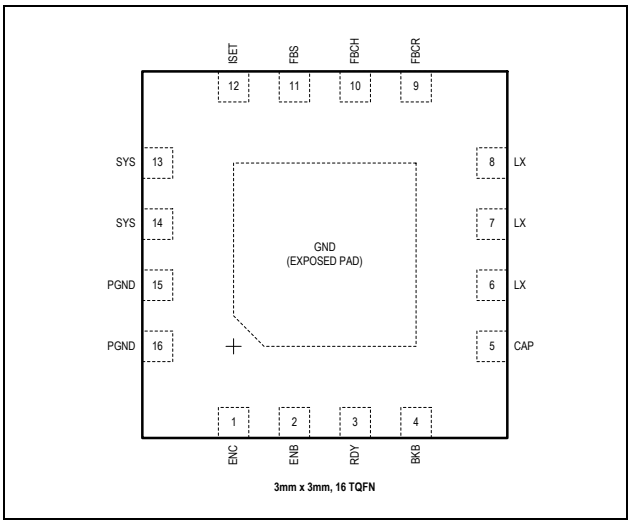
Key Applications

- Handheld Industrial Equipment
- Portable Devices/Computers with Removable Battery
- Industrial Sensor and Actuators
- Aftermarket Automotive Tracking

Simplified Application Diagram



Pin Configuration



***Ordering Information** appears at end of data sheet.*

19-101019; Rev 1; 5/21

maxim integrated™

Absolute Maximum Ratings

CAP, ENB, ENC to GND ..... -0.3V to +6V

SYS, BKB, RDY to GND ..... -0.3V to +6V

FBCH, FBCR to GND ..... -0.3V to CAP + 0.3V

FBS, ISET to GND ..... -0.3V to SYS + 0.3V

PGND to GND ..... -0.3V to +0.3V

Continuous Power Dissipation (T_A = +70°C, TQFN, derate 23.1mW/°C above +70°C) 1847.6mW

Operating Temperature Range ..... -40°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Maximum Junction Temperature ..... +150°C

Lead Temperature (soldering, 10 seconds) ..... +300°C

Soldering Temperature (reflow) ..... +260°C

LX RMS Current ..... $\pm 5.0A_{RMS}$

Output Short-Circuit Duration ..... Continuous

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T1633+5C
Outline Number	*21-0136*
Land Pattern Number	*90-0032*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	43.3°C/W
Junction to Case (θ_{JC})	4°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SYS} = 3.7V, V_{CAP} = 2.8V, T_J = -40°C to +125°C (typical values at T_J = +25°C), circuit of *Figure 1*, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYS Voltage Range	V_{SYS}	Guaranteed by LX peak backup current and SYS shutdown current		2.5		5.5	V
CAP Voltage Range	V_{CAP}	Guaranteed by maximum on-time and CAP shutdown current		0.5		5.5	V
SYS Shutdown Current	I_{SYS_SD}	V_{SYS} = 5.5V, V_{ENC} = V_{ENB} = 0V	T_A = +25°C		0.010	1	µA
			T_A = +125°C		0.46		
SYS Ready Supply Current	I_{SYS_RDY}	V_{FBS} = 1.3V, V_{FBCH} = 0.515V, V_{FBCR} = 0.6V	T_A = +25°C		4.5	8	µA
			T_A = +125°C		8		
SYS Backup Supply Current	I_{SYS_BU}	V_{FBS} = 1.212V, V_{FBCH} = 0.5V, V_{FBCR} = 0.6V			75	150	µA
CAP Shutdown Current	I_{CAP_SD}	V_{CAP} = 5.5V, V_{ENC} = V_{ENB} = 0V	T_A = +25°C		0.01	1	µA
			T_A = +125°C		0.2		
System Undervoltage Threshold	V_{UVLOF}	V_{SYS} falling, 100mV typical hysteresis, V_{CAP} = 0V		2.1	2.2	2.3	V
FBS Backup Voltage	V_{FBS_BU}	V_{FBS} rising, when discharging stops		1.188	1.2	1.212	V
FBS Charging Threshold	V_{FBS_CHG}	From V_{FBS} backup voltage, when charging begins		2	2.5	3	%
FBCH Threshold	V_{TH_FBCH}	V_{FBCH} rising, when charging stops; 10mV typical hysteresis		0.495	0.5	0.505	V
FBCR Threshold	V_{TH_FBCR}	V_{FBCR} rising, when RDY releases; 10mV typical hysteresis		0.495	0.5	0.505	V
ENC Input Threshold	V_{IL}	V_{FBS} = 1.3V, V_{FBCH} = 0.4V, when LX switching	V_{ENC} rising	600	850		mV
	V_{IH}	V_{FBS} = 1.3V, V_{FBCH} = 0.4V, when LX switching	V_{ENC} falling		950	1200	
ENB Input Threshold	V_{IL}	V_{FBS} = 1.1V, V_{FBCH} = 0.4V, when LX switching	V_{ENB} rising	600	850		mV
	V_{IH}	V_{FBS} = 1.1V, V_{FBCH} = 0.4V, when LX switching	V_{ENB} falling		950	1200	
ISET Resistor Range	R_{ISET}	Guaranteed by LX peak current limits		33		100	kΩ
LX Switching Frequency	F_{SW}	V_{CAP} = 1.5V, I_{SYS} = 1A			1.2		MHz

(V_{SYS} = 3.7V, V_{CAP} = 2.8V, T_J = -40°C to +125°C (typical values at T_J = +25°C), circuit of *Figure 1*, unless otherwise specified.)

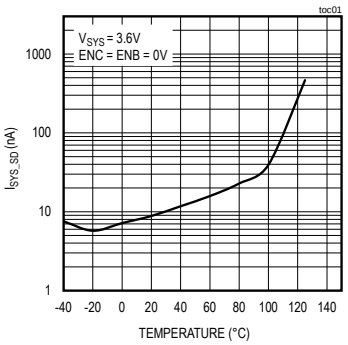
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Peak Backup Current Limit	I_{LX_BU}	Circuit of Figure 1, V_{CAP} = 2V, V_{SYS} = 2.5V (Note 1)	R_{ISET} = 33kΩ	2.25	3	3.75	A
	I_{LX_BU}	Circuit of Figure 1, V_{CAP} = 2V, V_{SYS} = 2.5V (Note 1)	R_{ISET} = 100kΩ		1		
LX Peak Charge Current Limit (Note 1)	I_{LX_CHG}	Circuit of Figure 1, V_{SYS} = 3.7V, V_{CAP} = 2V	R_{ISET} = 33kΩ	2.25	3	3.75	A
			R_{ISET} = 100kΩ		1		
Feedback Input Bias Current	I_{FBS}, I_{FBCH}, I_{FBCR}	V_{FBS} = 1.2V, V_{FBCH} = V_{FBCR} = 0.5V	T_A = +25°C	-0.1	0.01	+0.1	µA
			T_A = +125°C		0.01		
Enable Input Leakage Current	I_{ENC}, I_{ENB}	0V < V_{ENC}, V_{ENB} < 5.5V	T_A = +25°C	-1	0.004	1	µA
			T_A = +125°C		0.01		
LX Low-Side FET Resistance	R_{LOW}	V_{LX} switched to 0V			42	84	mΩ
LX High-Side FET Resistance	R_{HIGH}	V_{LX} switched to V_{SYS}			57	114	mΩ
LX Leakage Current	I_{LX_LKG}	V_{ENC} = V_{ENB} = 0V, V_{SYS} = 5.5V, V_{LX} = 0 to 5.5V	T_A = +25°C	-1	0.01	1	µA
			T_A = +125°C		0.26		
Maximum On-Time	t_{ON}	Typical Application Circuit, V_{SYS} = 2.9V	V_{CAP} = 2V	320	400	480	ns
			V_{CAP} = 1.2V		570		
Minimum Off-Time	t_{OFF}	Backup mode, V_{FBS} = 1.164V		80	100	120	ns
Maximum Duty Cycle	$Duty_{MAX}$	V_{CAP} = 0.5V		90	95		%
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising, 15°C typical hysteresis			165		°C
Logic Output Leakage High	I_{BKB_H}	V_{BKB} = 5.5V, V_{RDY} = 5.5V	T_A = +25°C	-1	0.001	+1	µA
	I_{RDY_H}	V_{BKB} = 5.5V, V_{RDY} = 5.5V	T_A = +125°C		0.01		
Logic Output Voltage Low	V_{BKB_L} V_{RDY_L}	I_{BKB} = 10mA, I_{RDY} = 10mA			0.1	0.4	V
High-Side FET Zero-Crossing	I_{ZXP}	Circuit of Figure 1, V_{SYS} = 2.9V, V_{CAP} = 2V (Note 1)			60		mA
Low-Side FET Zero-Crossing	I_{ZXN}	Circuit of Figure 1, V_{SYS} = 3.7V, V_{CAP} = 2V (Note 1)			180		mA

Note 1: DC measurement, actual inductor current accuracy in the circuit is affected by the propagation delay time.

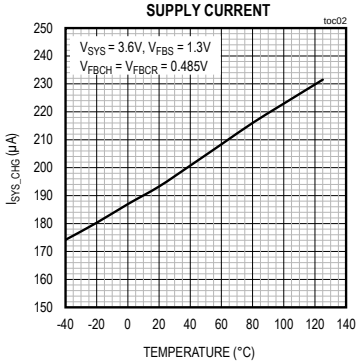
Typical Operating Characteristics

(V_{SYS} = 3.6V, V_{CAP} = 2.7V, C_{SYS} = 150µF, C_{CAP} = 22µF + 10F, L = 0.47µH, unless otherwise noted.)

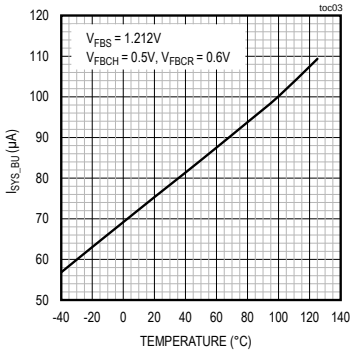
SYS PIN SHUTDOWN CURRENT



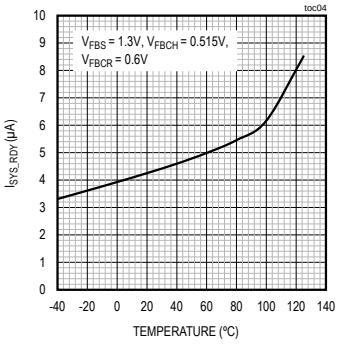
SYS PIN CHARGING SUPPLY CURRENT



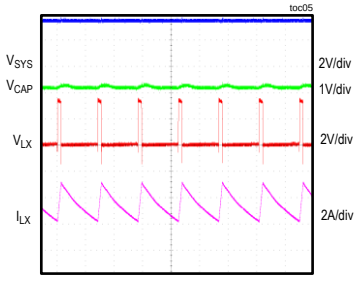
SYS BACKUP SUPPLY CURRENT



SYS READY SUPPLY CURRENT



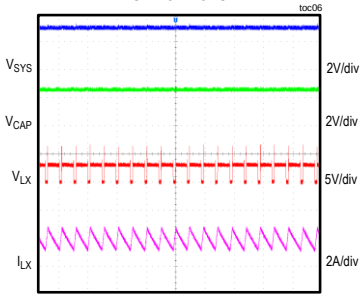
SWITCHING WAVEFORM WHILE CHARGING



VSYS = 3.6V, VCAP = 0V

4µs/div

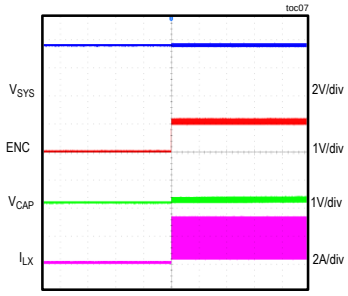
SWITCHING WAVEFORM DURING BACKUP



VSYS = 3V, VCAP = 2.7V, ISYS = 1A

4µs/div

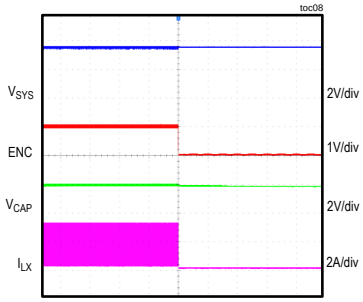
POWER-UP



VSYS = 3.6V

8ms/div

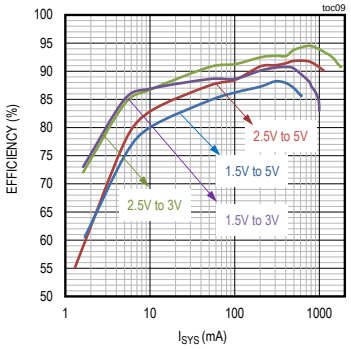
POWER-DOWN DURING CHARGING



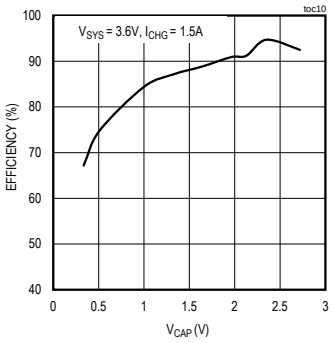
VSYS = 3.6V, VCAP = 2V

40ms/div

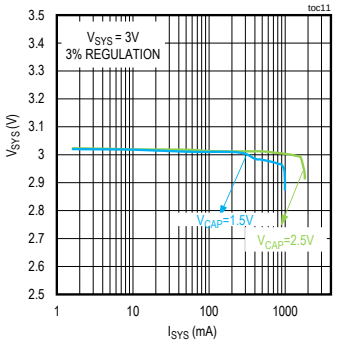
EFFICIENCY DURING BOOST MODE



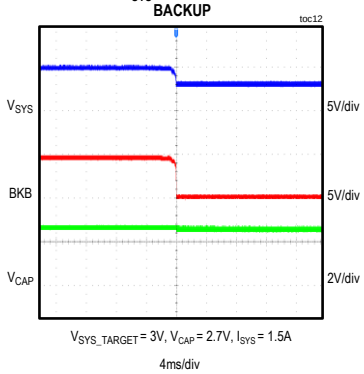
EFFICIENCY DURING BUCK MODE



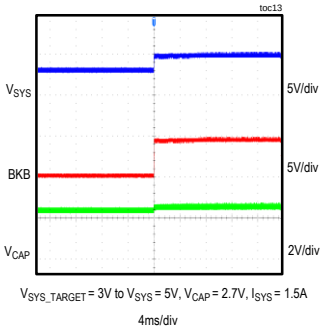
LOAD REGULATION



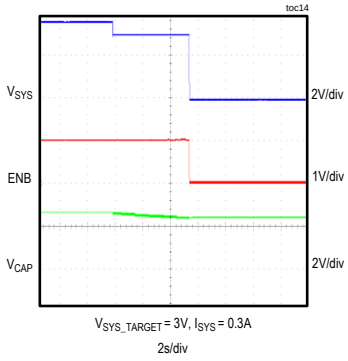
V_{SYS} TRANSITION BACKUP



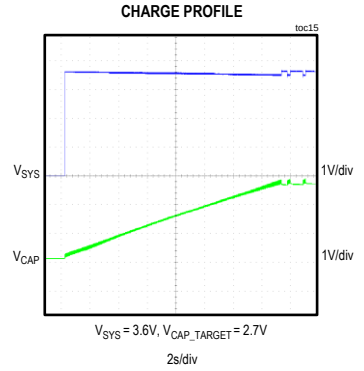
V_{SYS} TRANSITION FROM BACKUP TO CHARGING



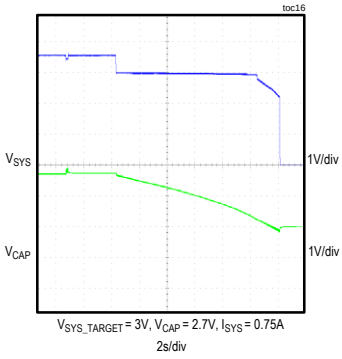
DISABLE BACKUP BY ENB



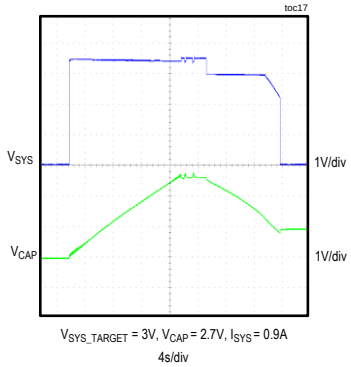
CHARGE PROFILE



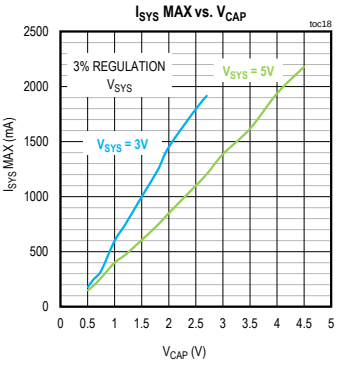
DISCHARGE PROFILE



CHARGE-DISCHARGE PROFILE

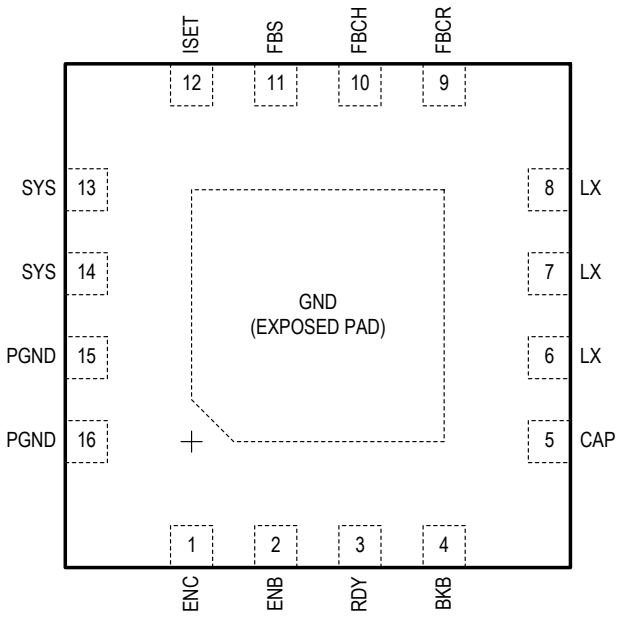


I_{SYS} MAX vs. V_{CAP}



Pin Configuration

16 TQFN



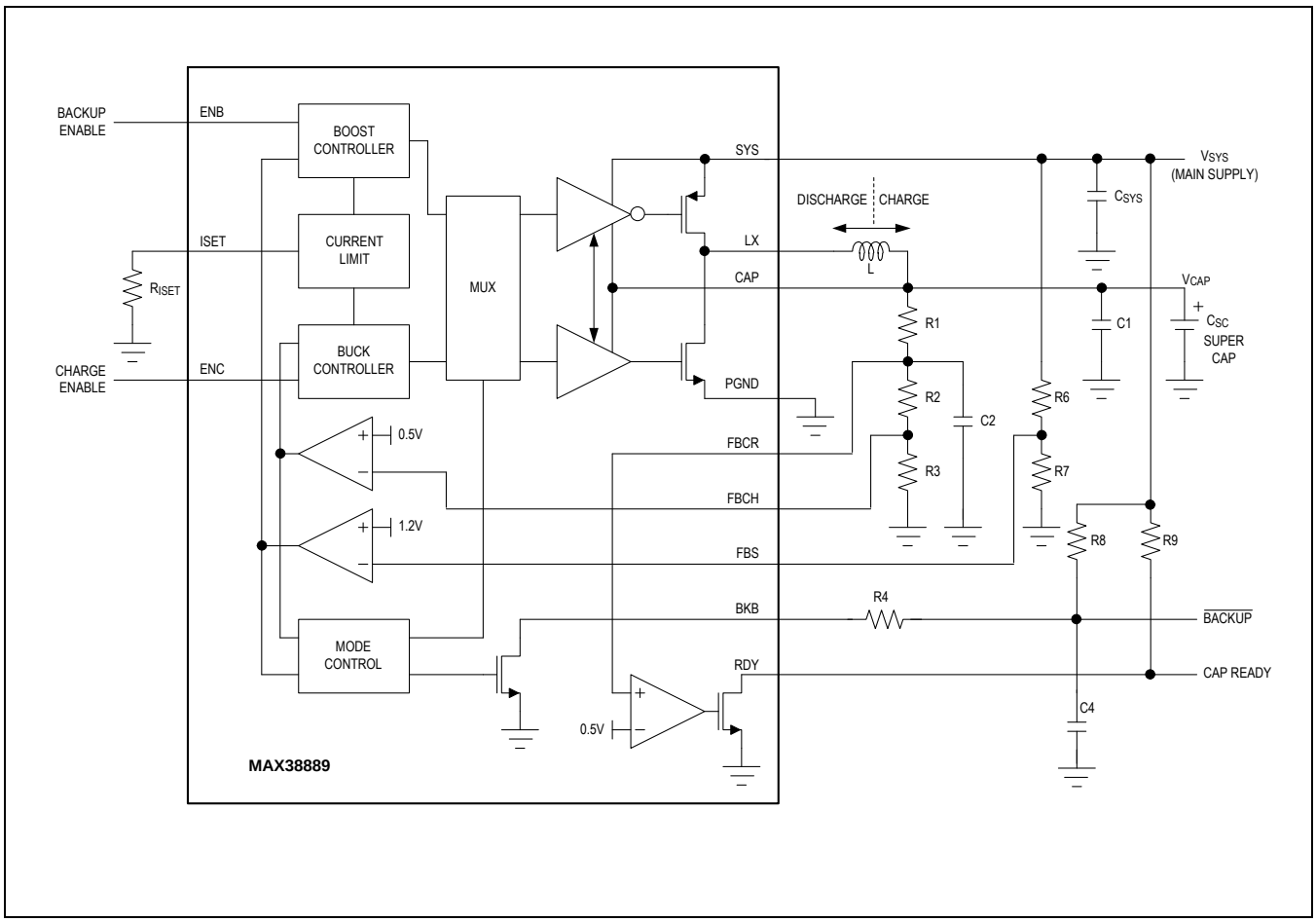
3mm x 3mm, 16 TQFN

Pin Descriptions

PIN	NAME	FUNCTION
1	ENC	Charger Enable Input. Drive this pin high to enable charging of the supercapacitor while V_{SYS} is above the charging threshold. Drive this pin low to disable charging. If not driven, tie this pin to the SYS rail.
2	ENB	Backup Enable Input. Drive this pin high to enable system backup when V_{SYS} drops below the backup threshold. Drive this pin low to disable backup. If not driven, tie this pin to the SYS rail.
3	RDY	Ready Status Pin. Connect a pullup resistor from RDY to a logic supply. V_{RDY} will be pulled low when V_{FBCR} is below 0.5V and released when it is above 0.5V. V_{RDY} is pulled low when V_{ENC} and V_{ENB} are both low.
4	BKB	Backup Status Pin. Connect a pullup resistor from BKB to a logic supply. V_{BKB} will be pulled low when V_{FBS} is regulating at 1.2V and released when it is above 1.23V. V_{BKB} is released high when V_{ENC} and V_{ENB} are both low.
5	CAP	Supercapacitor. Connect to a supercapacitor rated between 0.8V to 5V. Put a high-frequency capacitor of 22µF close to the CAP pin.
6, 7, 8	LX	Inductor Switching Node. Connect a 0.47µH inductor from LX to CAP. Keep this switching node separated from feedback signal nodes FBS, FBCH, and FBCR as much as possible.
9	FBCR	Supercapacitor Ready Input. RDY will go high when V_{FBCR} reaches 0.5V.
10	FBCH	Supercapacitor Feedback Input. Connect a resistor-divider from CAP to FBCH to GND to set the supercapacitor maximum charging voltage.

11	FBS	System Feedback Input. Connect a resistor-divider from SYS to FBS to GND to set the system backup operating voltage. When V_{FBS} is >102.5% of V_{FBS_BU}, the supercapacitor will be charged from SYS.
12	ISET	Charge/Discharge Current Select. During charging, the average supercapacitor current (I_{CAP_CHG}) is set to I_{CAP_CHG} = 1.5A x (33kΩ/R_{ISET}). During backup, V_{SYS} is regulated through the boost regulator with a peak inductor current of I_{LX_BU} = 3A x (33kΩ/R_{ISET}).
13, 14	SYS	System Supply. Connect to the system supply and bypass with 2x47µF and 2x22µF ceramic capacitors to PGND. In addition, place a high-frequency filter capacitor of 1µF close to the part across the SYS and PGND pins.
15, 16	PGND	Power Ground.
EP	GND	Analog Ground. Connect the exposed pad to the ground plane with excellent thermal conduction to ambient temperature to avoid overtemperature.

Functional Diagram



Detailed Description

The MAX38889 is a flexible storage capacitor or capacitor bank backup regulator transferring power efficiently between a storage element and a system supply rail.

When the main supply is present and its voltage is above the minimum threshold system supply voltage, the regulator operates in charging mode and charges the storage element with a maximum 3A peak, 1.5A average inductor current. Once the storage element is charged, the circuit draws only 4µA of current while maintaining the storage element in its ready state. The supercapacitor needs to be fully charged to enable backup operation.

When the main supply is removed, the regulator prevents the system from dropping below the set system backup operating voltage, boosting the supercapacitor voltage to a regulated V_{SYS} by discharging the storage element with a maximum 3A peak inductor current. During this backup mode of operation, the MAX38889 utilizes an adaptive on-time, current-limited, pulse-frequency-modulation (PFM) control scheme. Once the MAX38889 is in backup mode, the BKB flag is low.

The external pins allow various settings such as maximum supercapacitor voltage, system backup voltage (V_{SYS}), and peak inductor charge and discharge current.

The MAX38889 implements a True Shutdown™ feature, disconnecting SYS from CAP as well as protecting against a SYS short if $V_{CAP} > V_{SYS}$.

Charging and backup can be disabled by keeping the ENC and ENB pins low, respectively. The backup system status can be monitored through two status outputs: the RDY flag that indicates when the supercapacitor is charged and the BKB flag that indicates when backup operation is occurring.

Application Circuits

The typical application of the MAX38889 is shown in Figure 1.

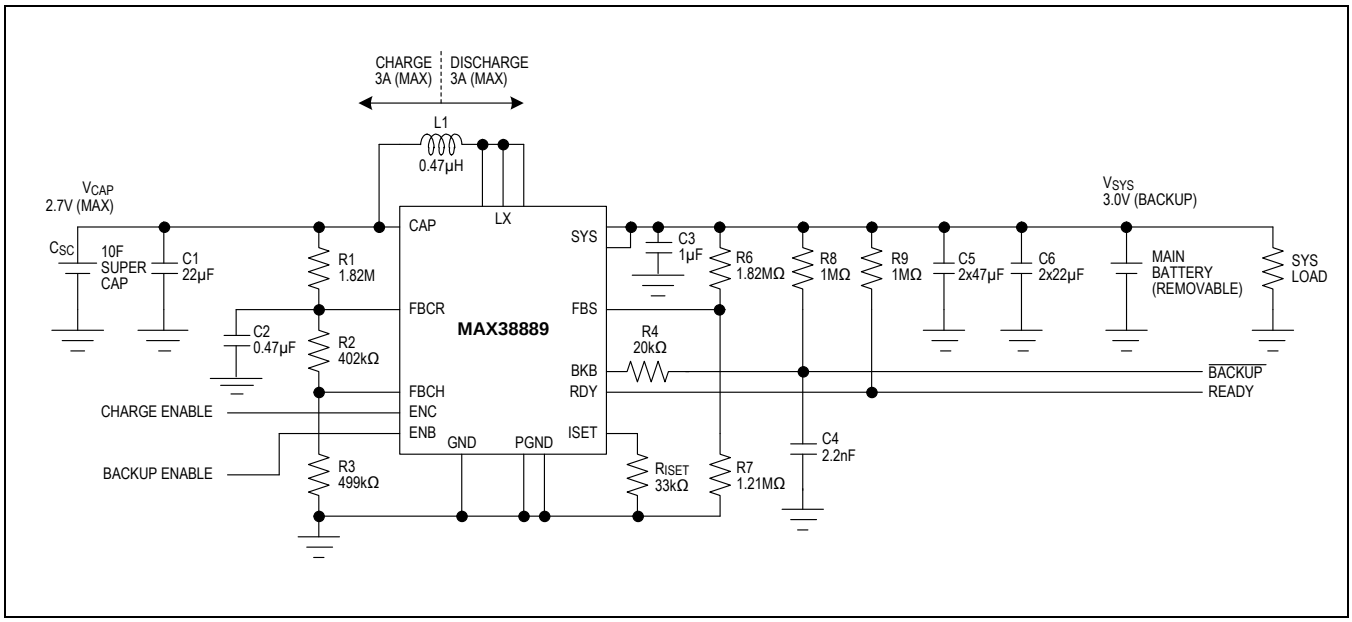


Figure 1. Application Circuit

Supercapacitor Voltage Configuration

The maximum supercapacitor voltage (V_{CAP_MAX}) during charging is determined by the resistor-divider driving the FBCH pin. When V_{FBCH} reaches 0.5V, further charging of the supercapacitor is halted. The threshold has a 2.5% (12.5mV) hysteresis. To keep the ready power drawn low, keep the quiescent current in the resistor-divider low by setting the resistor from FBCH to GND to 500kΩ. The resistance from CAP to FBCH (R1 + R2) can then be determined by the standard equation:

$$R1 + R2 = R3 \times \left(\frac{V_{CAP\_MAX}}{0.5V} - 1 \right)$$

Selecting V_{CAP_MAX} = 2.7V and R3 = 499kΩ:

R1 + R2 ≈ 2.2MΩ

The RDY pin is a flag that goes high when the supercapacitor has crossed a user-defined voltage. Like the FBCH input, the FBCR pin is driven from CAP through a resistor-divider. To save quiescent current, the FBCR and FBCH resistor-dividers can be combined using a three-resistor-divider string, as shown in Figure 1.

Total resistance from CAP to GND (R_T) is:

R_T = R1 + R2 = R3 = 2.2MΩ + 499kΩ ≈ 2.7MΩ

RDY will go high when V_{FBCR} is greater than 0.5V.

Assuming we want RDY to go high when V_{CAP} reaches 1.5V:

V_{CAP_RDY} = 1.5V

R3 = 499kΩ

$$R2 = R_T \times \left(\frac{0.5V}{V_{CAP\_RDY}} \right) - R3 = 2.7M\Omega \times \left(\frac{0.5V}{1.5V} \right) - 499k\Omega = 401k\Omega$$

Selecting R2 = 402kΩ:

$R1 = R_T - R2 - R3 = 2.7M\Omega - 402k\Omega - 499k\Omega = 1.8M\Omega$

Select R2 = 1.82MΩ for fine-tuning on the bench.

During backup, the supercapacitor voltage discharges and the boost converter automatically adjusts its duty cycle to regulate V_{SYS}. When V_{SYS} drops below UVLO threshold (V_{UVLOF}) or V_{FBCH} drops to 10% of the FBCH threshold voltage (V_{TH_FBCH}), the boost regulator stops delivering load current and the supercapacitor voltage is preserved with only the current from the resistor-divider discharging the supercapacitor further.

System Voltage Configuration

The backup system voltage is determined by a resistor-divider driving the FBS pin. Set the system backup voltage using a resistor-divider from SYS to FBS to GND. When V_{FBS} is above 1.23V, the DC-DC regulator draws power from the main battery through the SYS pin to charge the supercapacitor to the maximum voltage set by FBCH and be ready for backup. The peak charging current can be programmed to up to 3A, max. When the main battery is removed and V_{FBS} drops to 1.2V, the DC-DC regulator draws power from the supercapacitor and regulates the SYS pin to the programmed backup voltage with the programmed peak inductor current, which is a maximum of 3A.
In order to reduce the current flowing through the resistor-divider, select high-value resistors.
To set system the backup voltage to 3.0V, select the bottom resistor (R7) to 1.21MΩ. The top resistor value can be calculated by the following equation:

$$R6 = \left(3.0 \times \frac{R7}{1.2} \right) - R7$$

$$R6 = \left(3.0 \times \frac{1.21M\Omega}{1.2} \right) - 1.21M\Omega = 1.815M\Omega$$

Select R6 = 1.82MΩ for fine-tuning on the bench.

Charge/Discharge Current Configuration

The MAX38889 current configuration pin, ISET, gives the user the ability to optimize the efficiency around the maximum load requirements of the system during backup. A larger current setting allows the supercapacitor to be discharged to a lower voltage for a given load during backup.

A single resistor sets both the charging and backup current.

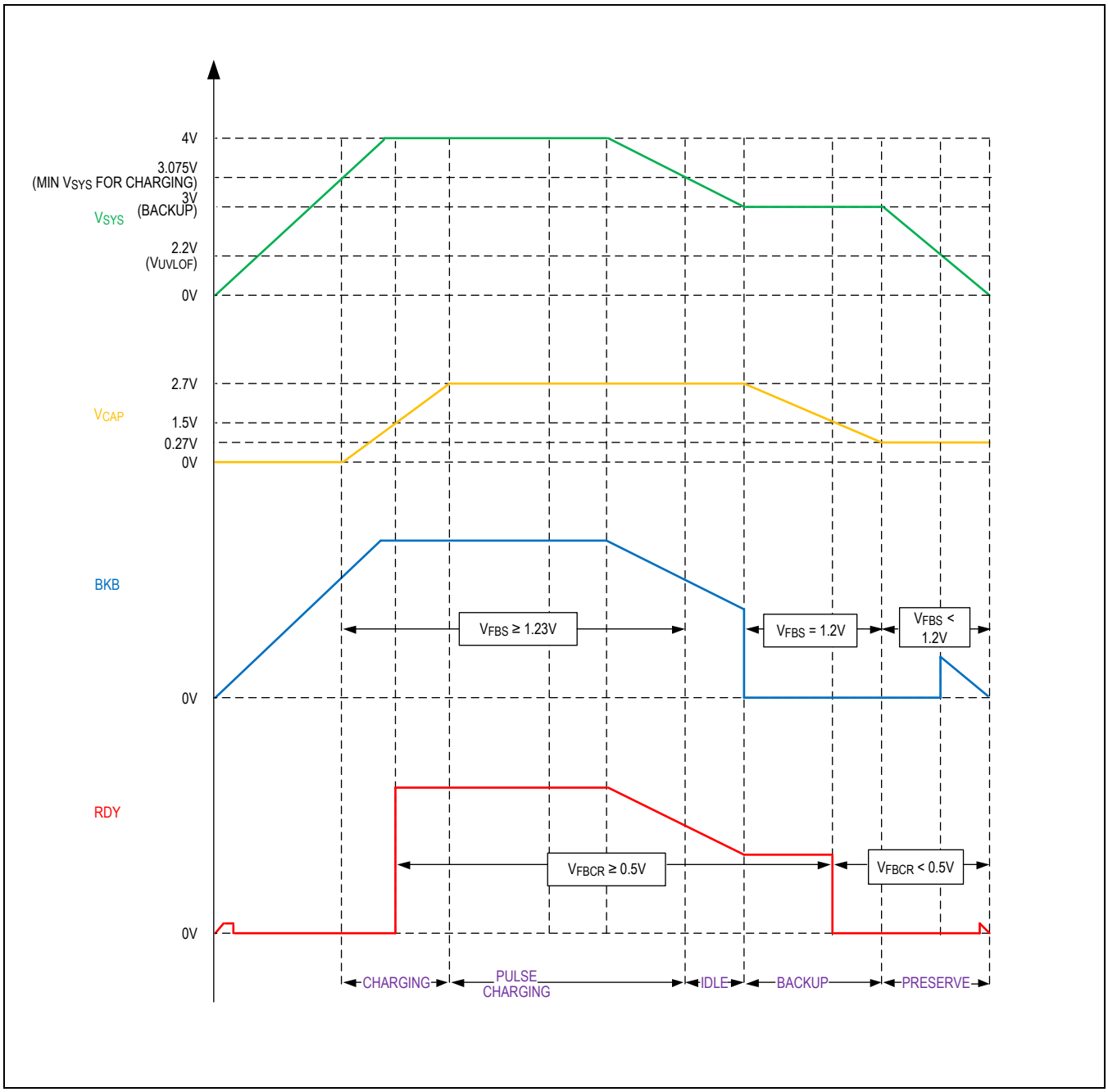


Figure 2. System Waveforms

Charging

Supercapacitor charging current and discharging current is determined by the same resistor, RISET. The buck regulator operates in forced discontinuous conduction mode (DCM) until the supercapacitor gets fully charged.

Average charging current (I_{CAP_CHG}) is determined by:

$$I_{CAP\_CHG} = 1.5A \times \left(\frac{33k\Omega}{R_{ISET}} \right)$$

where R_{ISET} can be selected from 100kΩ to 33kΩ, and I_{CAP_CHG} varies from 0.5A to 1.5A, respectively. Since charging current is efficiently drawn through a buck regulator, the average charging current from SYS (I_{SYS_CHG}) will be:

$$I_{SYS\_CHG} = 1.5A \times \left(\frac{33k\Omega}{R_{ISET}} \right) \times \left(\frac{V_{CAP}}{V_{SYS}} \right) \times \left(\frac{1}{\text{charging efficiency}} \right)$$

$$\text{Peak charging current} \left(I_{LX\_CHG} \right) = 3A \times \left(\frac{33k\Omega}{R_{ISET}} \right)$$

When the supercapacitor voltage reaches its maximum voltage as determined by the FBCH threshold, the forced DCM of the charging stops. After this, only pulse charging takes place.

Backup

During backup, the boost regulator regulates the system voltage to the set the backup voltage, thus limiting the peak inductor current (I_{LX_BU}) to:

$$I_{LX\_BU} = 3A \times \left(\frac{33k\Omega}{R_{ISET}} \right)$$

where R_{ISET} can be selected from 100kΩ to 33kΩ, and I_{LX_BU} varies from 1A to 3A, respectively.

For a given system load in backup (I_{SYS_BU}), the minimum supercapacitor voltage (V_{CAP_MIN}) needed to support the load can be calculated as:

$$V_{CAP\_MIN} = V_{SYS\_MIN} \times \left[\frac{I_{SYS\_BU}}{I_{LX\_BU} - \left(0.5 \times dI_{LX} \right)} \right] \times \left(\frac{1}{\text{backup efficiency}} \right)$$

Approximate a ripple current of 2A and 1A system load at 3.0V. Assuming an efficiency of 75%:

$$V_{CAP\_MIN} = 3V \times \left[\frac{1A}{3A - \left(0.5 \times 2 \right)} \right] \times \left(\frac{1}{75\%} \right) = 2V$$

Applications Information

Capacitor Selection

Capacitors at the SYS and CAP pins reduce current peaks and increase efficiency. Ceramic capacitors are recommended because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Choose an acceptable dielectric such as X5R where the ambient temperature is less than +85°C or X7R where the ambient temperature is less than +125°C. Due to the ceramic capacitor's capacitance derating at higher DC bias voltages, 2x47µF and 2x22µF ceramic capacitors are recommended at the SYS side and a 22µF ceramic capacitor at the CAP side for most applications. In addition, it is recommended to place a high-frequency filter capacitor of 1µF across the SYS and PGND pins as mentioned in the PCB Layout Guidelines.

Supercapacitor Selection

When the power source supplying the V_{SYS} voltage is removed, power to the output is provided by the MAX38889 operating in the backup or boost mode of operation using the supercapacitor as its source. In order to ensure that the supply voltage stays in regulation, the amount of power the supercapacitor can deliver at its minimal voltage should be greater than that required by the system. The MAX38889 presents a constant power load to the supercapacitor where smaller current is pulled out of the supercapacitor near its maximum V_{CAP} voltage. However, current drawn from the

supercapacitor increases as it discharges to maintain constant power at the load. The amount of energy required in backup mode is the product of the constant backup power and time defined as backup time, T_{BACKUP}.

The amount of energy available in the supercapacitor (C_{SC}) is calculated using the following formula:

$$E = \frac{1}{2} \times C_{SC} \times \left(V^2_{CAPMAX} - V^2_{CAPMIN} \right) \quad (J)$$

The amount of energy required to complete the backup equals to:

$$E = V_{SYS} \times I_{SYS} \times T_{BACKUP} \quad (J)$$

where I_{SYS} is the system load during backup.

Since the energy required at the system side during the backup event comes from the available energy in the supercapacitor, assuming conversion efficiency η and the given T_{BACKUP}, the required C_{SCAP} is determined by the following equation:

$$C_{SC} = \frac{2 \times V_{SYS} \times I_{SYS} \times T_{BACKUP}}{\left[\left(V^2_{CAPMAX} - V^2_{CAPMIN} \right) \times \eta \right]} \quad (F)$$

For example, in the Figure 1 application circuit, assuming a 200mA system load and an average efficiency of 93%, the minimum value of the supercapacitor required for a 10s backup time is:

$$C_{SC} = \frac{2 \times 3.0V \times 0.2A \times 10s}{\left[\left((2.7V)^2 - (1.5V)^2 \right) \times 0.93 \right]} = 2.56F$$

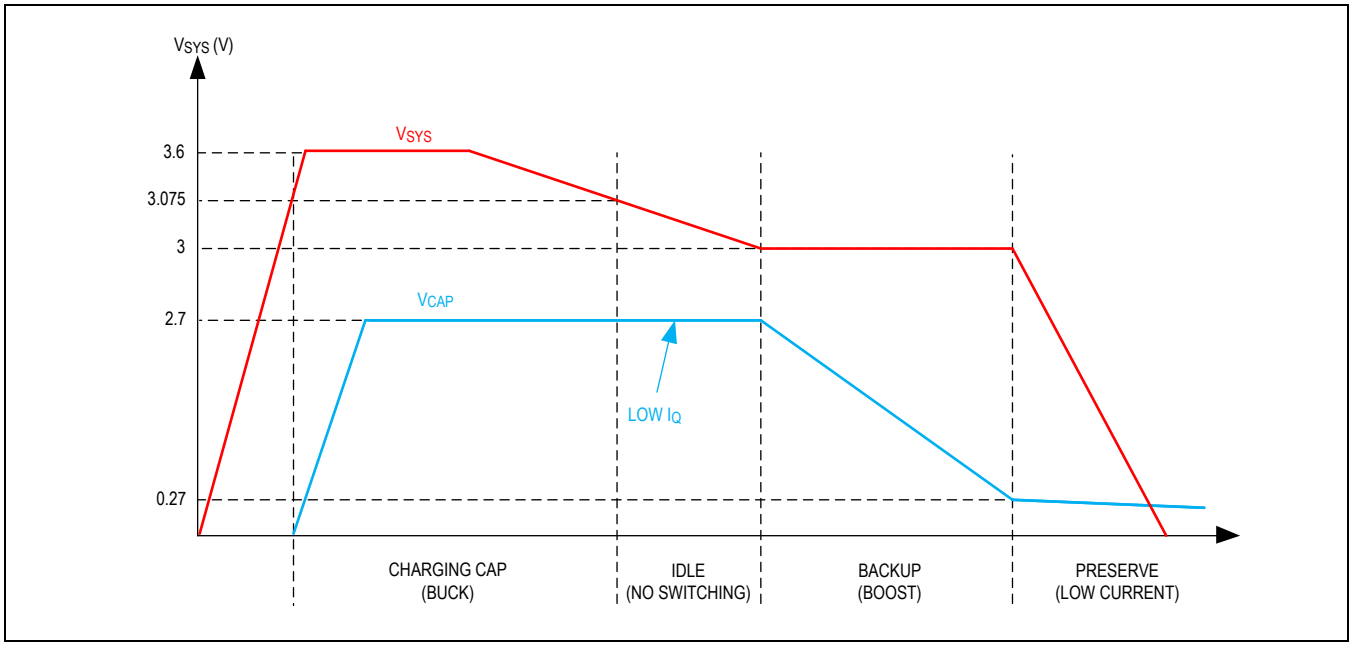


Figure 3. Charging/Discharging Waveforms

Inductor Selection

The recommended inductor value for the MAX38889 is 0.47µH.

Status Flags

The MAX38889 has two dedicated pins to report the device status to the host processor. Both of these output pins are open-drain type and require external pullup resistors. The recommended value for the pullup resistors is 1MΩ. The pins should be pulled up to the SYS rail.

BKB Flag

The BKB flag indicates that the converter is in backup mode, and it is low when the part is in backup mode and V_{FBS} is regulating at 1.2V. This pin is high when V_{FBS} is above 1.23V. BKB is high when V_{ENC} and V_{ENB} are both low.

RDY Flag

The RDY flag helps the external processor to detect that the supercapacitor is ready to back up the SYS voltage. The RDY flag is high when V_{FBCR} > 0.5V and low when V_{FBCR} < 0.5V. The RDY threshold can be set using external resistor divider from the supercapacitor to GND.

Enabling the Device

The MAX38889 has dedicated enable pins for both charging and backup modes. Both of the pins can either be driven individually by a digital signal, pulled up, or strapped to the SYS rail.

Charger Enable Input (ENC)

Drive this pin high to enable charging of the supercapacitor while V_{SYS} is above the charging threshold. Drive it low to disable charging and reduce quiescent current. The ENC voltage applied should be more than 950mV.

Backup Enable Input (ENB)

Drive this pin high to enable system backup when V_{SYS} drops below the backup threshold. Drive it low to disable backup and reduce quiescent current. The ENB voltage applied should be more than 950mV.

PCB Layout Guidelines

Minimize trace lengths to reduce parasitic capacitance, inductance and resistance, and radiated noise. Keep the main power path from SYS, LX, CAP, and PGND as tight and short as possible. Minimize the surface area used for LX, since this is the noisiest node. It is recommended to place a filter capacitor close to the part across the SYS and GND pins to minimize voltage spikes on account of trace inductance, as shown in Figure 4.

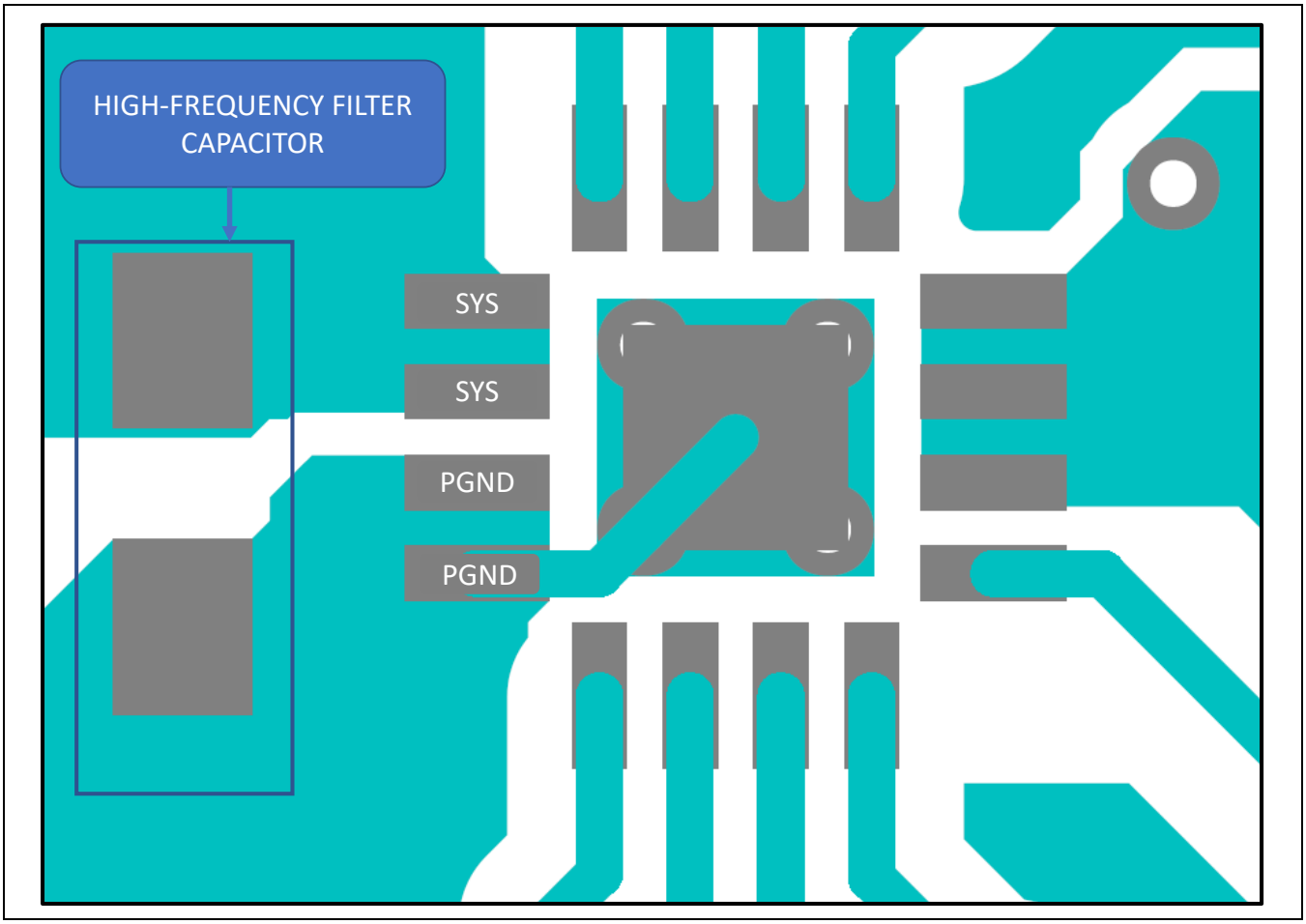


Figure 4. High-Frequency Filter Capacitor

The trace between the feedback resistor-dividers should be as short as possible and should be isolated from the noisy power path. Refer to the EV kit layout for best practices.

The PCB layout is important for robust thermal design. The junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connections. Using thick PCB copper and having a SYS, LX, CAP, and PGND copper pour will enhance the thermal performance. The TQFN package has a large, exposed pad under the package, which creates an excellent thermal path to the PCB. This pad is electrically connected to the analog GND of the controller (AGND). Its PCB pad should have multiple thermal vias connecting the pad to the internal ground plane. The thermal vias should either be capped or have a small diameter in order to minimize solder wicking and voids.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	FEATURES
MAX38889AATE+	-40°C to +125°C	3mm x 3mm, 16-pin TQFN	Enable input, selectable voltages and currents

+Denotes a lead (Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/21	Initial release	—
1	5/21	Updated Electrical Characteristics	4

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