*Click here to ask an associate for production status of specific part numbers.*

# 4.5V to 36V, 1A, High-Efficiency, Synchronous Step-Down DC-DC Converter

**MAX17645**

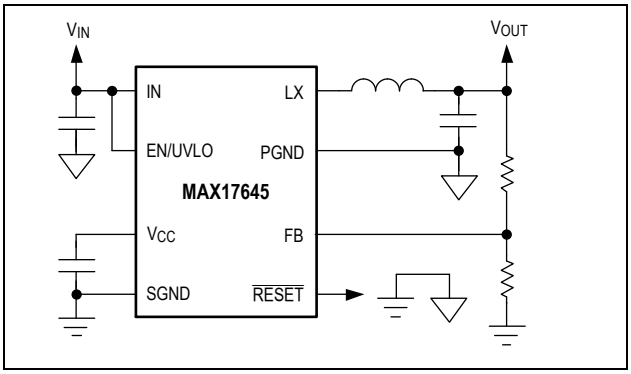
## Product Highlights

- Reduces External Components and Total Cost
  - No Schottky—Synchronous Operation
  - Internal Control Loop Compensation
  - Internal Soft-Start
  - All ceramic Capacitors, Ultra-Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 36V Input Voltage Range
  - Adjustable Output from 0.9V up to 89% of $V_{IN}$
  - Delivers Up to 1A Load Current
- High Efficiency
  - 90% Full-Load Efficiency ($V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 1A)
  - 2.2µA (typ) Shutdown Current
  - High Light-Load Efficiency with PFM Mode (MAX17645D)
- Flexible Design
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Output
  - Open-Drain Output ($\overline{RESET}$) for Output Status Monitoring
- Robust Operation
  - Built-in Hiccup Mode Overload Protection
  - Overtemperature Protection
  - CISPR32 Class B Compliant
  - Wide -40°C to +125°C Ambient Operating Temperature/-40°C to +150°C Junction Temperature

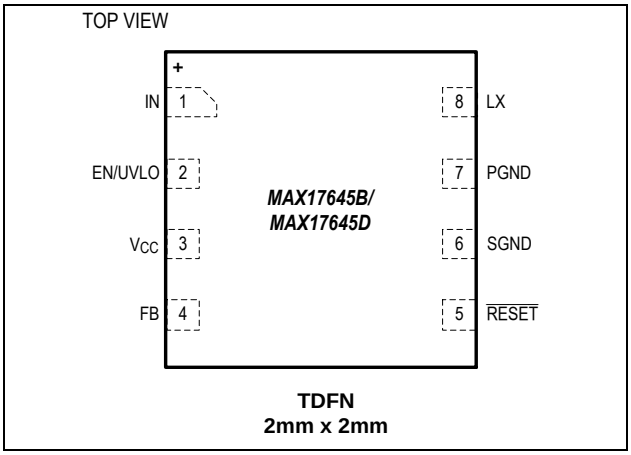
## Key Applications

- Factory Automation
  Within the many different applications in the Factory Automation space, one key need is the ability to generate less heat. Heat within the system needs to be managed to prevent overheating and shutdown. The MAX17645 dissipates less heat as it is a fully synchronous integrated FET DC-DC converter with high efficiency.
- Aftermarket Market Automotive
  Asset tracking application is an example within the aftermarket automotive space where the MAX17645 would provide a benefit. Asset tracking has increased in popularity, as the ability to wirelessly connect to the monitors has become easier. Typically, these units are designed to be as small as possible. The MAX17645 has integrated FETS and integrated compensation, all delivered in a small solution size. Small size and fewer components help to reduce overall design costs for the system.
- General Point of Load
  General point of load is a generic term that applies to a switching regulator that serves many applications and design environments. Critical to any environment is the robustness of the power conversion. With an operating range of -40°C to +125°C, current limit protection, overtemperature protection, and the ability to adhere to the CISPR32 class B emission standards, the MAX17645 delivers a small, high efficient power conversion in the most adverse environments and provides the designer the peace of mind that it is robust and reliable.

## Simplified Application Diagram




## Pin Description




***Ordering Information* appears at end of data sheet.**

*19-101430; Rev 1; 3/22*

## Absolute Maximum Ratings

$V_{IN}$ to PGND .....-0.3V to +40V

EN/UVLO to SGND ..... -0.3V to ($V_{IN}$ + 0.3V)

LX to PGND..... -0.3V to ($V_{IN}$ + 0.3V)

$V_{CC}$, FB to SGND .....-0.3V to +6.0V

$\overline{RESET}$ to SGND .....-0.3V to +5.5V

PGND to SGND.....-0.3V to +0.3V

LX total RMS Current ..... ±1.2A

Output Short-Circuit Duration..... Continuous

Continues Power Dissipation ($T_A$ = +70°C) 8-Pin TDFN (derate 13.9mW/°C above +70°C).....1110mW

Operating Temperature Range (Note 1)..... -40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Soldering Temperature (reflow)..... +260°C

Lead Temperature (soldering, 10s) ..... +300°C

**Note 1:** Junction temperature greater than +125°C degrades operating lifetimes.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| **8 TDFN** | |
|---|---|
| Package Code | T822CN+1 |
| Outline Number | 21-0487 |
| Land Pattern Number | 90-0349 |
| **Thermal Resistance, Four Layer Board*** | |
| Junction-to-Ambient ($\theta_{JA}$) | 72°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 20°C/W |

***Package thermal resistances were obtained using the MAX17645 evaluation kit with no airflow

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages.* Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

## Electrical Characteristics

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{PGND}$ = $V_{SGND}$ = 0V, $C_{VCC}$ = 1µF, $V_{FB}$ = 1V, LX = $\overline{RESET}$ = Unconnected, $T_A$ = -40˚C to +125˚C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to SGND, unless otherwise noted (Note 2))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY ($V_{IN}$)** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 4.5 | | 36 | V |
| Input Shutdown Current | $I_{IN-SH}$ | $V_{EN/UVLO}$ = 0V (Shutdown mode) | | 2.2 | | µA |
| Input Supply Current | $I_{Q-PFM}$ | $V_{FB}$ = 1.03 x $V_{FB\_REG}$ (MAX17645D) | | 115 | 170 | µA |
| | $I_{Q-PWM}$ | Normal switching mode, $V_{FB}$ = 0.8V (MAX17645B) | | 3.85 | | mA |
| **ENABLE/UVLO (EN/UVLO)** | | | | | | |
| EN/UVLO Threshold | $V_{ENR}$ | $V_{EN/UVLO}$ rising | 1.19 | 1.215 | 1.24 | V |
| | $V_{ENF}$ | $V_{EN/UVLO}$ falling | 1.06 | 1.09 | 1.15 | |
| | $V_{EN-TRUESD}$ | $V_{EN/UVLO}$ falling, true shutdown | | 0.75 | | |
| EN/UVLO Input Leakage Current | $I_{EN/UVLO}$ | 0 ≤ $V_{EN/UVLO}$ ≤ 1.5V, $T_A$ = +25°C | -50 | | +50 | nA |
| **LDO ($V_{CC}$)** | | | | | | |
| $V_{CC}$ Output Voltage Range | $V_{CC}$ | 6V ≤ $V_{IN}$ ≤ 36V, 0mA < $I_{VCC}$ < 10mA | 4.75 | 5 | 5.25 | V |
| $V_{CC}$ Current Limit | $I_{VCC-MAX}$ | $V_{CC}$ = 4.3V, $V_{IN}$ = 12V | 15 | 35 | 55 | mA |
| $V_{CC}$ Dropout | $V_{CC-DO}$ | $V_{IN}$ = 4.5V, $I_{VCC}$ = 5mA | | 0.15 | 0.3 | V |
| $V_{CC}$ UVLO | $V_{CC-UVR}$ | $V_{CC}$ rising | 4.05 | 4.18 | 4.3 | V |
| | $V_{CC-UVF}$ | $V_{CC}$ falling | 3.7 | 3.8 | 3.95 | |
| **POWER MOSFETs** | | | | | | |
| High-Side pMOS On-Resistance | $R_{DS-ONH}$ | $I_{LX}$ = 0.3A, (sourcing) | | 500 | 925 | mΩ |
| Low-Side nMOS On-Resistance | $R_{DS-ONL}$ | $I_{LX}$ = 0.3A, (sinking) | | 165 | 300 | mΩ |
| LX Leakage Current | $I_{LX-LKG}$ | $V_{EN/UVLO}$ = 0V, $V_{LX}$ = ($V_{GND}$ + 1V) to ($V_{IN}$ -1V), $T_A$ = $T_J$ = 25°C | -100 | | +100 | nA |
| **SOFT-START (SS)** | | | | | | |
| Soft-Start Time | $t_{SS}$ | | 2.9 | 3.15 | 3.4 | ms |
| **FEEDBACK (FB)** | | | | | | |
| FB Regulation Voltage | $V_{FB-REG}$ | MAX17645B | 0.890 | 0.9 | 0.910 | V |
| | | MAX17645D | 0.890 | 0.915 | 0.936 | |
| FB Leakage Current | $I_{FB}$ | $T_A$ = $T_J$ = 25°C | | -25 | | nA |
| **CURRENT LIMIT** | | | | | | |
| Peak Current-Limit Threshold | $I_{PEAK-LIMIT}$ | | 1.65 | 1.88 | 2.1 | A |
| Runaway Current-Limit Threshold | $I_{RUNAWAY-LIMIT}$ | | 2.05 | 2.44 | 2.7 | A |
| Negative Current-Limit Threshold | $I_{NEG-LIMIT}$ | MAX17645B | -1.26 | -1.1 | -0.9 | A |
| | | MAX17645D | -50 | 0 | 50 | mA |
| PFM Peak Current Limit Threshold | $I_{PFM}$ | MAX17645D | 0.38 | 0.43 | 0.48 | A |
| **Timing** | | | | | | |

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{PGND}$ = $V_{SGND}$ = 0V, $C_{VCC}$ = 1µF, $V_{FB}$ = 1V, LX = $\overline{RESET}$ = Unconnected, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to SGND, unless otherwise noted (Note 2))

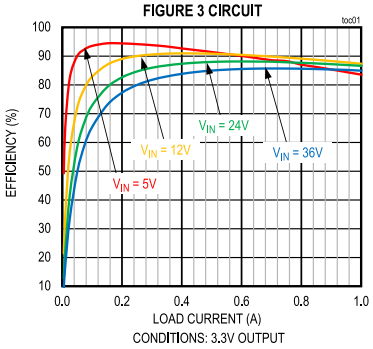
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Switching Frequency | $f_{SW}$ | | 605 | 650 | 695 | kHz |
| Number of Runaway Events to Hiccup | | | | 1 | | Cycles |
| $V_{FB}$ Undervoltage Trip Level to Cause Hiccup | $V_{FB-HICF}$ | | 0.56 | 0.58 | 0.6 | V |
| HICCUP Timeout | | | | 100 | | ms |
| Minimum On-Time | $t_{ON-MIN}$ | | | 90 | 120 | ns |
| Maximum Duty Cycle | $D_{MAX}$ | | 89 | 91 | 94 | % |
| LX Dead Time | $t_{DT}$ | | | 5 | | ns |
| **$\overline{RESET}$** | | | | | | |
| FB Threshold for $\overline{RESET}$ rising | | $V_{FB}$ rising | 93.5 | 95.5 | 97.5 | % |
| FB Threshold for $\overline{RESET}$ falling | | $V_{FB}$ falling | 90 | 92 | 94 | % |
| $\overline{RESET}$ Delay After FB Reaches 95.5% Regulation | | | | 1.6 | | ms |
| $\overline{RESET}$ Output Level Low | | $I_{\overline{RESET}}$ = 5mA | | | 0.2 | V |
| $\overline{RESET}$ Output Leakage Current | | $V_{\overline{RESET}}$ = $V_{CC}$, $T_A$ = +25°C | | | 0.1 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Threshold | | Temperature rising | | 166 | | °C |
| Thermal Shutdown Hysteresis | | | | 10 | | °C |

**Note 2:** Electrical specifications are production tested at $T_A$ = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.

## Typical Operating Characteristics

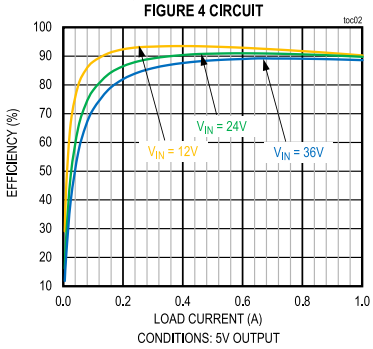
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{PGND}$ = $V_{SGND}$ = 0V, $C_{VCC}$ = 1µF, $T_A$ = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17645B, EFFICIENCY vs. LOAD CURRENT
FIGURE 3 CIRCUIT



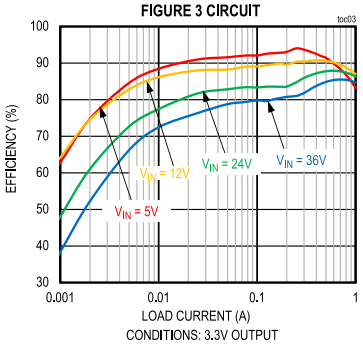

CONDITIONS: 3.3V OUTPUT

MAX17645B, EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



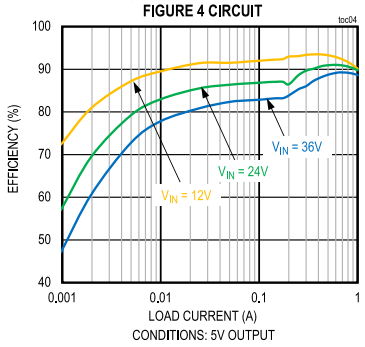

CONDITIONS: 5V OUTPUT

MAX17645D, EFFICIENCY vs. LOAD CURRENT
FIGURE 3 CIRCUIT



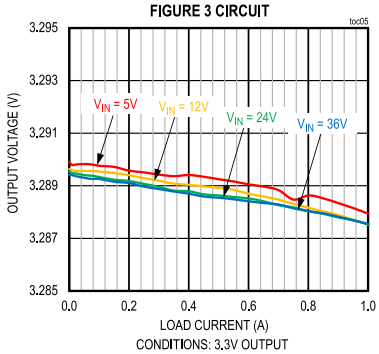

CONDITIONS: 3.3V OUTPUT

MAX17645D, EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



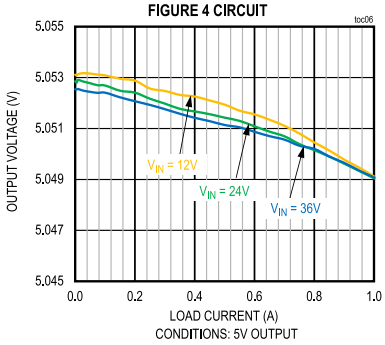

CONDITIONS: 5V OUTPUT

MAX17645B, LINE AND LOAD REGULATION
FIGURE 3 CIRCUIT



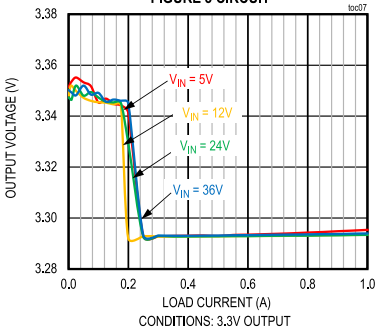

CONDITIONS: 3.3V OUTPUT

MAX17645B, LINE AND LOAD REGULATION
FIGURE 4 CIRCUIT



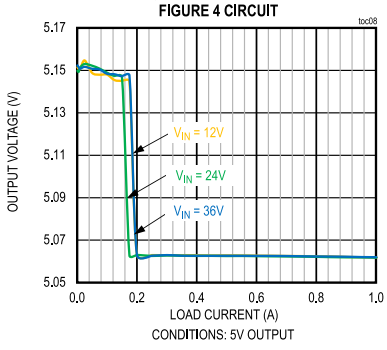

CONDITIONS: 5V OUTPUT

MAX17645D, LINE AND LOAD REGULATION
FIGURE 3 CIRCUIT



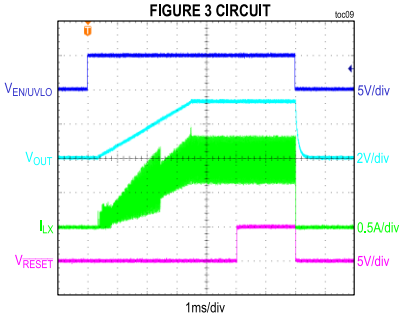

CONDITIONS: 3.3V OUTPUT

MAX17645D, LINE AND LOAD REGULATION
FIGURE 4 CIRCUIT




CONDITIONS: 5V OUTPUT

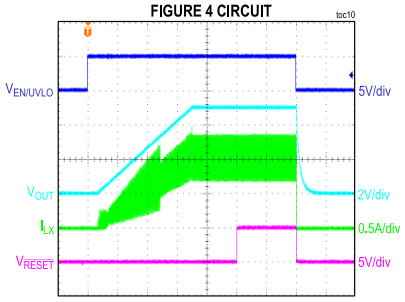
MAX17645B/MAX17645D
SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 3 CIRCUIT




CONDITIONS: 3.3V OUTPUT, 3.3Ω LOAD

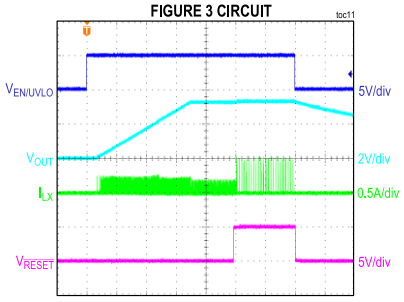
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{PGND}$ = $V_{SGND}$ = 0V, $C_{VCC}$ = 1µF, $T_A$ = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17645B/MAX17645D
SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 4 CIRCUIT



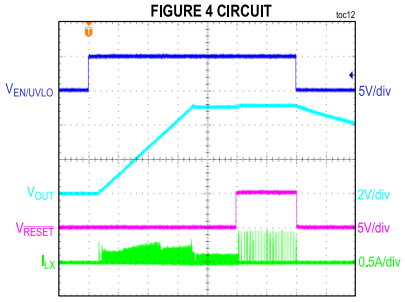

CONDITIONS: 5V OUTPUT, 5Ω LOAD

MAX17645D
SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 3 CIRCUIT



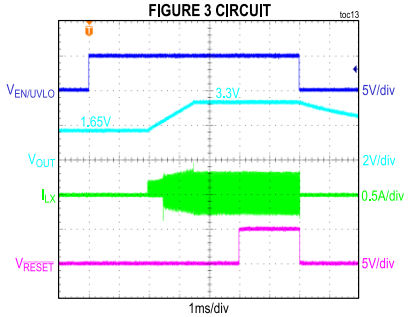

CONDITIONS: 3.3V OUTPUT, 330Ω LOAD

MAX17645D
SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 4 CIRCUIT



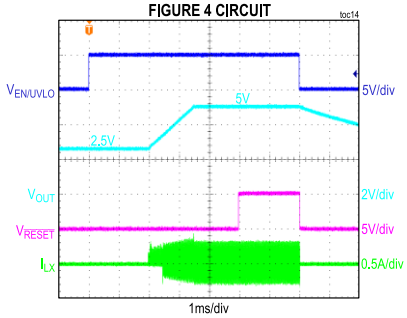

CONDITIONS: 5V OUTPUT, 500Ω LOAD

MAX17645B
SOFT-START WITH PREBIAS OF VOLTAGE 1.65V
FIGURE 3 CIRCUIT



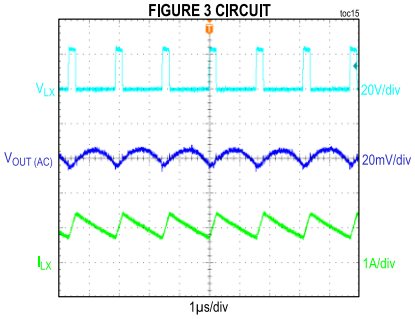

CONDITIONS: 3.3V OUTPUT, 330Ω LOAD

MAX17645B
SOFT-START WITH PREBIAS OF VOLTAGE 2.5V
FIGURE 4 CIRCUIT



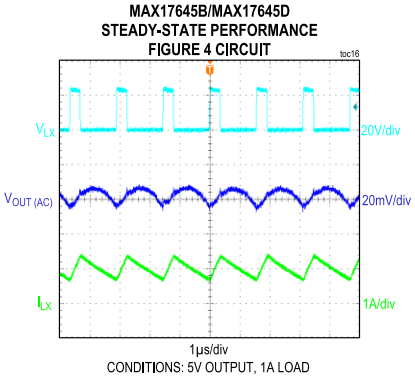

CONDITIONS: 5V OUTPUT, 500Ω LOAD

MAX17645B/MAX17645D
STEADY-STATE PERFORMANCE
FIGURE 3 CIRCUIT



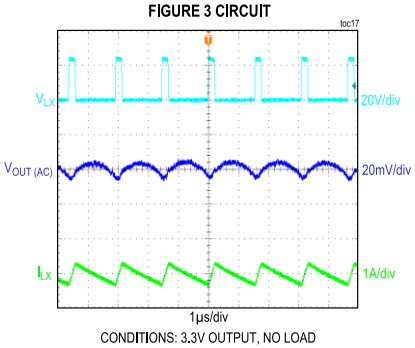

CONDITIONS: 3.3V OUTPUT, 1A LOAD

MAX17645B/MAX17645D
STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT



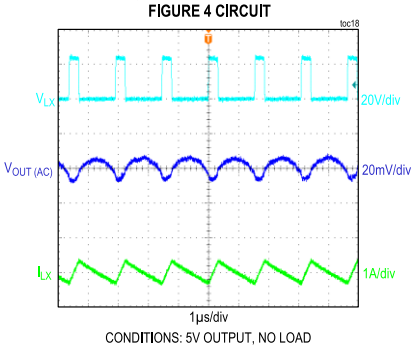

CONDITIONS: 5V OUTPUT, 1A LOAD

MAX17645B, STEADY-STATE PERFORMANCE
FIGURE 3 CIRCUIT




CONDITIONS: 3.3V OUTPUT, NO LOAD

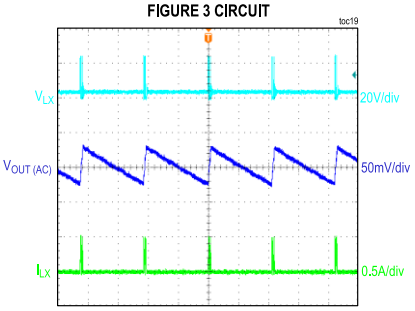
MAX17645B, STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT




CONDITIONS: 5V OUTPUT, NO LOAD

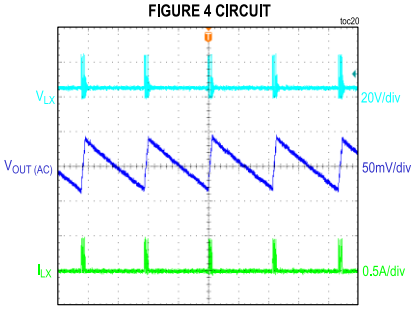
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{PGND}$ = $V_{SGND}$ = 0V, $C_{VCC}$ = 1µF, $T_A$ = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

**MAX17645D, STEADY-STATE PERFORMANCE**
**FIGURE 3 CIRCUIT**



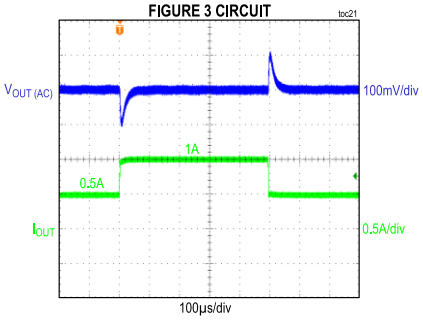

CONDITIONS: 3.3V OUTPUT, 10mA LOAD

**MAX17645D, STEADY-STATE PERFORMANCE**
**FIGURE 4 CIRCUIT**



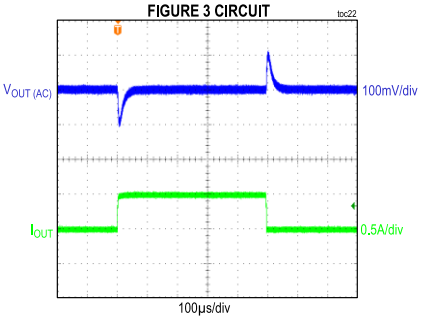

CONDITIONS: 5V OUTPUT, 10mA LOAD

**MAX17645B/MAX17645D**
**LOAD TRANSIENT BETWEEN 0.5A AND 1A**
**FIGURE 3 CIRCUIT**



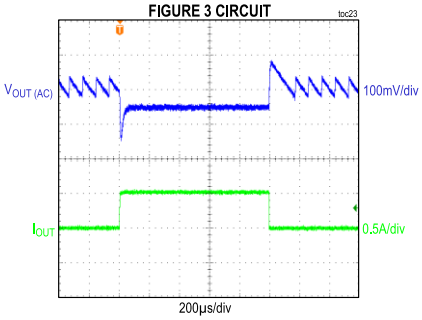

CONDITIONS: 3.3V OUTPUT

**MAX17645B**
**LOAD TRANSIENT BETWEEN 0A AND 0.5A**
**FIGURE 3 CIRCUIT**



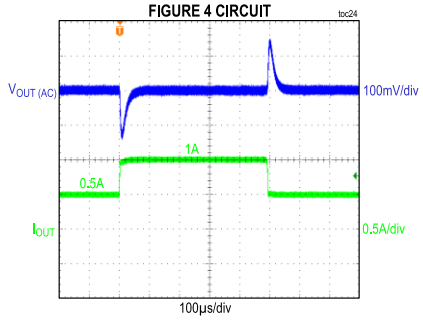

CONDITIONS: 3.3V OUTPUT

**MAX17645D**
**LOAD TRANSIENT BETWEEN 0.01A AND 0.5A**
**FIGURE 3 CIRCUIT**



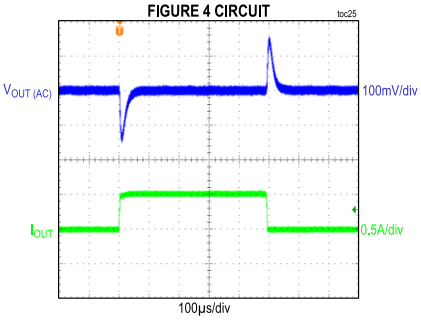

CONDITIONS: 3.3V OUTPUT

**MAX17645B/MAX17645D**
**LOAD TRANSIENT BETWEEN 0.5A AND 1A**
**FIGURE 4 CIRCUIT**



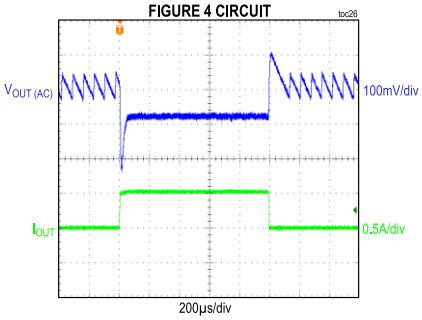

CONDITIONS: 5V OUTPUT

**MAX17645B**
**LOAD TRANSIENT BETWEEN 0A AND 0.5A**
**FIGURE 4 CIRCUIT**



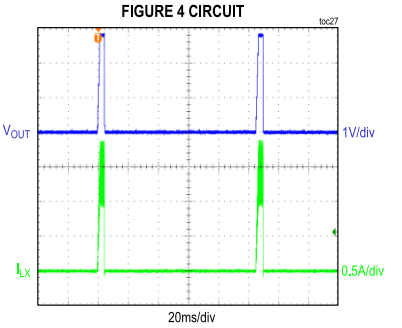

CONDITIONS: 5V OUTPUT

**MAX17645D**
**LOAD TRANSIENT BETWEEN 0.01A AND 0.5A**
**FIGURE 4 CIRCUIT**




CONDITIONS: 5V OUTPUT

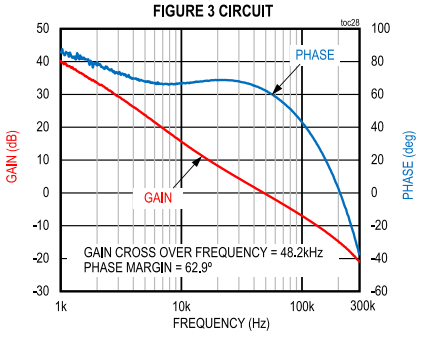
**MAX17645B, OVERLOAD PROTECTION**
**FIGURE 4 CIRCUIT**




CONDITIONS: 5V OUTPUT, R_LOAD = 2.1Ω

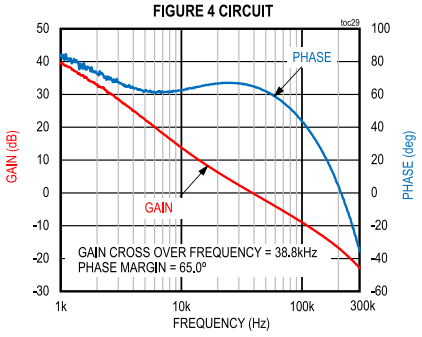
($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{PGND}$ = $V_{SGND}$ = 0V, $C_{VCC}$ = 1µF, $T_A$ = +25°C, unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

**MAX17645B, BODE PLOT**
**FIGURE 3 CIRCUIT**



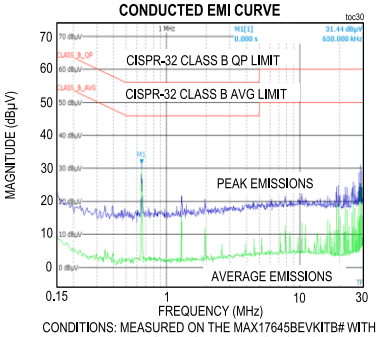

CONDITIONS: 3.3V OUTPUT, 1A LOAD

**MAX17645B, BODE PLOT**
**FIGURE 4 CIRCUIT**



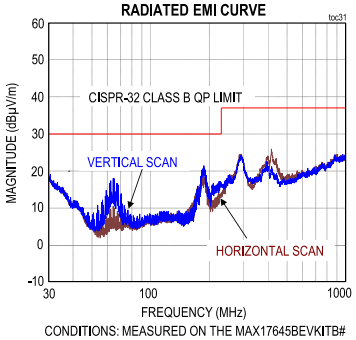

CONDITIONS: 5V OUTPUT, 1A LOAD

**MAX17645B, 5V OUTPUT, 1A LOAD CURRENT**
**CONDUCTED EMI CURVE**



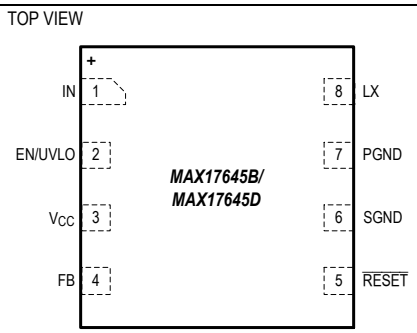

CONDITIONS: MEASURED ON THE MAX17645BEVKITB# WITH L102 = 10µH, C107 = C108 = 4.7µF/50V/X7R/1206

**MAX17645B, 5V OUTPUT, 1A LOAD CURRENT**
**RADIATED EMI CURVE**




CONDITIONS: MEASURED ON THE MAX17645BEVKITB#

## Pin Configuration

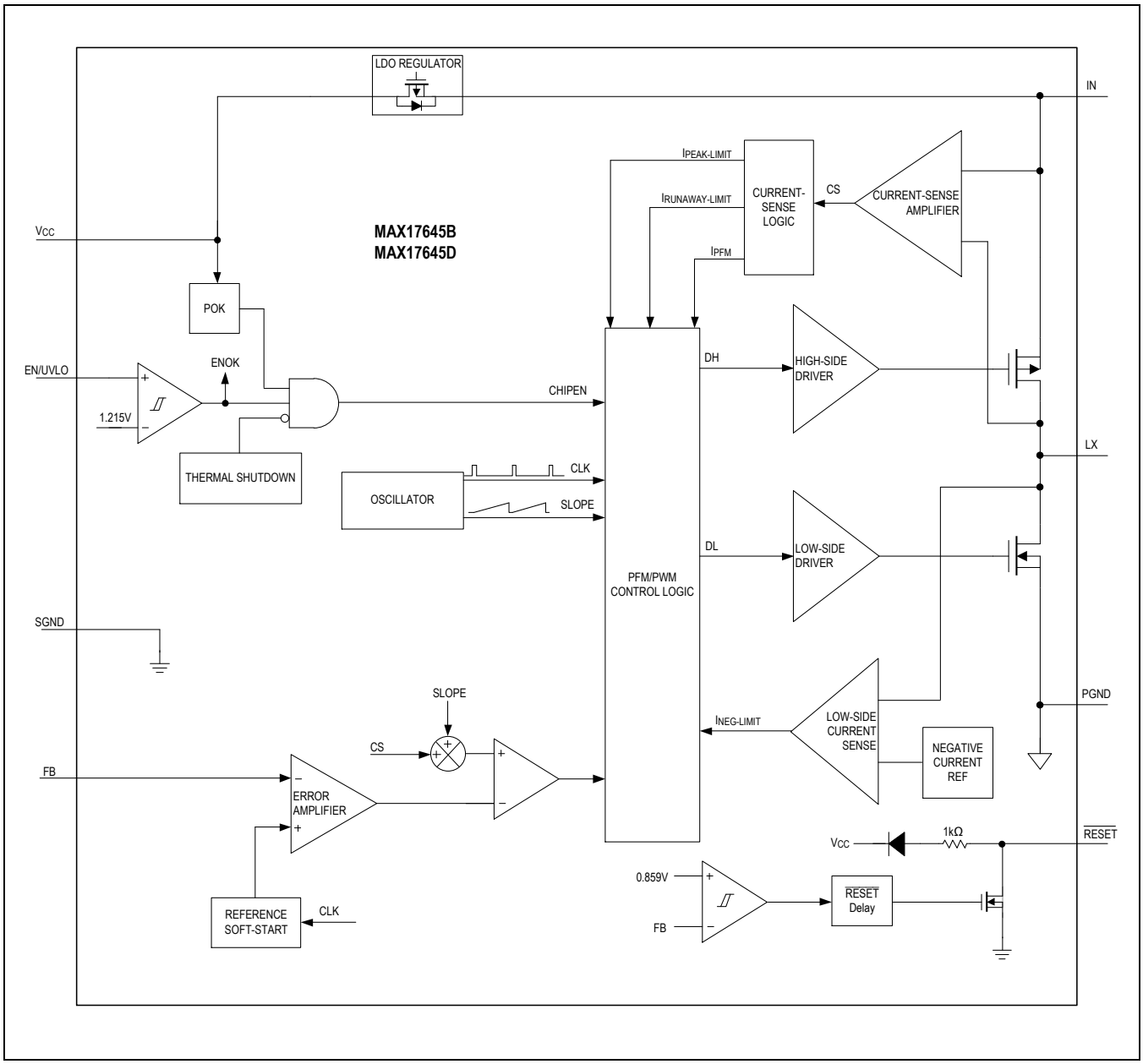



**TDFN**
**2mm x 2mm**

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | IN | Power Supply Input Pin. Decouple to PGND with a 2.2µF capacitor. Place the capacitor close to IN and PGND pins. |
| 2 | EN/UVLO | Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output and low to disable the output. Connect to the center of a resistor-divider between IN and SGND to program the input voltage at which the part turns on. Connect to IN pin for always-on operation. |
| 3 | $V_{CC}$ | Internal LDO Output. Typical output is 5V. Bypass $V_{CC}$ with a 1µF capacitor to SGND. |
| 4 | FB | Feedback Input. Connect FB to the center node of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details. |
| 5 | $\overline{RESET}$ | Open-Drain $\overline{RESET}$ Output. The $\overline{RESET}$ output is driven low if FB drops below 92% (typ) of its set value. $\overline{RESET}$ goes high impedance 1.6ms (typ) after FB rises above 95.5% (typ) of its set value. See *Electrical Characteristics* section for more details. |
| 6 | SGND | Signal Ground. |
| 7 | PGND | Power Ground. Connect PGND to the power ground plane. Connect SGND and PGND pins together at the ground return path of the output capacitor. See the *PCB Layout Guidelines* section. |
| 8 | LX | Switching Node Pin. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode. |

## Functional Diagram



## Detailed Description

The MAX17645 is a high-efficiency, high voltage, synchronous step-down DC-DC converter with integrated MOSFETs, operates over a 4.5V to 36V input. It can deliver up to 1A load current. The MAX17645 operates at 650kHz switching frequency. The MAX17645B operates in pulse-width modulation (PWM) mode at all loads. The MAX17645D operates in pulse-frequency modulation (PFM) mode at light loads. The output voltage is programmable from 0.9V up to 89% of $V_{IN}$. Built-in control loop compensation across the output voltage range eliminates the need for external compensation components. The feedback voltage regulation accuracy over -40°C to +125°C is ±1.1%.

The device features a peak-current-mode control architecture. In this architecture, while operating in PWM mode the part sets the duty cycle using a transconductance error amplifier, a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the rest of the switching cycle, the high-side MOSFET remains off and the low-side MOSFET remains on, inductor current ramps down. An appropriate dead time is implemented between the high-side and low-side state transitions to avoid cross conduction.

A fixed soft-start time of 3.15ms (typ) allows users to reduce input inrush current. The device also features an enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain $\overline{\text{RESET}}$ feature provides a power-good signal to the system upon achieving successful regulation of the output voltage.

### PWM Mode Operation

The MAX17645B operates in PWM mode, where the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM mode of operation as the converter switches in every clock cycle.

### PFM Mode Operation

The MAX17645D operates in PFM mode, which disables negative inductor current. In PFM operation, the part skips pulses and enters hibernate mode at light loads for higher efficiency. In PFM mode, the inductor current is forced to a fixed peak of 430mA (typ) every clock cycle until the output rises to 102.3% of its nominal voltage. Once the output reaches 102.3% of its nominal voltage, both high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of its nominal voltage. Most of the internal blocks are turned off in hibernate operation to reduce quiescent current. After the output falls below 101.1% of its nominal voltage, the device comes out of hibernate operation and initiates the process of delivering pulses of energy to the output until it reaches 102.3% of its nominal output voltage. The hibernate operation improves the light-load efficiency in PFM mode. The trade-off is that the output-voltage ripple is higher compared to PWM mode of operation and the switching frequency is not fixed at light loads.

### Linear Regulator

The MAX17645 has an internal Low Dropout (LDO) regulator which powers $V_{CC}$. During power-up, when the EN/UVLO pin voltage is above the true shutdown voltage ($V_{EN-TRUESD}$), $V_{CC}$ is powered from IN. Typical $V_{CC}$ output voltage is 5V. Bypass $V_{CC}$ to SGND with a 1µF low-ESR ceramic capacitor. $V_{CC}$ powers the internal blocks and driver stage of the power MOSFETs. The part is enabled when the $V_{CC}$ voltage rises above $V_{CC-UVR}$ (4.18 typ). The part is disabled when $V_{CC}$ voltage falls below $V_{CC-UVF}$ (3.8V typ).

### Enable/Undervoltage-Lockout Input

The device offers an adjustable input undervoltage-lockout (EN/UVLO) to enable or disable the converter. EN/UVLO can also be used as an input-voltage UVLO adjustment input. Driving EN/UVLO low (below $V_{ENF}$) disables both power MOSFETs. Driving EN/UVLO very low (below $V_{EN-TRUESD}$) disables both power MOSFETs as well as other internal circuitry, and reduces IN quiescent current to below 2.2µA (typ). Driving EN/UVLO high (above $V_{ENR}$) enables the converter. Connect EN/UVLO to IN pin for always-on operation. An external voltage-divider between IN and EN/UVLO to SGND adjusts the input voltage at which the device turns on or off. See the *Setting the Input Undervoltage-Lockout Level* section for more details.

When EN/UVLO voltage is above 1.215V (typ), the device's internal error-amplifier reference voltage starts to ramp up to monotonically raise the output voltage to the set level. The duration of the soft-start ramp is 3.15ms (typ), allowing a smooth increase of the output voltage.

The device is capable of soft-start into a prebiased output, without discharging the output capacitor in both the PFM and forced-PWM modes. This feature is useful in applications where digital integrated circuits with multiple rails are powered.

### $\overline{\text{RESET}}$ Output

The device includes a comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes to high impedance 1.6ms (typ) after the regulator output voltage rises above 95.5% (typ) of the nominal set voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops below 92% (typ) of the nominal set voltage. $\overline{\text{RESET}}$ also goes low during hiccup timeout period and thermal shutdown.

### Overcurrent Protection/Hiccup Mode

The device has a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side MOSFET current exceeds an internal limit of 1.88A (typ). A runaway current limit on the high-side MOSFET at 2.44A (typ) protects the device under high input voltage, and short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers hiccup mode. In addition, hiccup mode is triggered if the feedback voltage drops to $V_{FB-HICF}$ any time after soft-start is complete due to a fault condition. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 100ms (typ). Once the hiccup timeout period expires, soft-start is attempted again. The hiccup mode of operation ensures low power dissipation under an output short-circuit condition.

### Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +166°C (typ), a thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C (typ). Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection during normal operation.

## Applications Information

### Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output-voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}\right)\right)}{D_{MAX}} + \left(I_{OUT(MAX)} \times \left(R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)}\right)\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\text{-}MIN(MAX)}}$$

where:

$V_{OUT}$ = Steady-state output voltage in V

$I_{OUT(MAX)}$ = Maximum load current in A

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor in Ω

$f_{SW(MAX)}$ = Maximum switching frequency in Hz

$D_{MAX}$ = Maximum duty cycle (0.89)

$t_{ON\text{-}MIN(MAX)}$ = Worst-case minimum switch on-time (120ns)

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst case on-state resistance of low-side and high-side MOSFETs respectively in Ω

### Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source, switching noise, and voltage ripple on the input. The input capacitor RMS current requirement ($I_{RMS}$) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where $I_{OUT(MAX)}$ is the maximum load current. $I_{RMS}$ has a maximum value when the input voltage equals twice the output voltage ($V_{IN}$ = 2 x $V_{OUT}$), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Decouple IN to PGND with a minimum of 2.2µF/1206 package or equivalent capacitor. Calculate the input capacitance using the following equation based on input ripple requirement:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times \Delta V_{IN} \times f_{SW}}$$

where:

D = $V_{OUT}/V_{IN}$ and is the duty ratio of the converter

$\Delta V_{IN}$ = Allowable input voltage ripple in V

$f_{SW}$ = Switching frequency in Hz

η = Efficiency of the converter

In applications where the source is far from the device input, an appropriate electrolytic capacitor should be added to provide necessary damping of potential oscillations caused by the inductance of the input power path and input ceramic capacitor.

## Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current ($I_{SAT}$), and DC resistance ($R_{DCR}$). The required minimum inductance for a given application can be determined from the following equation:

$$L = 2 \times V_{OUT}$$

where L is inductance in µH and $V_{OUT}$ is output voltage in V. Select a low-loss inductor closest to the calculated value with acceptable dimensions. The saturation current rating ($I_{SAT}$) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit, $I_{PEAK-LIMIT}$ (1.88A typ).

## Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in application. The output capacitor is calculated and sized to support a 50% of maximum output current as the dynamic step load, and to contain the output-voltage deviation to within ±3% of the nominal set voltage. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{50}{V_{OUT}}$$

Where $C_{OUT}$ is the DC bias derated output capacitance in µF and $V_{OUT}$ is the output voltage.

## Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from IN to SGND (see *Figure 1*). Connect the center node of the divider to the EN/UVLO pin. Choose R1 to be 3.32MΩ (max) and then calculate R2 as follows:

$$R2 = \frac{R1 \times V_{ENR}}{(V_{INU} - V_{ENR})}$$

where $V_{INU}$ is the voltage at which the device is required to turn on. Ensure that the proper $V_{INU}$ voltage is set, which is greater than or equal to the minimum input voltage for desired output voltage. If the EN/UVLO pin is driven from an external signal source, a series resistance of 1kΩ minimum is recommended to be placed between the signal source output and the EN/UVLO pin to reduce voltage ringing on the line.

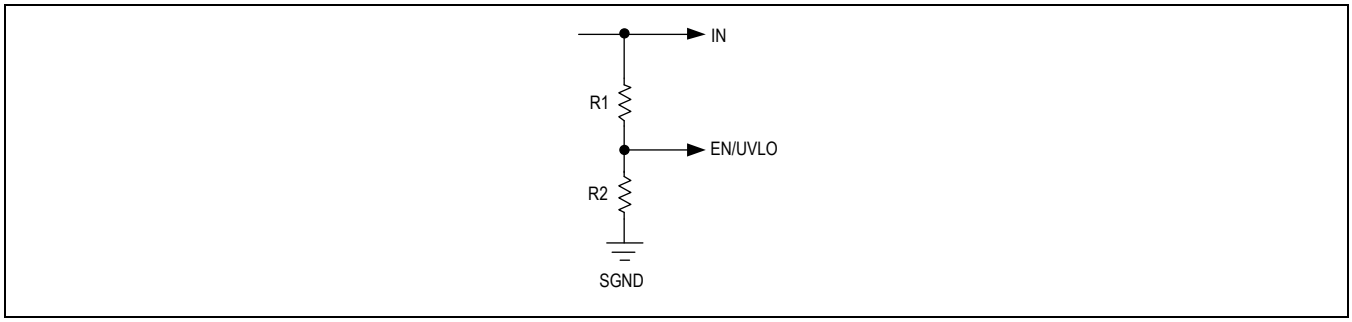



*Figure 1. Setting the Input Undervoltage-Lockout*

## Adjusting Output Voltage

The device supports an adjustable output voltage range of 0.9V to 89% of input voltage by using a resistive feedback divider from output to SGND (see *Figure 2*). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Choose R4 in the 20kΩ to 50kΩ range and calculate R3 with the following equation:

$$R3 = R4 \times \left[\frac{V_{OUT}}{0.9} - 1\right]$$

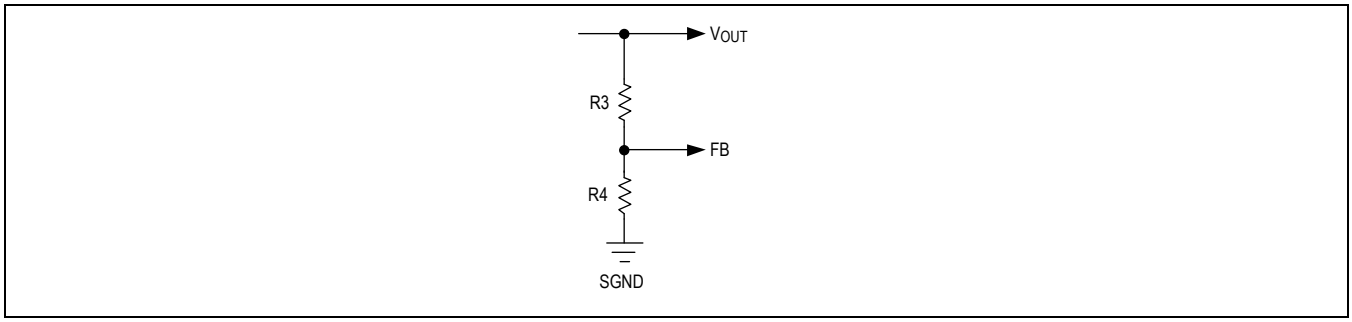



*Figure 2. Adjusting Output Voltage*

## Power Dissipation

At any particular operating condition, the power loss that contribute to temperature rise of the device is estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left(\frac{1}{\eta} - 1\right) - \left({I_{OUT}}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

$P_{OUT}$ = Output power

η = Efficiency of the converter

$R_{DCR}$ = DC resistance of the inductor

See *Typical Operating Characteristics* for more information on efficiency at typical operating conditions. The Theta-JA ($\theta_{JA}$) of the package measured on a standard EV kit is given below:

$$\theta_{JA} = 72°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{LOSS}\right)$$

Junction temperature greater than +125°C degrades operating lifetimes.

## PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pin of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the $V_{CC}$ pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity. PCB layout also affects the thermal performance of the design. For a sample layout that ensures first pass success, refer to the MAX17645 evaluation kit layout available at www.maximintegrated.com.

## Typical Application Circuits

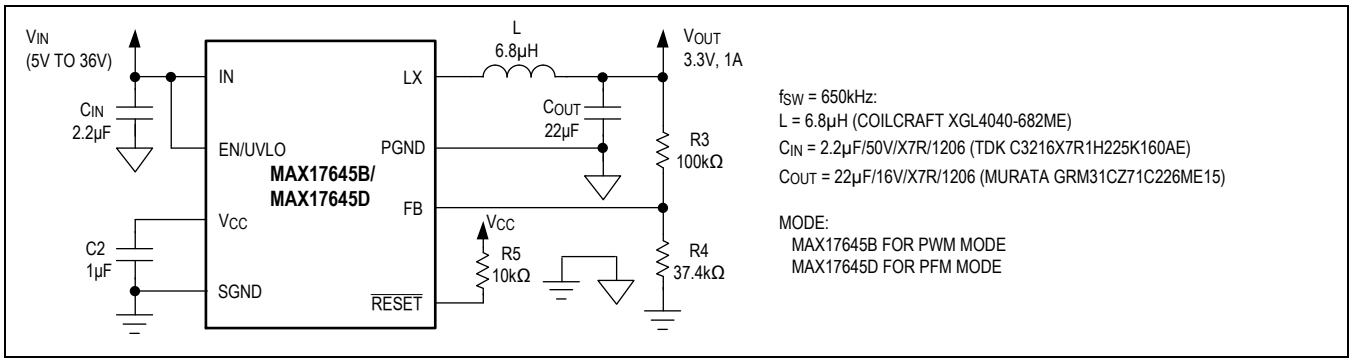



*Figure 3. 3.3V, 1A Output Step-Down Regulator*

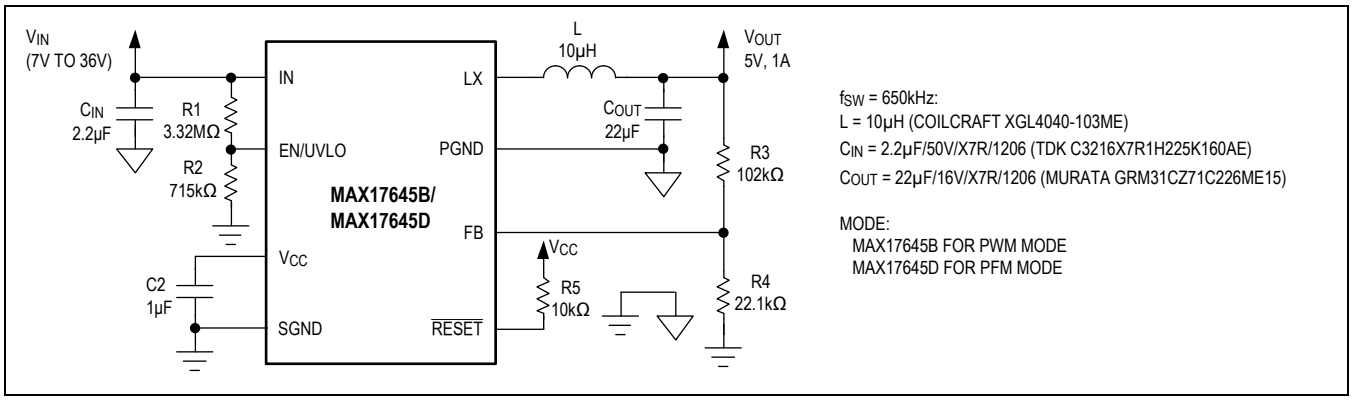



*Figure 4. 5V, 1A Output Step-Down Regulator*

## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE | MODE OF OPERATION |
|---|---|---|---|
| MAX17645BATA+ | -40°C to +125°C | 8 TDFN | PWM |
| MAX17645BATA+T | -40°C to +125°C | 8 TDFN | PWM |
| MAX17645DATA+ | -40°C to +125°C | 8 TDFN | PFM |
| MAX17645DATA+T | -40°C to +125°C | 8 TDFN | PFM |

*+ Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape and reel.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 3/22 | Release for Market Intro | — |
| 1 | 3/22 | Updated part number in header | 1–22 |