MAX14922

High-Side Switch Controller with Current Limiting

General Description

The MAX14922 is a high-side, n-channel FET controller for implementing industrial high-side switches for switching ground-connected loads. The MAX14922 device controls an external nMOS power transistor, allowing low R_{ON} high-side switch applications from a +9V to +70V supply range.

Fast inductive load turn-off can be achieved with use of a high-voltage TVS diode enabling up to -70V (max) voltage clamping. Ground-connected TVS diodes allow clamping of exceptionally high inductive energies.

Load current is limited to a user-defined value through a sense resistor. External FET overload protection is achieved using an auto-retry timing feature, as defined by a user-selected capacitor (C_{BLANK} at t_{BLANK} input) or optionally using an external timing control.

The MAX14922 features an on-chip comparator enabling monitoring of the high-side switch output or the supply input voltage with a user-selected threshold. An integrated charge pump enables high speed switching rates when using low R_{ON} FETs in the 20kHz to 50kHz range.

The MAX14922 is available in a 3mm x 3mm, 16-TQFN package. The MAX14922 device is specified over the -40ºC to +125ºC operating temperature range.

Applications

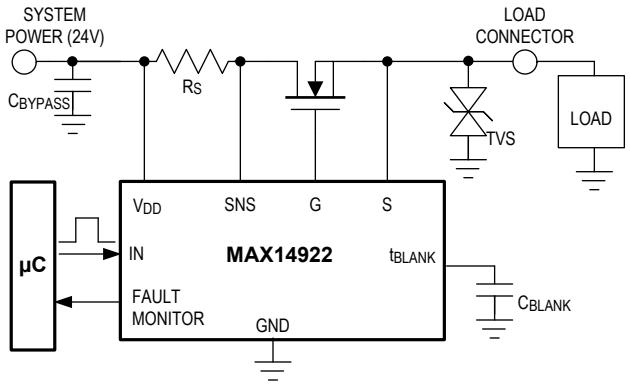
- Industrial Digital Outputs
- High-Side Switches
- Motor Holding Brakes
- Relay and Solenoid Drivers

Benefits and Features

- +9V to +70V Operating Supply Range
- 5V / 50mA Integrated Linear Regulator
- -40°C to +125°C Ambient Temperature Operating Range
- 16-TQFN Package, 3mm x 3mm, 0.5mm Pin Pitch
- Robust Design Features
  - Ultra High-Speed Inductive Load Turn-Off by Clamping to -70V
  - Supply Independent Inductive Clamping
  - Support of Low R_{ON} FETs Having Q_g (Total) = 50nC
  - External FET Turn-On Propagation Delay < 20µs
  - Active Current Limit Control During Overcurrent
- Fault Monitoring Diagnostic Features
  - Overcurrent Detect Output
  - High Supply-Voltage Indication
  - Flexible Supply or Load Voltage Monitor
  - Undervoltage Lockout
  - Thermal Warning and Shutdown Protection
  - Device Ready Indication

Ordering Information appears at end of data sheet.

Simple High-Side Switch Application



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Absolute Maximum Ratings

V_{DD} (Continuous) ..... -0.3V to +75V
V_{DD} (100µs) ..... -0.3V to +85V
SNS (Continuous) .....(V_{DD} - 0.3V) to (V_{DD} + 0.3V)
SNS (100µs) ..... -0.3V to (V_{DD} + 6V)
S ..... -70V to (V_{DD} + 6V)
G ..... (S - 0.3V) to min(S + 18, CP + 0.3V)
CP .....(V_{DD} - 0.3V) to (V_{DD} + 18V)
V_L ..... -0.3V to +6V
IN, t_{BLANK}, COMP ..... -0.3V to +6V
V_5, $\overline{OVCURR}$, $\overline{THW}$, RDY, $\overline{OV}$ ..... -0.3V to +6V
$\overline{LO}$ ..... -0.3V to (V_L + 0.3V)
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 23.10mW/°C above +70°C.) 1847.6mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN

Package Code	T1633+5C
Outline Number	21-0136
Land Pattern Number	90-0032
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	68°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	10°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	43.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	4°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = +9V to +70V, V_5 = 5.0V, V_L = 2.5V to 5.5V. T_A = -40°C to +125°C. Typical values are at T_A = +25ºC, V_{DD} = +24V, and V_L = 5V. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply						
Operating Supply Voltage	V_{DD}	Range for which the high-side switch operates normally	9		70	V
Supply Current	I_{DD}	V_{DD} = 24V, IN = X, No Load on V_5		0.9	1.25	mA
Undervoltage-Lockout Threshold	V_{DD_UV}	V_{DD} rising, UV turns active low and G is turned low/off when V_{DD} < V_{DD_UV}	7.7		9.0	V
Undervoltage-Lockout Hysteresis	V_{DD_UVHYST}			0.5		V

Electrical Characteristics (continued)

(V_{DD} = +9V to +70V, V_5 = 5.0V, V_L = 2.5V to 5.5V. T_A = -40°C to +125°C. Typical values are at T_A = +25ºC, V_{DD} = +24V, and V_L = 5V. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE DETECTION ($\overline{OV}$)						
Overvoltage Threshold	V_{DD_OV}	V_{DD} rising; OV turns on low when V_{DD} > V_{DD_OV}	36.5	38.5	40.5	V
Overvoltage-Lockout Hysteresis	V_{DD_OVHYST}			1		
Linear Regulator (V_5)						
Linear Regulator Output Voltage	V_5	0mA to 50mA load current on V_5 (*Note 2*)	4.9	5	5.1	V
V_5 Short-Circuit Current Limit	I_{CL_V5}		50			mA
V_5 Undervoltage Lockout Threshold	V_{5_UVLO}	V_5 rising	3.8		4.2	V
V_5 Undervoltage Lockout Hysteresis	$V_{5\_UVLO\_HYS}$			0.4		V
V_5 Load regulation	ΔV_{5_LDR}	V_{DD} = 24V, 1mA ≤ I_{LOAD_V5} ≤ 50mA (*Note 2*)		0.4	1	%
V_5 Line Regulation	ΔV_{5_LNR}	9V ≤ V_{DD} ≤ 70V, I_{LOAD_V5} = 1mA		0.1	0.5	mV/V
V_5 Load Capacitance	C_{V5}	External capacitance on V_5	0.8	1		µF
Logic Supply (V_L)						
Logic Supply Current	I_{VL}	IN = X		10	16	µA
Logic Supply Input Voltage	V_L		2.5		5.5	V
Logic Supply Undervoltage-Lockout Threshold	V_{L_UVLO}	V_L Rising	1.4		2.1	V
Logic Supply Undervoltage-Lockout Threshold Hysteresis	$V_{L\_UVLO\_HYST}$			100		mV
LOGIC I/O (IN, $\overline{LO}$, RDY, $\overline{OVCURR}$, $\overline{THW}$, $\overline{OV}$)						
Input Voltage High	V_{IH}		0.7 x V_L			V
Input Voltage Low	V_{IL}				0.3 x V_L	V
Input Threshold Hysteresis	V_{I_TH}	V_L = 5.5V		0.35		V
Input Pulldown Resistor	$R_{PULLDOWN}$	IN Input	140	200	260	kΩ
Output Logic High	V_{OH}	$\overline{LO}$, I_{OUT} = -5mA	V_L - 0.2			V
Output Logic Low	V_{OL}	I_{OUT} = +5mA			0.2	V
Output Three-State Leakage	I_{LEAK}	All logic outputs, GND < V < 5V	-1		+1	µA
CURRENT SENSE (SNS)						
Current Limit Threshold	V_{CL}	V_{CL} = (V_{SNS} – V_{DD})	27	30	33	mV

Electrical Characteristics (continued)

(V_{DD} = +9V to +70V, V_5 = 5.0V, V_L = 2.5V to 5.5V. T_A = -40°C to +125°C. Typical values are at T_A = +25ºC, V_{DD} = +24V, and V_L = 5V. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SNS Input Current	I_{SNS}	V_{DD} - 300mV ≤ V_{SNS} ≤ V_{DD} + 300mV	-1		+1	µA
Short-Circuit Current Threshold	SC_{TH}		40			mV
Auto-Retry Current Limiting Timing						
Blanking Time Range	t_{ON_CL}	Settable through t_{BLANK} capacitor, V_{DS} < 3V	0.2		100	ms
Blanking Time External Capacitance	C_{BLANK}	External capacitance to obtain a blanking time between 0.2ms and 100ms	1		500	nF
Blanking Time Accuracy	$t_{ON\_CL\_ACC}$	t_{ON_CL} versus ideal based on 100% accurate capacitor	-15		+15	%
Auto-Retry Duty Cycle		ON to OFF time while in overcurrent	1.6	2	2.5	%
FET CONTROL (G, S)						
Gate-Source On-Voltage	V_{G_ON}	V_{DD} > V_{DD_UV}, IN = HIGH, I_G = 1uA	V_S + 11.9		V_S + 14.1	V
Gate Turn-On Current	I_{G_SRC}	V_{DD} > V_{DD_UV}, IN = HIGH; During external FET turn-on transition	1.5		3.5	mA
Gate Turn-Off Current	I_{G_SNK}	During external FET turn-off transient	1.4		3.4	mA
Gate-Source Resistance In OFF State	R_{GS_OFF}	V_{DD} > V_{DD_UV}, IN = LOW		32	80	Ω
Gate-Source Output Voltage During Current Limiting	$V_{G\_MIN\_REG}$	V_{DD} > V_{DD_UV}, IN = HIGH	V_S + 0.2			V
Charge Pump Output Resistance	CP_{RES}	V_{DD} > V_{DD_UV}		12	18	kΩ
Charge Pump Load Current	CP_{LOAD}	V_{DD} > V_{DD_UV}			300	µA
Source Input Current	I_S	0V < V_S < 70V	-15		+15	µA
THERMAL PROTECTION						
Chip Thermal Shutdown	TC_{SHDN}	Temperature rising		150		°C
Chip Thermal Shutdown Hysteresis	TC_{SHDN_HYST}			10		°C
Chip Thermal Warning	TC_W	Temperature rising		110		°C
Chip Thermal Warning Hysteresis	TC_{W_HYST}			10		°C
PROPAGATION DELAY (IN to G)						
Prop Delay Low To High	t_{PDLH}	Delay from IN to V_{GS} rising to V_{GST} = 9V, C_{GATE} = 3.3nF. See Figure 1		11	20	µs
Prop Delay High To Low	t_{PDHL}	Delay between IN switching low to V_{GS} falling to 4V, C_{GATE} = 3.3nF. See Figure 1		14	20	µs

Electrical Characteristics (continued)

(V_{DD} = +9V to +70V, V_5 = 5.0V, V_L = 2.5V to 5.5V. T_A = -40°C to +125°C. Typical values are at T_A = +25ºC, V_{DD} = +24V, and V_L = 5V. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator Input (COMP)						
Clamp Voltage		I_{COMP} = 1mA			2.8	V
Input Threshold High	V_{TH_COMP}		0.99	1.025	1.06	V
Input Threshold Low	V_{TL_COMP}		0.93	0.975	1.01	V
Input Hysteresis	V_{HYST_COMP}			50		mV
Input Current	I_{IN_COMP}	0V < V_{COMP} < 1.5V			2	uA
Propagation Delay Low To High	t_{PLH_COMP}	Delay from COMP rising from 0V to 1.5V to output	0.3	0.66	1.2	µs
Propagation Delay High To Low	t_{PHL_COMP}	Delay from COMP falling from 1.5V to 0V to output	0.4	0.67	1.3	µs
DEBOUNCE TIMES						
Supply Undervoltage Debounce Time	$t_{VDD\_UV\_DB}$			200		µs
Supply Overvoltage Debounce Time	$t_{VDD\_OV\_DB}$			200		µs
EMC PROTECTION						
ESD IEC Contact Discharge	V_{ESD_C}	S to GND, IEC-61000-4-2 Contact (*Note 3*)		±9		kV
ESD IEC Air Discharge	V_{ESD_A}	S to GND, IEC-61000-4-2 (*Note 3*)		±15		kV
ESD	V_{ESD}	All other pins. Human Body Model		±2		kV
Surge Tolerance	V_{SURGE}	S to GND, IEC61000-4-5 with 42Ω, TVS on S (*Note 3*)		±2		kV

Note 1: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: A regulator with higher output load current creates high power dissipation. A 50mA output load current is only feasible by limiting the ambient temperature (T_A) or supply voltage V_{DD}.

Note 3: Surge and ESD tolerances are tested with TVS protections on V_{DD} to GND and on S to GND. The maximum voltages are limited to ±85V by the TVS limit. A 200V tolerant transistor is connected between SNS, S, and G.

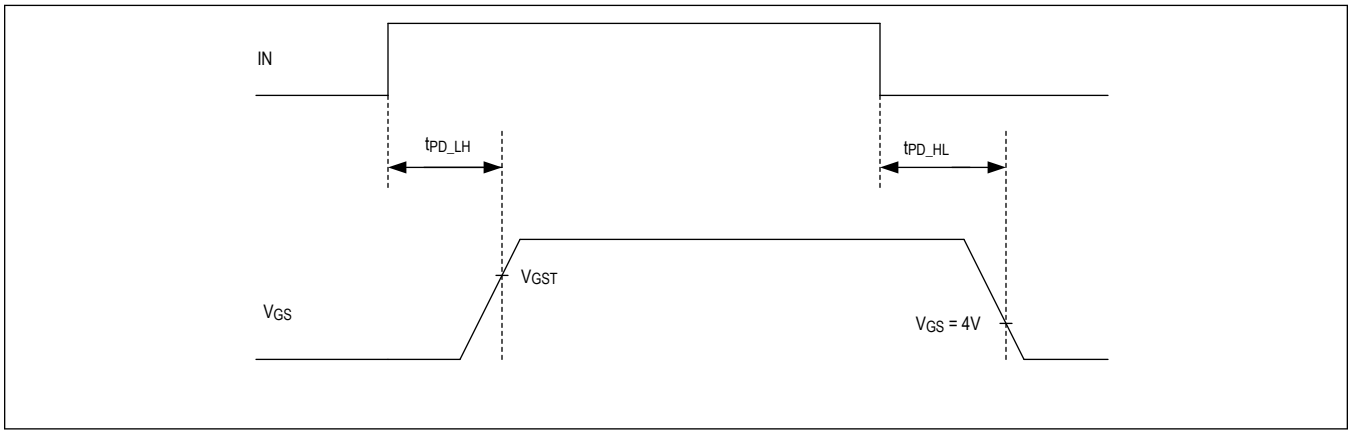
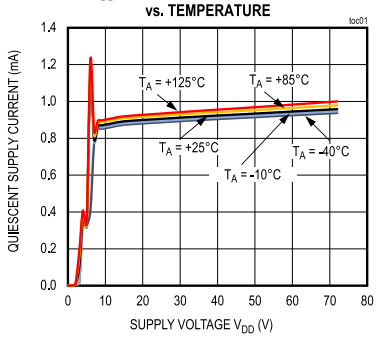


Figure 1. IN to G Propagation Times

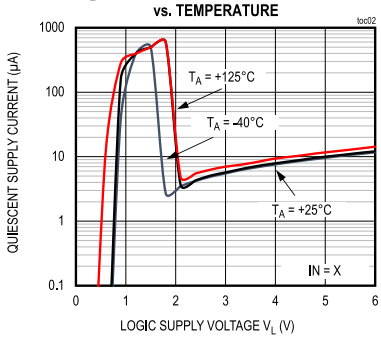
Typical Operating Characteristics

(V_{DD} = 24V, V_L = 5V, T_A = 25°C, unless otherwise noted.)

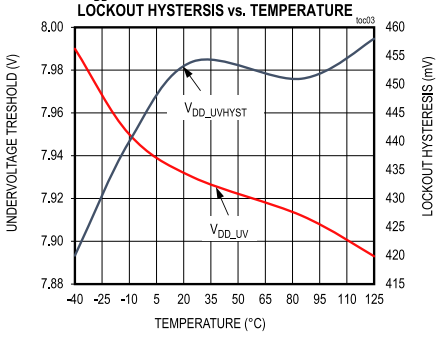
V_{DD} QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



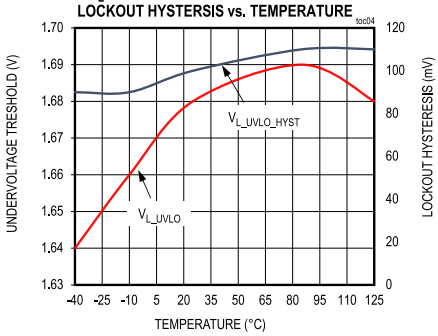
V_L LOGIC QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



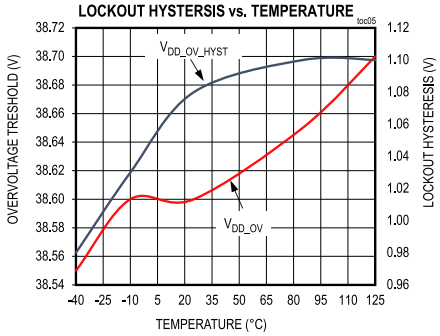
V_{DD} UNDERVOLTAGE THRESHOLD AND LOCKOUT HYSTERSIS vs. TEMPERATURE



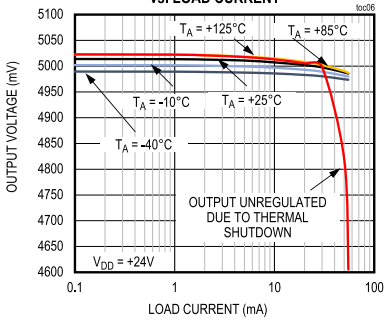
V_L UNDERVOLTAGE THRESHOLD AND LOCKOUT HYSTERSIS vs. TEMPERATURE



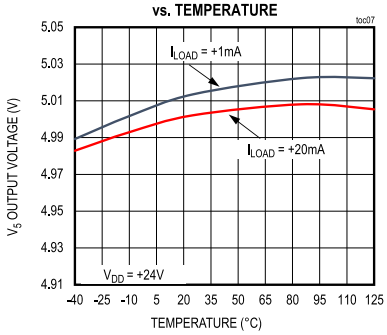
OVERVOLTAGE THRESHOLD AND LOCKOUT HYSTERSIS vs. TEMPERATURE



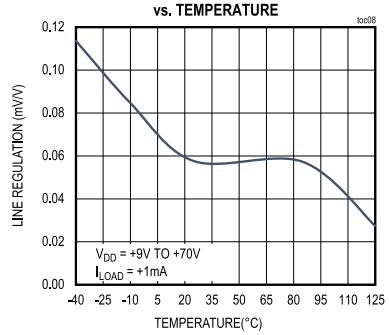
V_5 OUTPUT VOLTAGE vs. LOAD CURRENT



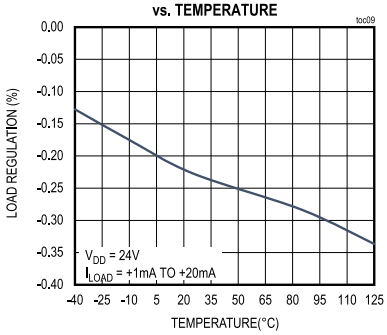
V_5 OUTPUT VOLTAGE vs. TEMPERATURE



V_5 LINE REGULATION vs. TEMPERATURE



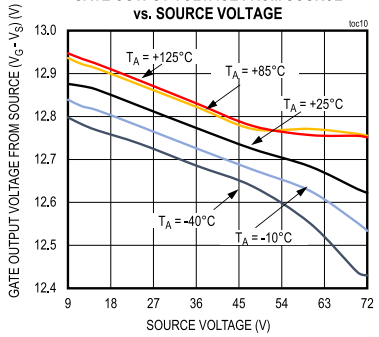
V_5 LOAD REGULATION vs. TEMPERATURE



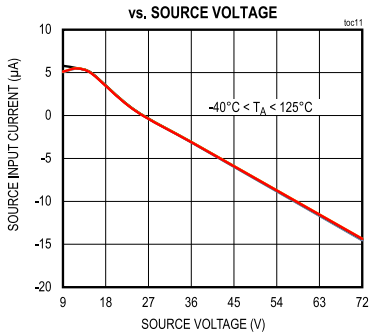
Typical Operating Characteristics (continued)

(V_{DD} = 24V, V_L = 5V, T_A = 25°C, unless otherwise noted.)

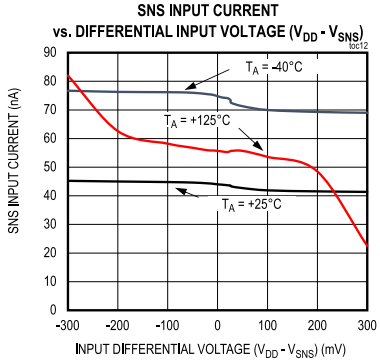
GATE OUTPUT VOLTAGE FROM SOURCE vs. SOURCE VOLTAGE



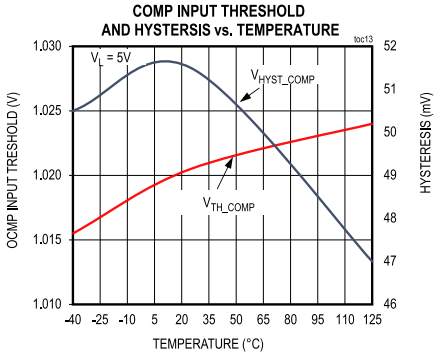
SOURCE INPUT CURRENT vs. SOURCE VOLTAGE



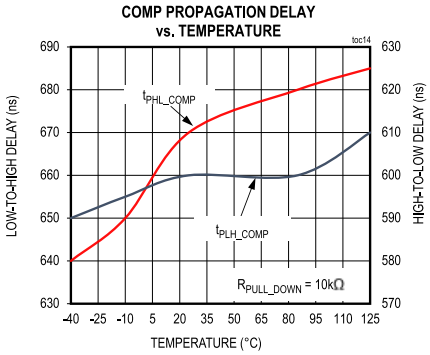
SNS INPUT CURRENT vs. DIFFERENTIAL INPUT VOLTAGE (V_{DD} - V_{SNS})



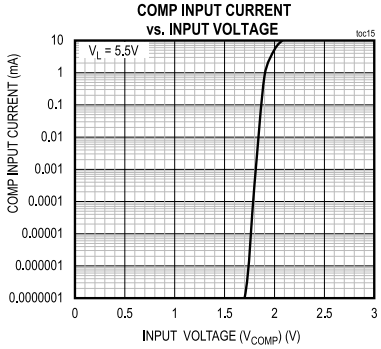
COMP INPUT THRESHOLD AND HYSTERSIS vs. TEMPERATURE



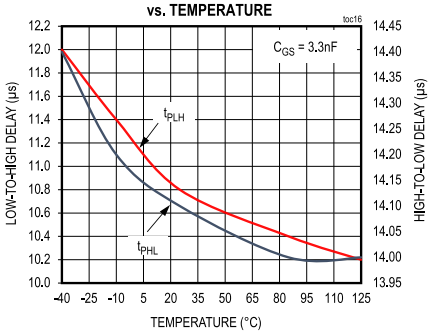
COMP PROPAGATION DELAY vs. TEMPERATURE



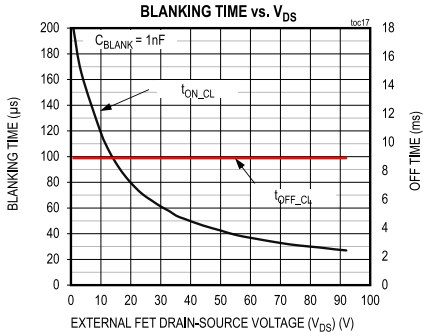
COMP INPUT CURRENT vs. INPUT VOLTAGE



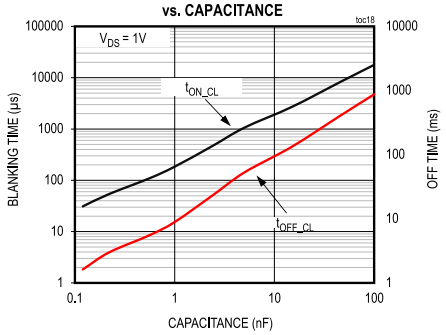
IN TO GATE PROPAGATION DELAY vs. TEMPERATURE



BLANKING TIME vs. V_{DS}



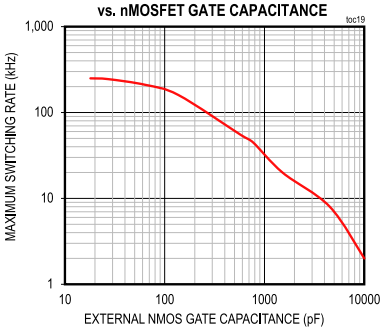
BLANKING TIME vs. CAPACITANCE



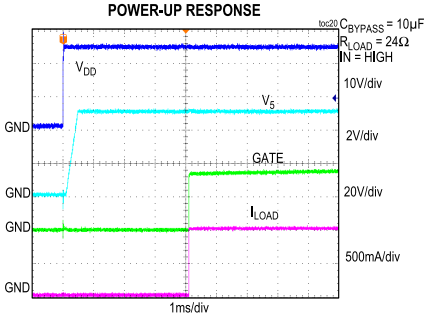
Typical Operating Characteristics (continued)

(V_{DD} = 24V, V_L = 5V, T_A = 25°C, unless otherwise noted.)

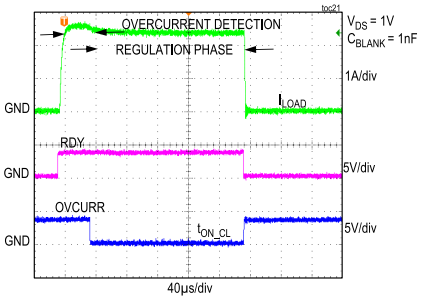
MAXIMUM SWITCHING RATE vs. nMOSFET GATE CAPACITANCE



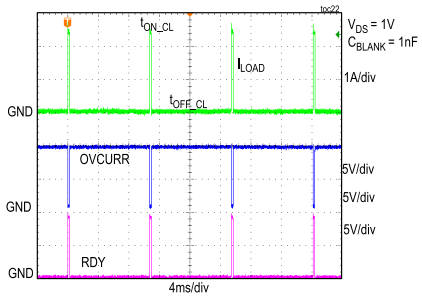
POWER-UP RESPONSE



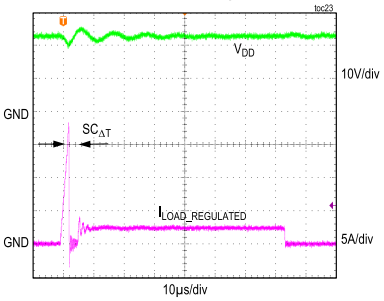
OVERCURRENT PROTECTION



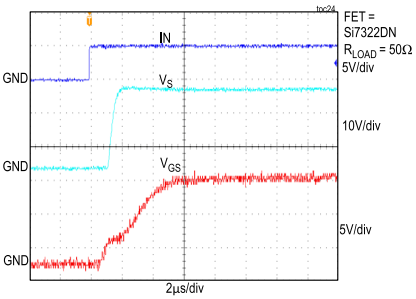
BLANKING TIME AND AUTO-RETRY



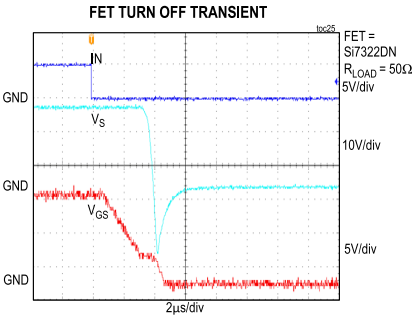
SHORT-CIRCUIT DETECTION AND INTERVENTION



FET TURN ON TRANSIENT

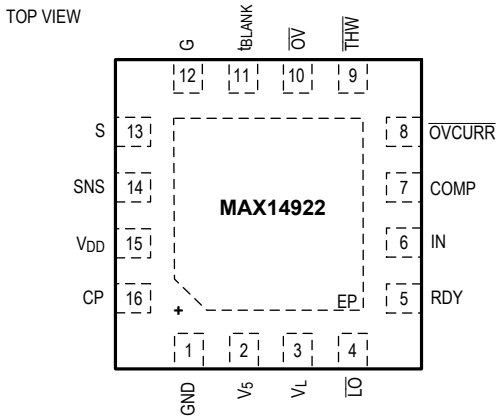


FET TURN OFF TRANSIENT



Pin Configuration

MAX14922



TQFN-EP
3mm x 3mm

Pin Description

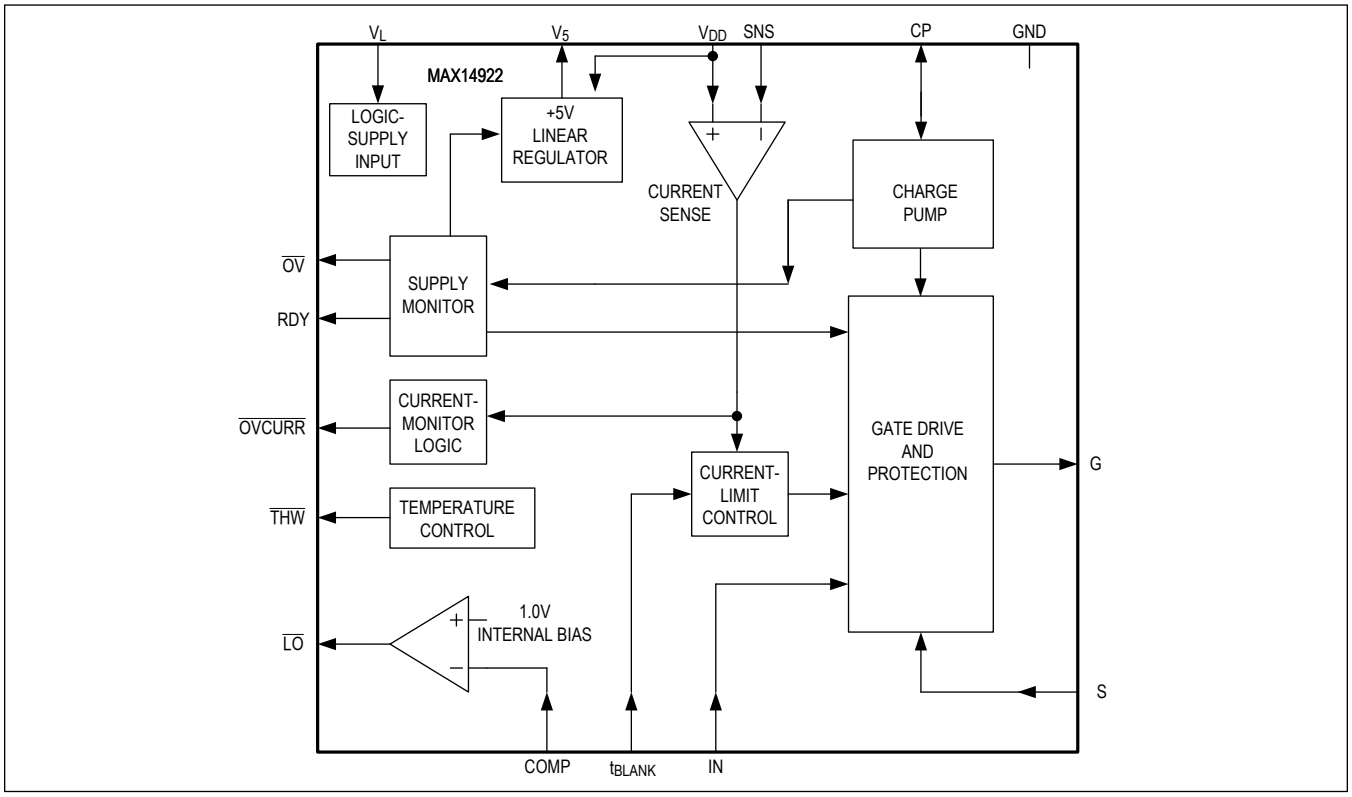
PIN	NAME	FUNCTION	TYPE
POWER SUPPLY			
1	GND	Ground	Ground/ Supply Return
2	V_5	Linear Regulator Output, 5V. Connect a 1µF bypass capacitor to GND.	Supply
3	V_L	Logic Supply Input. Connect supply between 2.5V and 5.5V to V_L. Connect a 100nF bypass capacitor to GND.	Supply
15	V_{DD}	Supply Voltage, Nominally 24V. Bypass V_{DD} to GND using a 10µF capacitor.	Supply
16	CP	Charge-Pump Tank Capacitor. Connect a 1µF/16V capacitor between CP and V_{DD}.	Supply
CURRENT SENSE			
14	SNS	Sense Input. Connect a current sense resistor between SNS and V_{DD} to define the maximum load current. Sense is a high-impedance analog voltage input.	HV Input
FET DRIVE			
12	G	Gate Drive Output. Connect to G to the gate of the nMOS power FET.	HV Output
13	S	Source Input. Connect to Source terminal of the nMOS power FET. This is a high-impedance input. Connect a 1nF capacitor to GND for improved EMC.	HV Input
CONTROL			
6	IN	Switch Control Input. Drive IN high to close the HS switch; drive IN low to open the HS switch.	Logic Input
7	COMP	Comparator Input. Generates the $\overline{LO}$ output	Analog Input
11	t_{BLANK}	Blanking Time Input. Connect a capacitor between t_{BLANK} and GND to set the overcurrent auto-retry blanking time. Connect t_{BLANK} to GND to disable auto-retry current limiting. See the Detailed Description section for details.	Analog Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
DIAGNOSTIC OUTPUTS			
4	$\overline{LO}$	Output Voltage Monitor, Push-Pull. $\overline{LO}$ is low when the COMP voltage is higher than the threshold voltage. $\overline{LO}$ is high when the COMP input voltage is lower than the threshold voltage.	Logic Output
5	RDY	Ready Open-Drain Logic Output. RDY turns output low when, for any reason, the output keeps the external FET off. Connect a pullup resistor, if used.	Logic Output
8	$\overline{OVCURR}$	Overcurrent Open-Drain Logic Output. $\overline{OVCURR}$ turns output low when the high-side switch is in current limit. If used, connect a pullup resistor to use $\overline{OVRCURR}$.	Logic Output
9	$\overline{THW}$	Thermal Warning Open-Drain Output. The output is asserted low when the temperature of the chip is higher than the thermal warning voltage. Connect an external pullup resistor if used.	Logic Output
10	$\overline{OV}$	Overvoltage Open-Drain Logic Output. The $\overline{OV}$ turns on output low when V_{DD} voltage rises above the $\overline{OV}$ threshold of 39V typ. Connect a pullup resistor, if used.	Logic Output
EXPOSED PAD			
—	EP	Exposed Pad. Connect exposed pad to GND.	Ground/ Supply Return

Functional Diagram

Functional Block Diagram



Detailed Description

The MAX14922 is a high-side n-channel FET controller for implementing a high-side switch that operates as an industrial digital output. The MAX14922 is specified for operation with supplies up to 70V. The controller features accurate, active current limiting with current defined by the R_S sense resistor connected between the V_{DD} and SNS inputs.

The device is used with an external low R_{ON} FET, which acts as a load switch to industrial loads. High inductive clamping voltages can be achieved by connecting an external ground-connected TVS diode to the MAX14922 S input. The device features diagnostics such as load or supply-voltage monitoring, gate output ready, high voltage-supply indication, current limiting, current limit auto-retry timing, and overcurrent indication.

The MAX14922 features an internal 5V LDO supply output (V_5) capable of delivering up to 50mA of output current.

Logic Interface

The logic interface requires a V_L supply in the range of 2.5V to 5.5V. This ensures that the logic levels on all logic I/O pins are CMOS compliant. If used, connect pullup resistors to the open-drain logic outputs. If not used, connect the open-drain logic outputs to GND.

5V Linear Regulator

The integrated 5V linear regulator (V_5) can supply up to 50mA load current. Note that linear regulators have high power dissipation when powered from high supply voltage. Calculate the power dissipation in the regulator as $P_{DIS}(W) = (V_{DD} - V_5) \times I_{V5}$. The power dissipation might be excessive for high load currents in combination with high supply voltage resulting in self heating of the device. Verify that the MAX14922 maximum thermal ratings are not exceeded at the highest operating temperatures.

When the MAX14922 enters thermal shutdown, the V_5 linear regulator is automatically turned off. The regulator turns on automatically when the chip temperature drops by 10°C (typ).

Inductive Loads

When the load current flowing into an inductive load is abruptly stopped when the external FET is turned off, the inductance tries to draw current, which results in a high kick-back voltage. This kick-back voltage, seen on the source of the FET, needs to be limited/clamped to a voltage in the range of the *Absolute Maximum Ratings*, to protect the MAX14922 S input from negative voltages.

Due to the S input maximum rating of -70V, a ground-connected TVS diode can be used for inductive energy clamping and absorption. Using a ground-connected TVS diode provides the additional advantage that the clamping voltage is independent of the V_{DD} supply input voltage, and provides a means for low-power dissipation for inductive clamping by providing a fast demagnetization event. Ensure that the TVS diode can dissipate the heat during worst-case inductive load clamping at the highest ambient operating temperature.

Diagnostic Features

MAX14922 integrated diagnostic features enable monitoring and control of vital parameters in the application. In case of load faults, damaged FET, short-circuit conditions, and unwanted high ambient temperature, the device features logic outputs that alert the controller to force an appropriate response to ensure safety and reliability of the application. In cases when the diagnostic outputs are not required, the outputs can either be left unconnected or connected to ground.

Output or Supply Voltage Monitor

The integrated comparator input COMP allows monitoring of any voltage in the system, for example the V_{DD} supply voltage or the source voltage of the external FET. The internal comparator, compares the COMP input voltage with a 1V (typ) internal reference. The inverse logic is presented on the $\overline{LO}$ logic output. Connect a resistive voltage-divider between the S or V_{DD} input to set the threshold voltage.

Output Ready

RDY is an open drain output that signals normal device operation when RDY is pulled passively high by a pullup resistor. The device is not ready for normal operation when the MAX14922 actively drives RDY low, signalling an application issue, regardless of the IN input logic state.

The following conditions drives RDY low:

1. Undervoltage of any of the power supplies (V_{DD}, V_5, and V_L).
2. When the device is in overcurrent for a time longer than the blanking time, i.e, a FET overload condition.
3. Thermal shutdown.
4. Charge pump overload: if the external FET is switched on/off at a high frequency, the voltage generated by the charge pump drops due to a high load current. In this case the output FET is forced OFF to reduced the charge pump current load, the external FET is re-enabled when the charge pump voltage is higher than 9V.

High Supply Indication (OV)

When the V_{DD} supply voltage rises beyond the $\overline{OV}$ threshold (approximately +39V), the $\overline{OV}$ output goes active low. When the $\overline{OV}$ is low, the MAX14922 continues to operate normally as the device operates with V_{DD} supply voltages of up to 70V. $\overline{OV}$ output can indicate that the supply is higher than the system is designed for. $\overline{OV}$ output can be used to turn the FET off by driving IN low. The external nMOS transistor is not turned off, remains ON even when $\overline{OV}$ is low. An external control signal or a controller can turn off the FET by forcing IN low during an overvoltage condition, or an external and gate can be used for high supply shut-off operation.

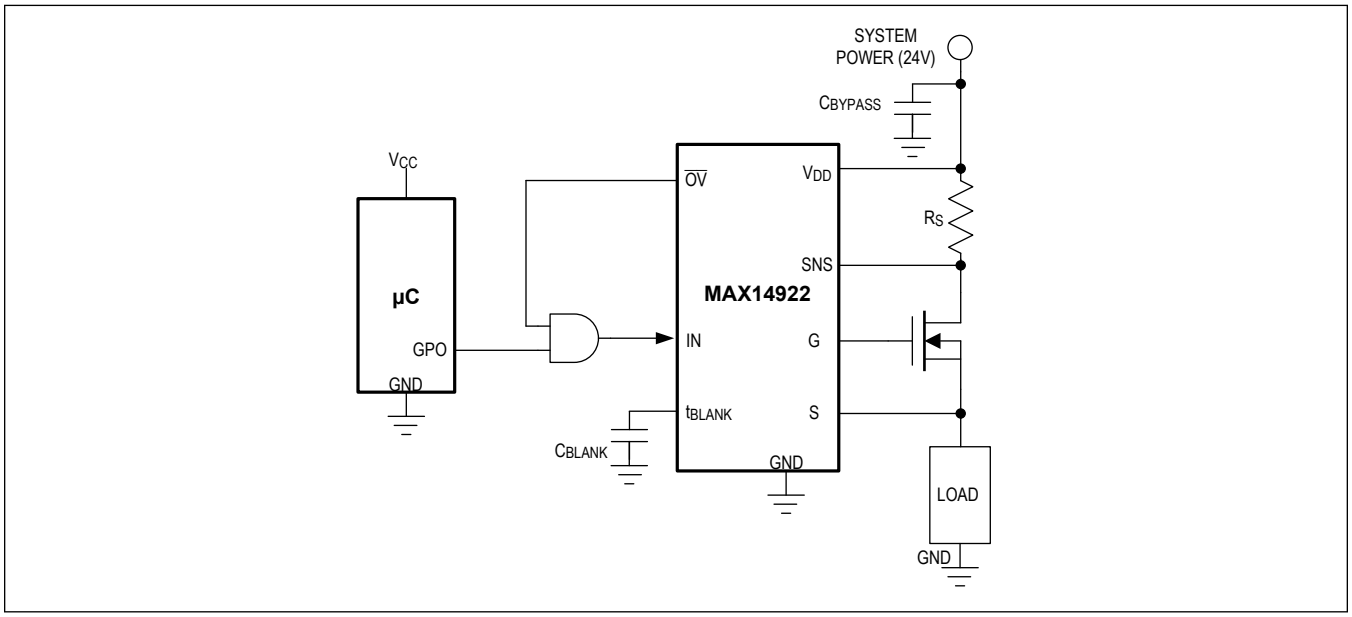


Figure 2. High Supply Shut-off Application

Overcurrent Monitor

The open drain $\overline{OVCURR}$ output transitions low when the load current exceeds the current limit set by the sense resistor (R_S).

Current Limiting

Connect a sense resistor (R_S) between V_{DD} and SNS inputs to set the maximum current allowed in the application. The current limit is calculated as $I_{CL} = \frac{V_{CL}}{R_S}$. Consider the variation of I_{CL} due to the tolerance of V_{CL} and R_S. When the load current exceeds the current limit, then the device actively regulates the nFET gate-source voltage to control the load

current.

Current Limit Auto-Retry Timing

During an overcurrent condition, the MAX14922 actively regulates the current during the blanking time set by the capacitor value on the t_{BLANK} input. If the load draws overcurrent for a period longer than the blanking time, the device turns the external FET off for protection purposes. After an Off-delay equal to about 50x the blanking time, the nFET is automatically turned on again. Auto-retry On/Off cycling continues until the cause for overcurrent is removed by the user. The $\overline{OVCURR}$ logic output goes low after the detection of the overcurrent, and remains low until the overcurrent condition is removed. At the end of the blanking time, the RDY output is also asserted low to indicate that the external nFET is forced off.

During an overcurrent event, internal control logic monitors and reduces the gate voltage so that the V_{GS} is reduced. Refer to TOC21 and TOC22 in the *Typical Operating Characteristics* section for information on overcurrent detection (blanking time and auto-retry).

The blanking time can be defined by the capacitor between the t_{BLANK} input and GND. Select a capacitor value such that the blanking time to the OFF-time duty cycle does not exceed the nMOS power transistor safe operating area (SOA) under worst-case supply voltage, temperature, load current, and output short-circuit conditions. The MAX14922 automatically reduces the blanking time duration, proportionally to the nFET V_{DS} (the higher the V_{DS}, the shorter the blanking time), according to the following formula:

$$t_{ON\_CL}(\mu s) = \frac{2000 \times C_{BLANK}(nF)}{\left(10 + 0.9V_{DS}\right)}$$

Refer to TOC17 and TOC18 for blanking-time dependence on V_{DS} (V) and C_{BLANK} (nF) capacitance in the *Typical Operating Characteristics* section.

Auto-retry cycling can be disabled by shorting t_{BLANK} to GND. In this case, the RDY output does not toggle low. A controller needs to turn off the nFET and manage the overload condition in order to protect the nFET from damage.

Short-Circuit Protection

A short-circuit applied at the load output would result in a high short-circuit current mainly limited by the FET R_{ON}. When the MAX14922 detects an excessively high transient load current, it turns the FET off for about 5µs and then turns the FET back on at a controlled rate so that the short-circuit load current is then determined by the sense resistor value. Refer to TOC23 in the *Typical Operating Characteristics* section for short-circuit detection and intervention response for the MAX14922.

Thermal Warning and Shutdown

The MAX14922 features integrated temperature monitoring and a protective shutdown feature. The device integrated temperature sensor signals thermal warning at 110ºC (typical). During thermal warning the $\overline{THW}$ logic output goes low indicating an overtemperature warning event. During a thermal warning event, the device is still in normal operation. When the temperature cools down by 10ºC, the $\overline{THW}$ logic output goes back high.

When the device temperature rises above 150ºC, MAX14922 enters shutdown mode. Regardless of the state of the IN input, the Gate output is turned off forcing the external FET to turn off. The internal LDO generating 5V output is turned off as well. As the temperature reduces by 10ºC, the device returns to normal operation with the $\overline{THW}$ output low, and the V_5 regulator output on at 5V.

Maximum Switching Frequency

The maximum switching FET frequency is determined by the time and ability of the internal charge pump to charge and discharge the external power FET gate capacitance. The charge pump delivers 2.5mA (typ) turn-on and turn-off currents allowing drive of low R_{ON} MOSFETs. FET parts specify their gate charge under a typical ON condition. As reference, the maximum switching frequency that the MAX14922 can switch the Si7322DN having 13nC (typ) specified total gate charge is 45kHz. Similarly, the low R_{ON} SiR622DP with 27nC (typ) specified total gate charge can be switched with 20kHz. The RDY output can be used to check if the charge pump is able to drive a FET at higher frequencies. Refer

to TOC19 in the Typical Operating Characteristics section for the maximum switching rate vs. gate capacitance of the external FET.

Applications Information

Selecting the Power nFET Transistor

The following lists the criteria for selecting a suitable FET for an application.

- The FET current capability must be higher than the maximum required load current.
- R_{ON} should be low enough for power dissipation considerations during maximum load current.
- The external FET drain-source breakdown voltage (V_{BR}) or (V_{DSS}) should be larger than the TVS clamp voltage plus the max supply V_{DD}.
- The FET thermal package impedance must be low enough to dissipate the worst-case transient power dissipation, which usually is a short circuit to GND or a negative voltage. Use the FET SOA curves in conjunction with blanking time as a reference.
- The total gate charge should be less than 40nC.
- The gate-source threshold voltage should be > 0.8V.
- The maximum allowable gate voltage should be greater than 16V.

Examples of 100V FETs with MAX14922 are: Si7322, IPD60N10, PSMN021-100, Si4190, and STD100N10.

Transient EMC Protection

The MAX14922 does not have protection against Surge (IEC 6100-4-5) and high levels of ESD (IEC 61000-4-2). A TVS diode needs to be connected between the S input and GND to protect against such negative Surge and negative ESD. The same TVS diode also clamps the inductive energy during load turn-off.

The transient currents caused by positive surge and/or ESD voltages applied to OUT flows through the parasitic nMOS source-drain body diode and the sense resistor into the V_{DD} supply and/or clamping V_{DD} TVS diode, standard nMOS power transistors, and sense resistors can tolerate the power dissipated in them during standard industrial-level transient currents of ±2kV/42Ω surge and ±9kV contact ESD.

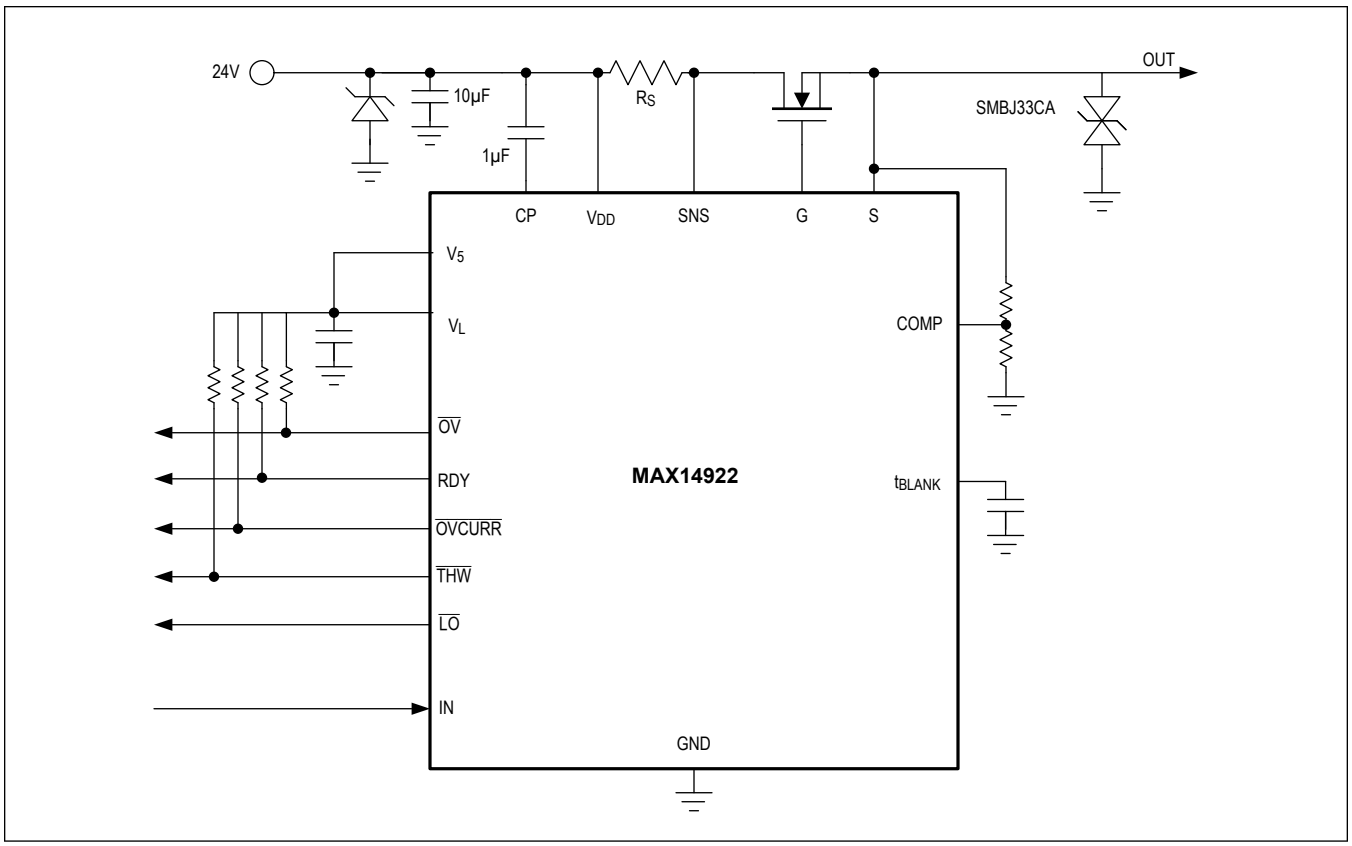


Figure 3. Transient EMC Protection Scheme

Inductive Clamping

Select a TVS power and size that can safely dissipate the energy in the inductive load during load turn-off and demagnetization under worst-case conditions. The worst case is the highest temperature operating conditions in the module enclosure with the highest load current and inductance.

Operation with High Supply Voltages

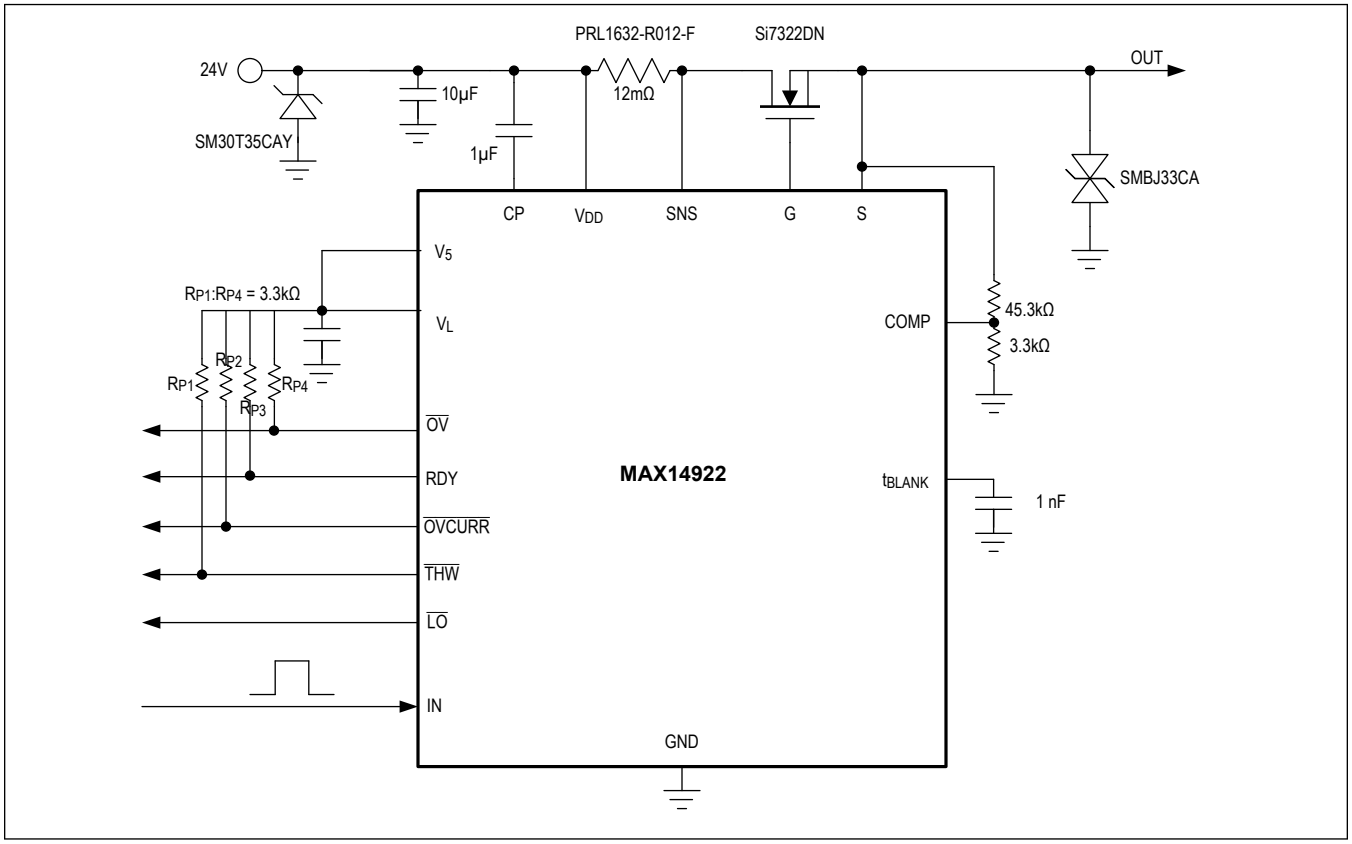
If the maximum V_{DD} operating supply voltage is expected to be higher than the bipolar TVS working voltage, then a silicon diode should be put in series with the TVS. This is shown in the 2A / 60V Applications Diagram in the *Typical Application Circuit*.

Typical Application Circuits

2A / 24V Application Circuit

The following circuit illustrates a circuit for realizing a 2A high-side switch with 24V nominal, 33V maximum supply voltage and 33V inductive load clamping voltage. The high-side switch R_{ON} is (48mΩ + 12mΩ) = 60mΩ. A Zener diode, SM30T35CAY, clamps the supply at 48V in case of supply overvoltage or excursions.

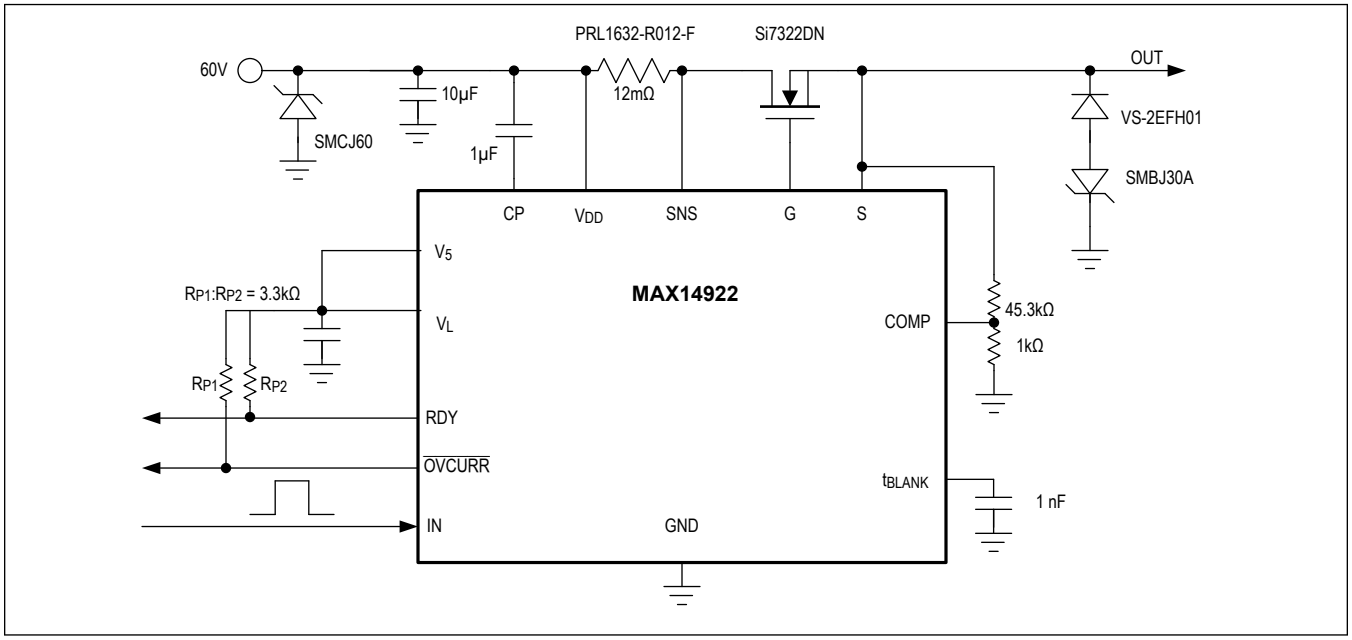
Typical Application Circuits (continued)



2A / 60V Application Circuit

The following circuit illustrates a circuit for realizing a 2A load current, 60V maximum supply high-side switch with 30V inductive load clamping voltage. The high-side switch R_{ON} is (48mΩ + 12mΩ) = 60mΩ. In case of supply overvoltage or overshoot, the SMCJ60 TVS clamps the energy.

Typical Application Circuits (continued)



Ordering Information

PART NUMBER	TEMP. RANGE	PIN PACKAGE	TOP-MARKING
MAX14922ATE+	-40°C to +125°C	16 TQFN-EP*	APB
MAX14922ATE+T	-40°C to +125°C	16 TQFN-EP*	APB

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/20	Initial release	—