littleBits

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1.0.0 Required Engineering Deliverables

1.0.1 Product Requirements Document (PRD) conforming to LB standards as described in this document. Template PRDs are provided by LB (**HDK-hardware-dev-manual/Design/Templates for PRD**).

1.0.2 Schematic Diagram (SCH) conforming to LB standards as described in this document. Template SCHs are provided by LB in the **HDK-eagle-templates-libraries/Eagle Templates for SCH and BRD** folder of the HDK.

1.0.3 PCB Layout (PCB) conforming to LB standards as described in this document. Template PCBs are provided by LB in the **HDK-eagle-templates-libraries/Eagle Templates for SCH and BRD** folder of the HDK.

2.0.0 Design Requirements

2.0.1 System Parameters:

VCC = 5VDC

BitSnap connector max current = 1A

Nominal temperature range = 10C to 40C

2.0.2 Female bitSnap connector pinout:

Pin 1: GND (ground, 0VDC)

Pin 2: SIG (signal, 0 to 5 V continuous)

Pin 3: VCC (power, 5VDC)

2.0.3 Male bitSnap connector pinout:

Pin 1: VCC (power, 5VDC)

Pin 2: SIG (signal, 0 to 5 V continuous)

Pin 3: GND (ground, 0VDC)

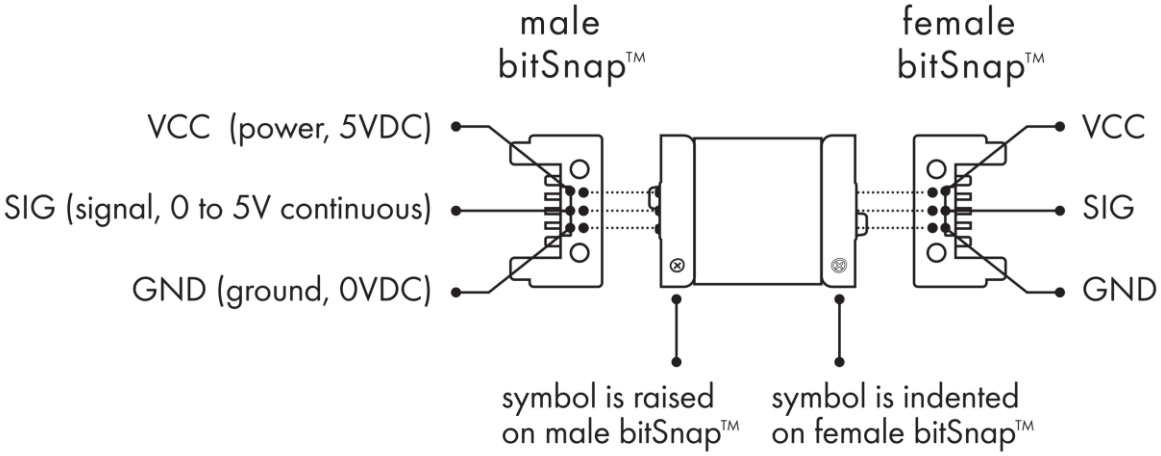

Figure 1: Male and female bitSnap™ connector pinouts

2.0.4 All inputs must be high impedance. The preferred input impedance must be equal to or greater than 1 MΩ (megOhm).

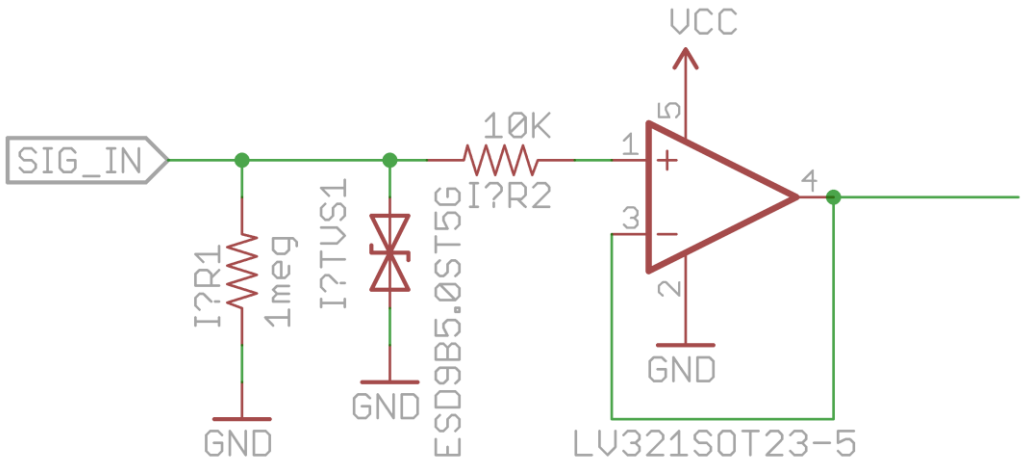

Figure 2: Example of an input stage, included in the Eagle templates

2.0.5 All outputs must be low impedance, with symmetric drive characteristics (yields same performance when either sinking or sourcing current.) The output impedance must be less than 100 ohms.

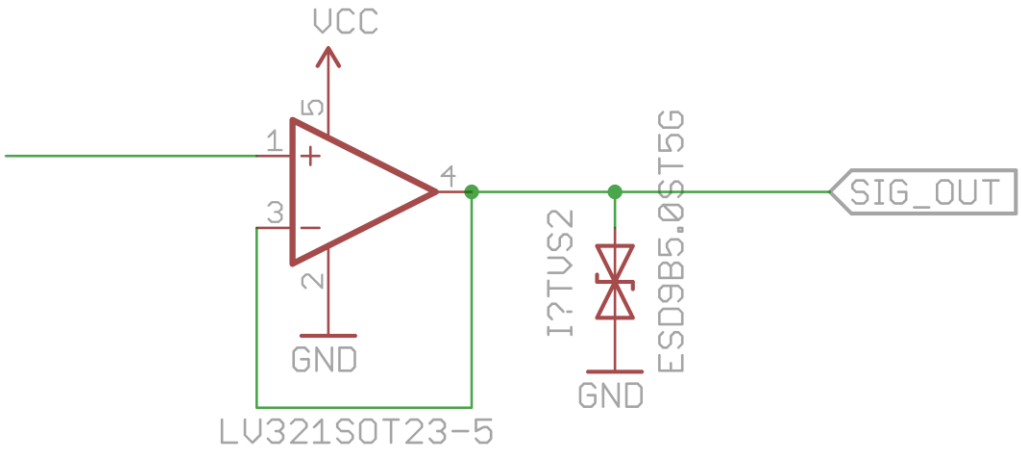

Figure 3: Example of an output stage, included in the Eagle templates

2.0.6 All ICs must have at least one 0.1 uF bypass capacitor on every IC power supply.

2.0.7 There must be a series ferrite bead between all circuitry and bitSnap Vcc connections (see Figure 4).

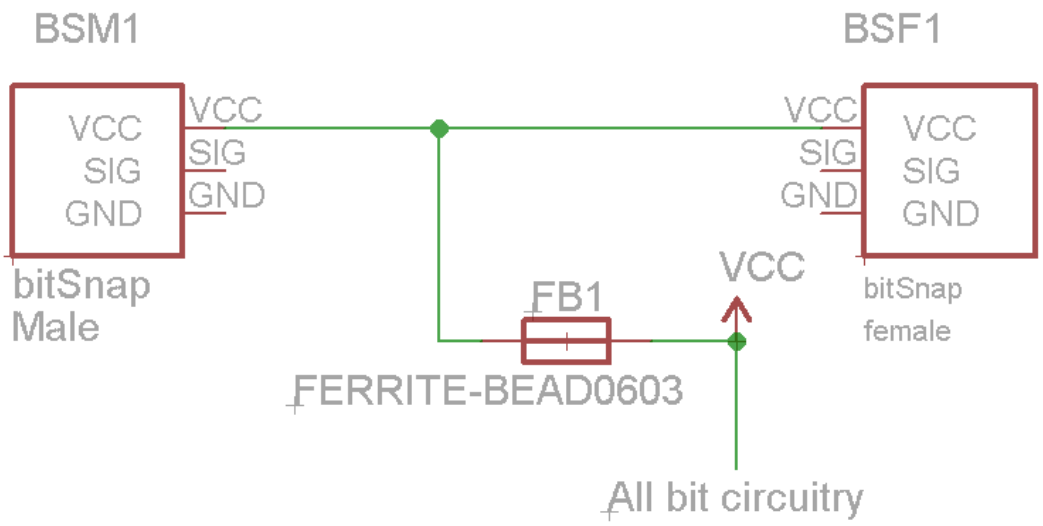

Figure 4: Required topology of Vcc connection

2.0.8 Inputs: Every bitSnap input must have a series 10K current limiting resistor on the SIG line (see Figure 2).

2.0.9 Inputs: Every bitSnap input must have a shunt TVS diode, or equivalent ESD countermeasures (see Figure 2).

2.0.10 Inputs: Floating bitSnap inputs are **not** permitted.

2.0.11 Preferred Parts. littleBits recommends the use of specific part numbers for typical functions such as opamps, switches, potentiometers, and others. A list of these preferred parts can be found in HDK-eagle-templates-libraries/libraries/lbPreferredParts.xlsx. SMD components are preferred over through-hole and the 0603 footprint is preferred for passive components.

3.0.0 Preparations

3.0.1 Download and install the following from the HDK-eagle-templates-libraries repository

Parts Libraries:

libraries/LITTLEBITS140915.lbr

Design Rules Files:

libraries/littleBitsDRC_140813.dru //for 2-layer boards

libraries/littleBits4-LAYERDRC_140813.dru //for 4-layer boards

4.0.0 Product Design Requirement (PRD)

4.0.1 The PRD should be created by the developer from the template provided by LB. The template is available in Design/Templates for PRD/prd_template.xls. A copy of the template will be provided by LB in the module repo if the project is accepted.

5.0.0 Schematic (SCH)

5.0.1 The schematic should be based on one of the SCH templates provided by LB, found in **Design/Eagle Templates for SCH and BRD**.

5.0.2 Schematic grid must be set to 0.1 inch.

6.0.0 Printed Circuit Board (PCB)

6.0.1 Set the PCB layout primary grid to 0.05mm. Set the alternate grid to 0.01mm.

6.1.0 **Component Choice and Placement**

6.1.1 bitSnap connectors must not be moved from their original positions in the templates.

6.2.0 **Design Rule Check**

6.2.1 Board layouts must be verified using the littleBits DRC file provided.

6.2.2 The DRC file must be run with only layers 1 to 20 turned on.

6.2.3 Width error of revision number copper text can be ignored.