8/16-Port IEEE 802.3at PoE PSE Controller with Power Management and LED Control

FEATURES

- **Fully Compliant IEEE 802.3at (Type 2) PSE**
- **Up to 16 PSE Ports**
- **Fully Autonomous System-Level Power Manager**
  - **No Host Processor Required**
- **System-Level PoE LED Controller**
  - **Per-Port Status and Fault LEDs**
  - **Supply Overload LED with Hysteresis**
- eFlash-Programmable System Settings
  - Port- and System-Level Power Thresholds
  - LED Mapping and Blink Rate
  - Port Power Priority
- ECC-Protected eFlash and Data RAMs
- Very High Reliability Multipoint PD Detection
- Lowest Per-Port Power Path Dissipation
  - 100mΩ Sense Resistance
  - 57mΩ or Lower MOSFET $R_{DS(ON)}$
- Chipset Isolation Eliminates Isolated 3.3V Supply
- Available in a 64-Lead 7mm × 11mm (LTC9103) and 24-Lead 4mm × 4mm (LTC9101-3) QFN Packages

APPLICATIONS

- Small Business PoE PSE Switches/Routers

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DESCRIPTION

The LTC®9101-3/LTC9103 chipset is a 8/16-port power sourcing equipment (PSE) controller and power manager designed for use in IEEE 802.3at compliant Power over Ethernet (PoE) systems. The LTC9101-3 manages a user-defined system-level power budget across all ports. Port power is automatically assigned based on system power availability, initial physical classification and after power up, port dynamic power consumption.

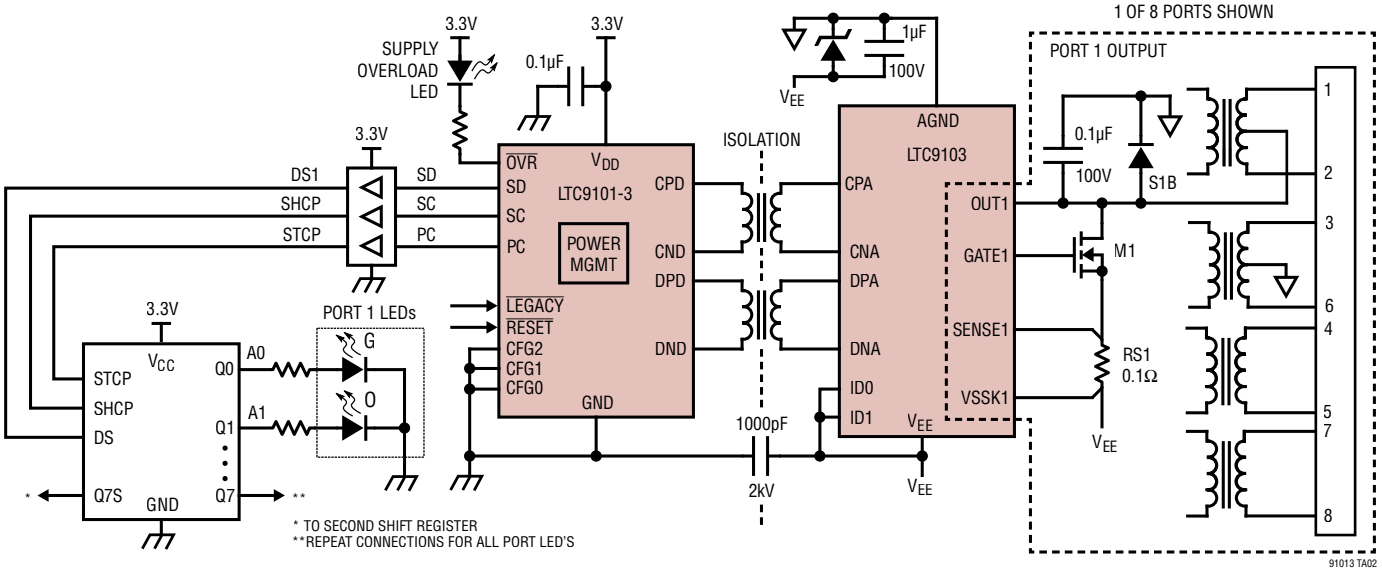
The LTC9101-3 prioritizes port power by port number (port 1 is highest priority) and automatically removes power from lower priority ports to accommodate higher priority ports.

The LTC9101-3 features an interface to control an external serial LED driver. LED indications include Port On, Port Off, Port Power Denied, and Port Fault states. A Supply Overload LED indicates system power usage is near power limit or a port is being denied power.

The LTC9101-3 operates without a host present. Configuration is accomplished by pin settings and I^2C-based flash programming.

The LTC9101-3 autonomously performs compliant 802.3at detection, classification power up, power on, and fault management.

TYPICAL APPLICATION



Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 4)

LTC9103

Supply Voltages (with respect to V_{EE})
- AGND ..... –0.3V to 80V
- PWRIN ..... –0.3V to 80V
- CAP3, CAP4 ..... –0.3V to 5V
- VSSKn ..... –0.3V to 0.3V

Analog Pins
- SENSEn, OUTn ..... –20V to 80V
- GATEn, IDn, PWRMDn ..... –0.3V to 80V
- CPA, CNA, DPA, DNA ..... –0.3V to CAP3 + 0.3V
- EXT3 ..... –0.3V to 30V

Operating Ambient Temperature ..... –40°C to 85°C
Operating Junction Temperature (Note 2) ... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C

(Note 1)

LTC9101-3

Supply Voltages (with respect to DGND)
- V_{DD} ..... –0.3V to 3.6V
- CAP1, CAP2 ..... –0.3V to 1.32V

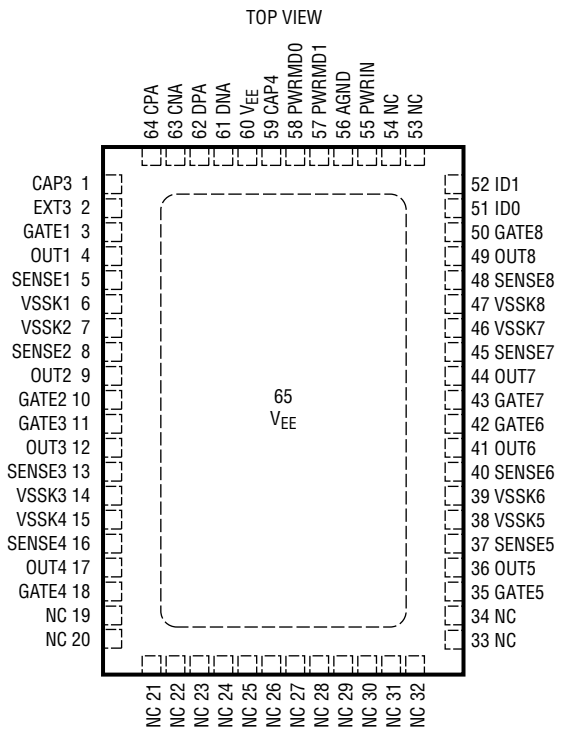
Digital Pins
$\overline{\text{LEGACY}}$, $\overline{\text{OVR}}$, CFGn, SDAIN, SDAOUT, SCL, $\overline{\text{RESET}}$, SC, SD, PC ..... –0.3V to V_{DD} + 0.3V

Analog Pins
- CPD, CND, DPD, DND ..... –0.3V to V_{DD} + 0.3V

Operating Ambient Temperature ..... –40°C to 85°C
Operating Junction Temperature (Note 2) ... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C

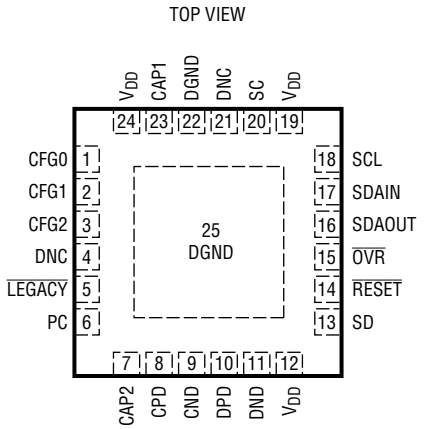
PIN CONFIGURATION

LTC9103



UKJ PACKAGE
64-LEAD (7mm × 11mm) PLASTIC QFN
θ_{JC} = 1°C/W, θ_{JA} = 22°C/W
EXPOSED PAD (PIN 65) IS V_{EE}, MUST BE SOLDERED TO PCB

LTC9101-3



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
θ_{JC} = 4°C/W, θ_{JA} = 47°C/W
EXPOSED PAD (PIN 25) IS DGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC9101AUF-3#PBF	LTC9101AUF-3#TRPBF	91013	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC9103AUKJ#PBF	LTC9103AUKJ#TRPBF	LTC9103	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Main PoE Supply Voltage	AGND – V_{EE}	●	51		57	V
	LTC9103 Undervoltage Lock-Out	AGND – V_{EE}	●		8.2	9	V
V_{DD}	V_{DD} Supply Voltage	V_{DD} – DGND	●	3.0	3.3	3.6	V
	Undervoltage Lock-Out				2.8		V
	V_{DD} Slew Rate, Falling	2.4 ≤ V_{DD} – DGND ≤ 3.0 (Note 7)				20.0	mV/µs
V_{CAP1}, V_{CAP2}	Internal Regulator Supply Voltage	V_{CAP1} – DGND, V_{CAP2} – DGND (Note 12)			1.2		V
V_{CAP3}	Internal 3.3V Regulator Supply Voltage	CAP3 – V_{EE} (Note 12)	●	3	3.3	3.6	V
$t_{CAP3EXT}$	CAP3 External Supply Rise Time	0.5V < CAP3 < CAP3(min), EXT3 tied to CAP3 (Note 7)	●			1	ms
V_{CAP4}	Internal 4.3V Regulator Supply Voltage	C_{AP4} – V_{EE} (Note 12)			4.3		V
I_{EE}	V_{EE} Supply Current	PWRIN Pin Connected to AGND, EXT3 LOW, All Gates Fully Enhanced		7.7	11	14	mA
	3.3V Rail Supply Current	From CAP3 = 3.3V (EXT3 HIGH)		4.2	5.4	6.6	mA
I_{DD}	V_{DD} Supply Current	(V_{DD} – DGND) = 3.3V	●		40	60	mA
Detection							
	Forced Current	Load Resistance 15.5K to 32K	● ●	220 143	240 160	260 180	µA µA
	Forced Voltage	Load Resistance 18.5K to 27.5K	● ●	7 3	8 4	9 5	V V
	Detection Current Compliance	AGND – OUTn = 0V	●		0.8	0.9	mA
V_{OC}	Detection Voltage Compliance	AGND – OUTn, Open Port	●		10.4	12	V
	Detection Voltage Slew Rate	AGND – OUTn, C_{PORT} = 150nF (Note 7)	●			0.01	V/µs
	Min. Valid Signature Resistance		●	15.5	17	18.5	kΩ
	Max. Valid Signature Resistance		●	27.5	29.7	32	kΩ
Classification							
V_{CLASS}	Classification Voltage	AGND – OUTn, SENSEn – VSSKn < 5mV	●	16		20.5	V
	Classification Current Compliance	SENSEn – VSSKn, OUTn = AGND (Note 14)	●	7	8	9	V
	Classification Threshold	SENSEn – VSSKn (Note 13) Class Signature 0 – 1 Class Signature 1 – 2 Class Signature 2 – 3 Class Signature 3 – 4 Class Signature 4 – Overcurrent	 ● ● ● ● ●	 0.5 1.3 2.1 3.1 4.5	 0.65 1.45 2.3 3.3 4.8	 0.8 1.6 2.5 3.5 5.1	 mV mV mV mV mV
V_{MARK}	Classification Mark State Voltage	AGND – OUTn, SENSEn – VSSKn < 5mV	●	7.5	9	10	V
	Mark State Current Compliance	OUTn = AGND	●	7	8	9	mV
Gate Driver							
	GATE Pin Pull-Down Current	Port Off, GATEn = V_{EE} + 5V			1		mA
	GATE Pin Fast Pull-Down Curre	GATEn = V_{EE} + 5V			65		mA
	GATE Pin On Voltage	GATEn – V_{EE}, I_{GATEn} = 1µA	●	11		14	V
Output Voltage Sense							
V_{PG}	Power Good Threshold Voltage	OUTn – V_{EE}	●	2	2.4	2.8	V
	OUT Pin Pull-Up Resistance to AGN	Port On Port Off	 ●	 300	2500 500	 700	kΩ kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense							
V_{LIM}	Active Current Limit	OUTn – VEE < 10V Class 0 – Class 3 Class 4		 40 80	 42.5 85	 45 90	 mV mV
V_{INRUSH}	Active Current Limit, Inrush	OUTn – V_{EE} < 30V (Note 14)		40	42.5	45	mV
V_{HOLD}	DC Disconnect Sense Voltage	SENSEn – VSSK	●	500	700	900	µV
V_{SC}	Short-Circuit Sense	SENSEn – VSSKn – V_{LIM}			60		mV
Digital Interface							
V_{ILD}	Digital Input Low Voltage	$\overline{LEGACY}$, $\overline{RESET}$, CFGn (Note 6)	●			0.8	V
	I^2C Input Low Voltage	SCL, SDAIN (Note 6)	●			1.0	V
V_{IHD}	Digital Input High Voltage	(Note 6)	●	2.2			V
	Digital Output Low Voltage	I_{SDAOUT} = 3mA, $I_{\overline{OVR}}$ = 3mA I_{SDAOUT} = 5mA, $I_{\overline{OVR}}$ = 5mA	● ●			0.4 0.7	V V
	LED Driver Output Pull-Up to V_{DD}	SC, SD, PC	●	46	50	58	kΩ
	LED Driver Output Pull-Down to DGND	SC, SD, PC	●	46	50	58	kΩ
	LED Shift Driver Clock Frequency	(Note 7)			40		kHz
	Parallel Capture Clock Frequency	(Note 7)			526		Hz
t_{PC_CLK}	Parallel Capture Clock Period	(Note 7)			1.9		ms
	Internal Pull-Up to V_{DD}	$\overline{LEGACY}$, $\overline{RESET}$, CFG2			50		kΩ
	Internal Pull-Down to DGND	CFG0			50		kΩ
	EXT3 Pull-Down to V_{EE}				50		kΩ
	IDn Internal Pull-Up to CAP4	V(IDn) = 0V			5		µA
PSE Timing Characteristics (Note 7)							
t_{DET}	Detection Time	Beginning to End of Detection	●		380	500	ms
t_{CEV}	Class Event Duration		●	6	15	20	ms
t_{CEVON}	Class Event Turn On Duration	C_{PORT} = 0.6µF	●			0.1	ms
t_{CLASS}	Class Event I_{CLASS} Measurement Timing		●	6			ms
t_{ME1}	Mark Event Duration (Except Last Mark Event)	(Note 10)	●	6	9.6	12	ms
t_{ME2}	Last Mark Event Duration	(Note 10)	●	6	20		ms
t_{PON}	Power On Delay	From End of Valid Detect to End of Valid Inrush	●			400	ms
t_{ED}	Fault Delay	From Power On Fault to Next Detect	●	2.4	3	3.6	s
t_{START}	Maximum Current Limit Duration During Inrush		●	50	60	75	ms
t_{CUT}	Maximum Overcurrent Duration After Inrush		●	50	60	75	ms
	Maximum Overcurrent Duty Cycle		●	5.8	6.3	6.7	%
t_{LIM}	Maximum Current Limit Duration After Inrush		●	10	15	20	ms
t_{MPS}	Maintain Power Signature (MPS) Pulse Width Sensitivity	Current Pulse Width to Reset Disconnect Timer (Note 8)	●			6	ms
t_{DIS}	Maintain Power Signature (MPS) Dropout Time	(Note 5)	●	320	370	400	ms
	Minimum Pulse Width for $\overline{RESET}$		●	4.5			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Timing (Figure 4, Note 7 and 9)							
f_{SCLK}	Clock Frequency		●			1	MHz
t_1	Bus Free Time		●	480			ns
t_2	Start Hold Time		●	240			ns
t_3	SCL Low Time		●	480			ns
t_4	SCL High Time		●	240			ns
t_5	SDAIN Data Hold Time		●	60			ns
	Data Clock to SDAOUT Valid		●			250	ns
t_6	Data Set-Up Time		●	80			ns
t_7	Start Set-Up Time		●	240			ns
t_8	Stop Set-Up Time		●	240			ns
t_r	SCL, SDAIN Rise Time		●			120	ns
t_f	SCL, SDAIN Fall Time		●			60	ns
	SCL Fall to ACK Low		●			250	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This chipset includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 140°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: All currents into device pins are positive; all currents out of device pins are negative.

Note 4: The LTC9103 operates with a negative supply voltage (with respect to AGND). To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 5: t_{DIS} is the same as t_{MPDO} defined by IEEE 802.3.

Note 6: The LTC9101-3 digital interface operates with respect to DGND. All logic levels are measured with respect to DGND.

Note 7: Guaranteed by design, not subject to test.

Note 8: The IEEE 802.3 defines MPS as the set of minimum PSE and PD input current requirements to maintain power. An LTC9101-3/LTC9103 port resets its MPS timer when V_{SENSEn} – VSSKn ≥ V_{HOLD} for t_{MPS} and removes port power when V_{SENSEn} – VSSKn ≥ V_{HOLD} for a period longer than t_{DIS}. See Disconnect section.

Note 9: Values Measured at V_{IHD}.

Note 10: Load characteristics of the LTC9103 during Mark: 7V < (AGND – V_{OUTn}) < 10V.

Note 11: The I²C device address is fixed in software with a factory-default value of 0x20 (7-bit address b0100000). The state of the AD[3:0] bits may be reconfigured through a user-defined Configuration package. See Bus Addressing.

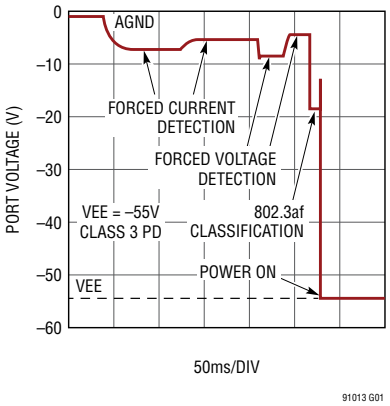
Note 12: Do not source or sink current from CAP1, CAP2, CAP3 and CAP4.

Note 13: Port current and port power measurements depend on sense resistor value (0.1Ω typical). See External Component Selection for details.

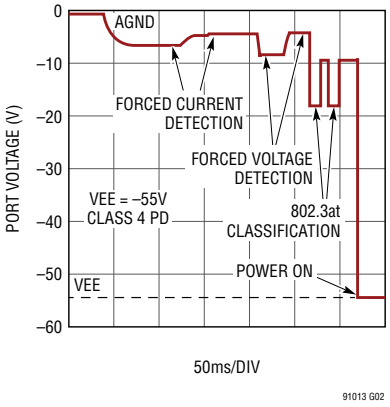
Note 14: See Inrush Control for details on inrush threshold selection.

TYPICAL PERFORMANCE CHARACTERISTICS (R_{SENSE} = 0.1Ω unless otherwise specified.)

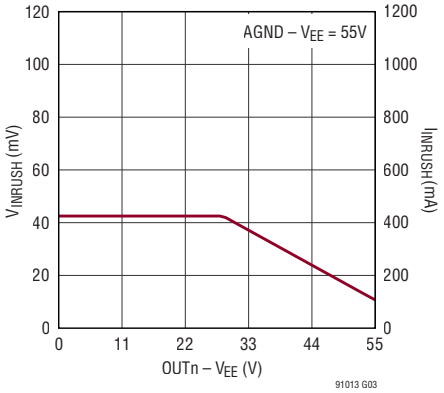
802.3af Power On Sequence



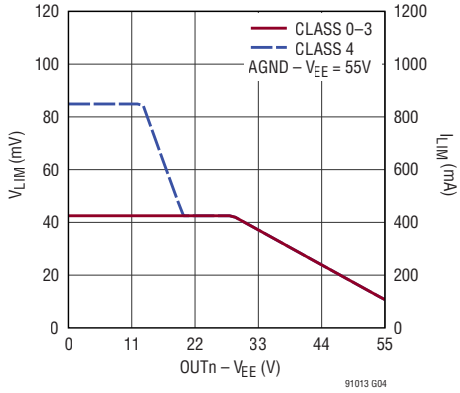
802.3at Power On Sequence



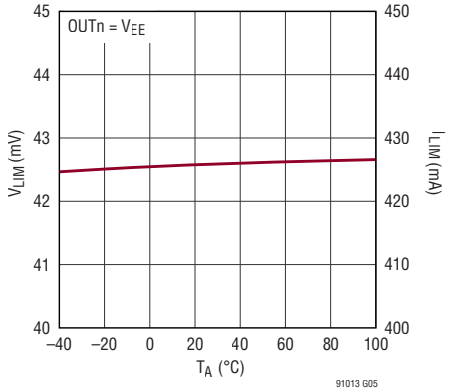
Inrush Current Limit (Note 14)



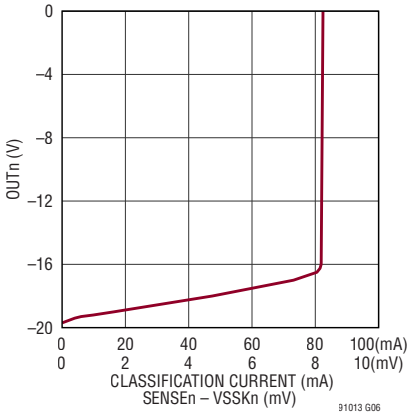
Power-On Current Limits



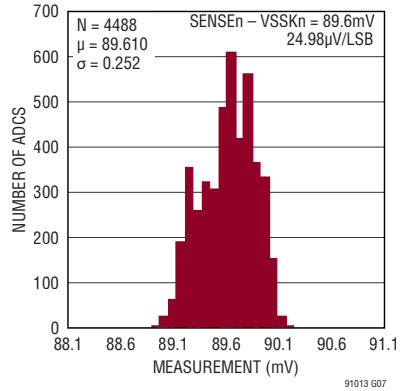
I_{LIM} vs Temperature



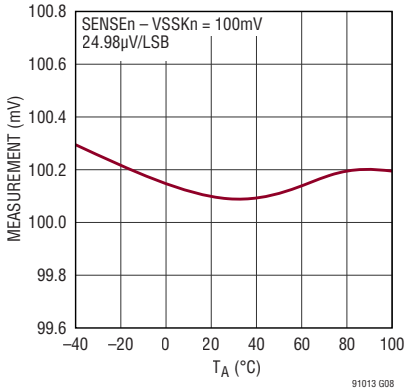
Classification Current Compliance



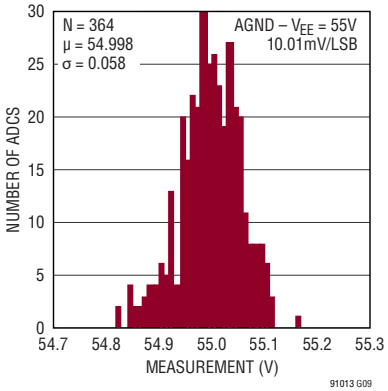
Port Current Measurement



Port Current Measurement vs Temperature

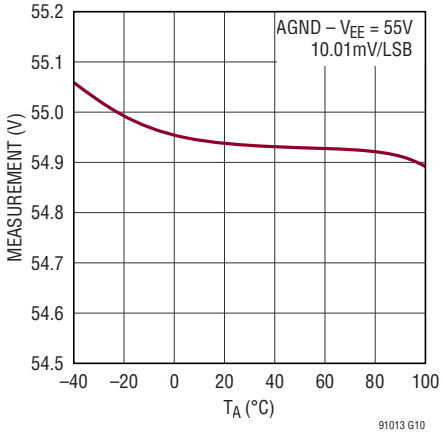


V_{EE} Measurement

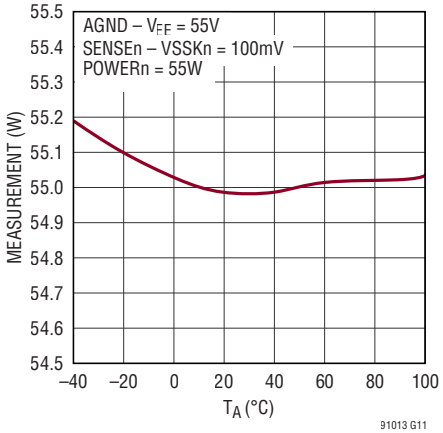


TYPICAL PERFORMANCE CHARACTERISTICS (R_{SENSE} = 0.1Ω unless otherwise specified.)

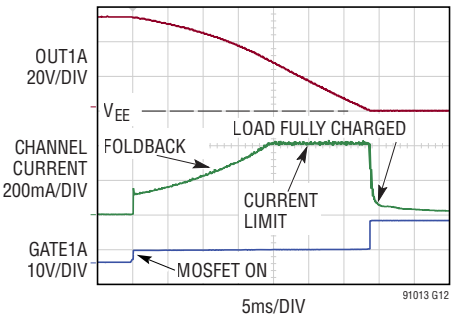
V_{EE} Measurement vs Temperature



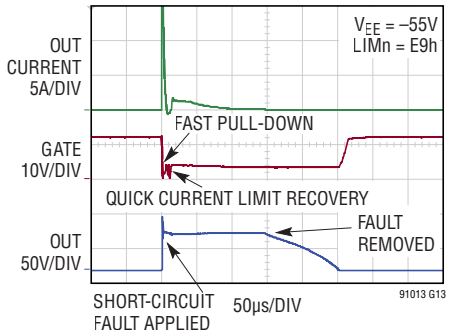
Port Power Measurement vs Temperature



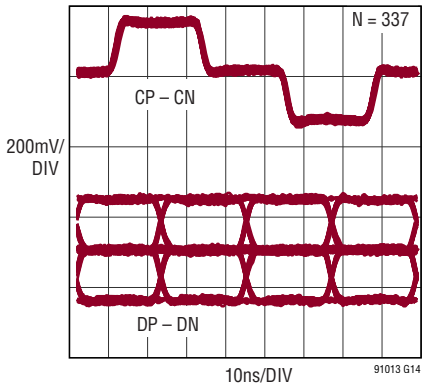
Powering Up into 180µF



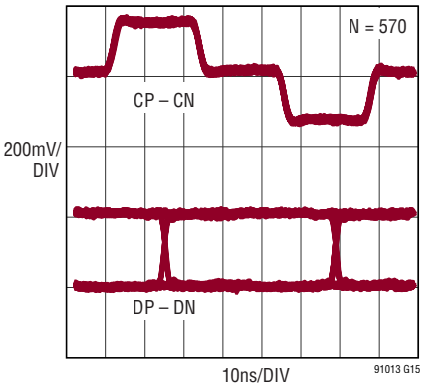
Short Circuit Recovery



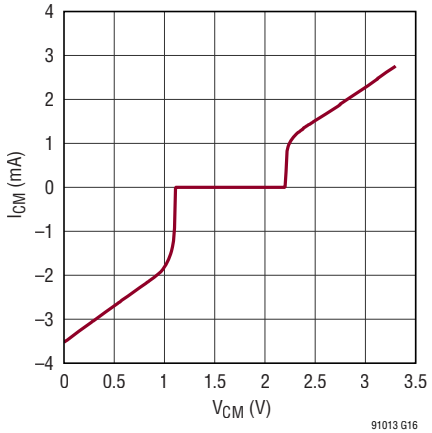
CLOCK and DATA WRITE EYE DIAGRAM



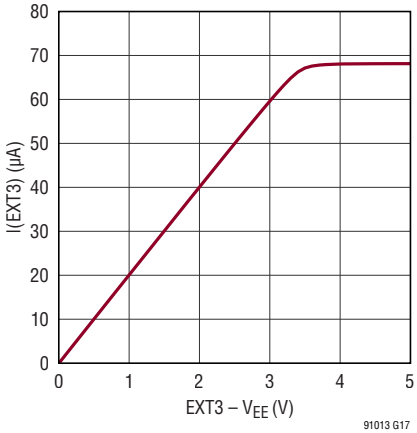
CLOCK and DATA READ EYE DIAGRAM



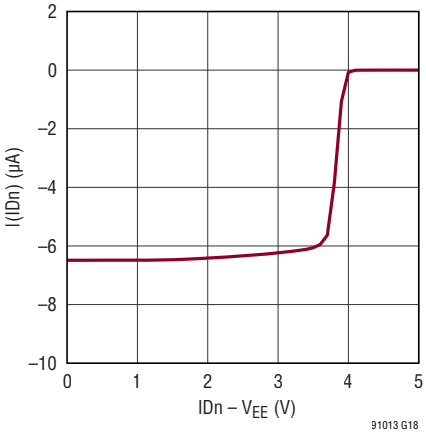
LTC9103 CP/CN and DP/DN Common Mode Correction Current



EXT3 Pin Current vs Voltage

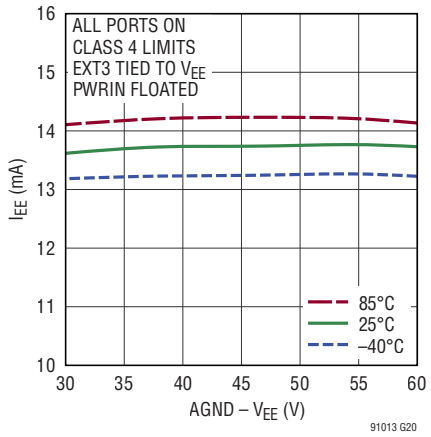


IDn Pin Current vs Voltage

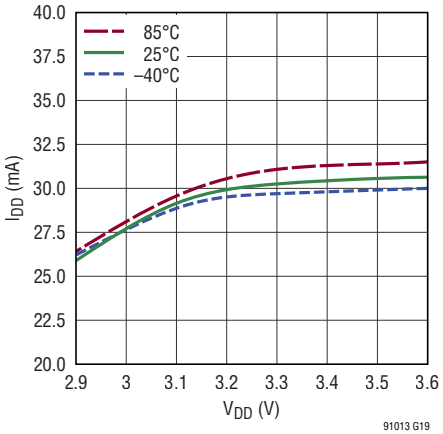


TYPICAL PERFORMANCE CHARACTERISTICS (R_{SENSE} = 0.1Ω unless otherwise specified.)

V_{EE} Supply Current vs Voltage and Temperature



LTC9101-3 V_{DD} Supply Current vs Voltage and Temperature



PIN FUNCTIONS

LTC9103

CAP3 (Pin 1): Analog Internal 3.3V Power Supply Bypass Capacitor. Connect a 1µF ceramic cap to V_{EE}. A 3.3V power supply may be connected to this pin to improve power supply efficiency. The EXT3 pin must be pulled to CAP3 to shut off the internal 3.3V regulator if power is supplied externally. Do not source or sink current from this pin.

EXT3 (Pin 2): External 3.3V Enable. Connect the EXT3 pin to CAP3 to shut off the internal 3.3V regulator when power is supplied externally. Float or connect to V_{EE} for internal regulator operation.

VSSK[8:1] (Pins 47, 46, 39, 38, 15, 14, 7, 6 Respectively): Kelvin Sense to V_{EE}. Connect VSSKn to V_{EE} side of sense resistor for port n through a 0.1Ω resistor. Do not connect directly to V_{EE} plane. See Kelvin Sense Layout Requirements.

SENSE[8:1] (Pins 48, 45, 40, 37, 16, 13, 8, 5 Respectively): Current Sense Input, Port n. SENSEn monitors the external MOSFET current via a 0.1Ω sense resistor between SENSEn and VSSKn. If the voltage across the sense resistor reaches the current limit threshold I_{LIM}, the GATEn pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. If the port is unused, tie SENSEn to V_{EE}.

OUT[8:1] (Pins 49, 44, 41, 36, 17, 12, 9, 4 Respectively): Output Voltage Monitor, Port n. Connect OUTn to the output port. A current limit fold-back circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the drain-to-source voltage exceeds 10V. A 500k resistor is connected internally from OUTn to AGND when the port is idle. If the port is unused, the OUTn pin must float.

GATE[8:1] (Pins 50, 43, 42, 35, 18, 11, 10, 3 Respectively): Gate Drive, Port n. Connect GATEn to the gate of the external MOSFET for port n. When the MOSFET is turned on, the gate voltage is driven to 12V (typ) above V_{EE}. During a current limit condition, the voltage at GATEn will be reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATEn is pulled down, turning the MOSFET off and raising a port fault event. If the port is unused, the GATEn pin must float.

ID[1:0] (Pin 52, 51 respectively): Transceiver ID. Sets the address of the LTC9103 on the multidrop high-speed data interface. ID numbering must start at 00b. Tie high by connecting to CAP3. Tie low by connecting to V_{EE}. The first LTC9103 must have address 00b and, if present, the second must have address 01b.

PWRIN (Pin 55): Startup Regulator Bypass and External Low Voltage Supply Input. Power for the internal 4.3V and 3.3V internal supplies. An internal regulator maintains the voltage of this pin above 6V. An external resistor or supply may be connected to this node to improve the power efficiency of the LTC9103. Connect a 1µF capacitor between this pin and V_{EE}.

AGND (Pin 56): Analog Ground.

PWRMD[1:0] (Pin 57, 58 Respectively): Maximum Power Mode Input. These pins must be left unconnected for all LTC9101-3/LTC9103 applications.

CAP4 (Pin 59): Analog Internal 4.3V Power Supply Bypass Capacitor. Connect a 1µF ceramic cap to V_{EE}. Do not source or sink current from this pin.

V_{EE} (Pins 60, 65): Main PoE Supply Input. Connect to a –51V to –57V supply, relative to AGND.

DNA (Pin 61): Data Transceiver Negative Input Output (Analog). Connect to DND through a data transformer.

DPA (Pin 62): Data Transceiver Positive Input Output (Analog). Connect to DPD through a data transformer.

CNA (Pin 63): Clock Transceiver Negative Input Output (Analog). Connect to CND through a data transformer.

CPA (Pin 64): Clock Transceiver Positive Input Output (Analog). Connect to CPD through a data transformer.

Common Pins

NC, DNC (LTC9101-3 Pin 4, 21; LTC9103 Pins 19-34, 53, 54: All pins identified with “NC” or “DNC” must be left unconnected.

PIN FUNCTIONS

LTC9101-3

CFG[2:0] (Pins 3, 2, 1 Respectively): Device Configuration Inputs. Tie the configuration pins to set the number of ports and connected LTC9103s. See DEVICE CONFIGURATION for details.

$\overline{\text{LEGACY}}$ (Pin 5): Legacy Mode Input. Tie the $\overline{\text{LEGACY}}$ pin to DGND for Legacy Mode Operation. Leave floating for IEEE 802.3at compliant Operation. Legacy Mode is continuously and globally updated based on pin state.

PC (Pin 6): LED Shift Register Parallel Capture Output. This pin provides the parallel capture strobe for external shift registers. PC must be followed locally by a Schmitt trigger to drive the downstream shift registers.

CAP[2:1] (Pins 7, 23 Respectively): Core Power Supply Bypass Capacitors. Connect each pin to a 1µF capacitance to DGND for the internal 1.2V regulator bypass. Do not use other capacitor values. Do not source or sink current from this pin.

CPD (Pin 8): Clock Transceiver Positive Input Output (Digital). Connect to CPA through a data transformer.

CND (Pin 9): Clock Transceiver Negative Input Output (Digital). Connect to CNA through a data transformer.

DPD (Pin 10): Data Transceiver Positive Input Output (Digital). Connect to DPA through a data transformer.

DND (Pin 11): Data Transceiver Negative Input Output (Digital). Connect to DNA through a data transformer.

V_{DD} (Pins 12, 19, 24): V_{DD} IO Power Supply. Connect to a 3.3V power supply relative to DGND. Each V_{DD} pin must be locally bypassed with at least a 0.1µF capacitor. A 10µF bulk capacitor must be connected across V_{DD} for increased surge immunity.

SD (Pin 13): LED Shift Register Data Output. This pin provides the data for external shift registers. SD must be followed locally by a Schmitt trigger to drive the downstream shift registers.

$\overline{\text{RESET}}$ (Pin 14): Reset Input, Active Low. When $\overline{\text{RESET}}$ is low, the LTC9101-3/LTC9103 is held inactive with all ports off and all internal registers reset. When $\overline{\text{RESET}}$ is pulled high, the LTC9101-3/LTC9103 begins normal operation. $\overline{\text{RESET}}$ can be connected to an external capacitor or RC network to provide a power turn-on delay. Internal filtering of $\overline{\text{RESET}}$ prevents glitches less than 1µs wide from resetting the LTC9101-3/LTC9103. Internally pulled up to V_{DD}.

$\overline{\text{OVR}}$ (Pin 15): Supply Overload Indicator Output, Active Low. The $\overline{\text{OVR}}$ pin may be used to drive an LED through a current limiting resistor.

SDAOUT (Pin 16): Serial Data Output, Open Drain Data Output for the I^2C Serial Interface Bus. The LTC9101-3 uses two pins to implement the bidirectional SDA function to simplify opto isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

SDAIN (Pin 17): Serial Data Input. High impedance data input for the I^2C serial interface bus. The LTC9101-3 uses two pins to implement the bidirectional SDA function to simplify opto isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

SCL (Pin 18): Serial Clock Input. High impedance clock input for the I^2C serial interface bus. The SCL pin should be connected directly to the I^2C SCL bus line. SCL must be tied high if the I^2C serial interface bus is not used.

SC (Pin 20): LED Shift Register Clock Output. This pin provides the clock signal for external shift registers. SC must be followed locally by a Schmitt trigger to drive the downstream shift registers.

DGND (Pins 22, 25): Digital Ground. DGND must be connected to the return from the V_{DD} supply.

TEST TIMING DIAGRAMS

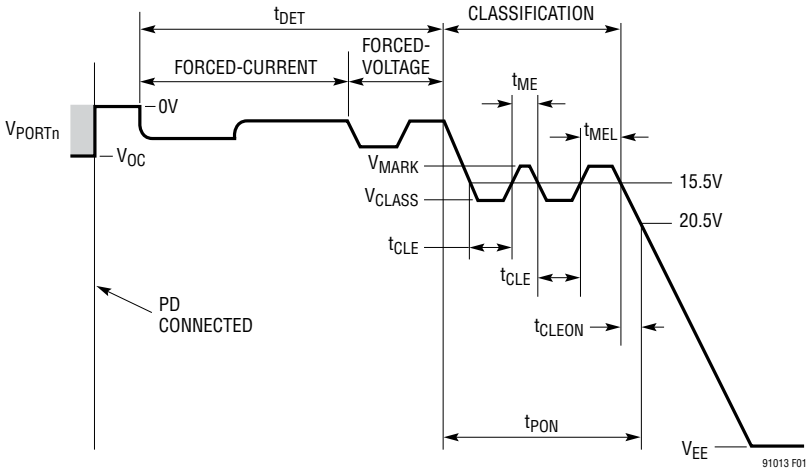


Figure 1. Detect, Class and Turn-On Timing

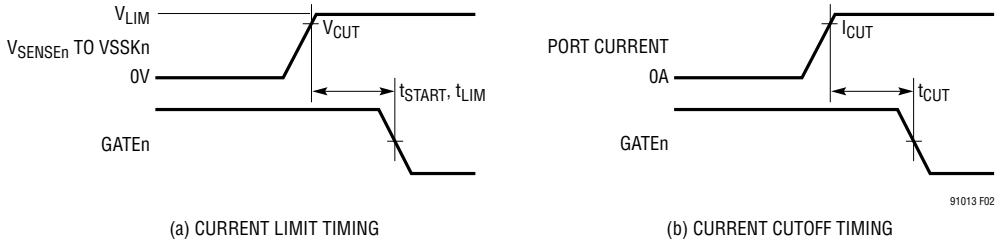


Figure 2. Current Timings

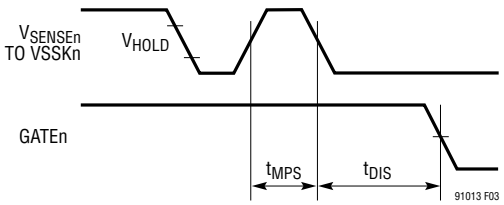


Figure 3. DC Disconnect Timing

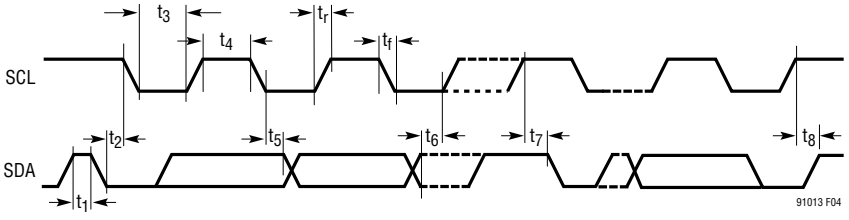


Figure 4. I²C Interface Timing

I²C TIMING DIAGRAMS

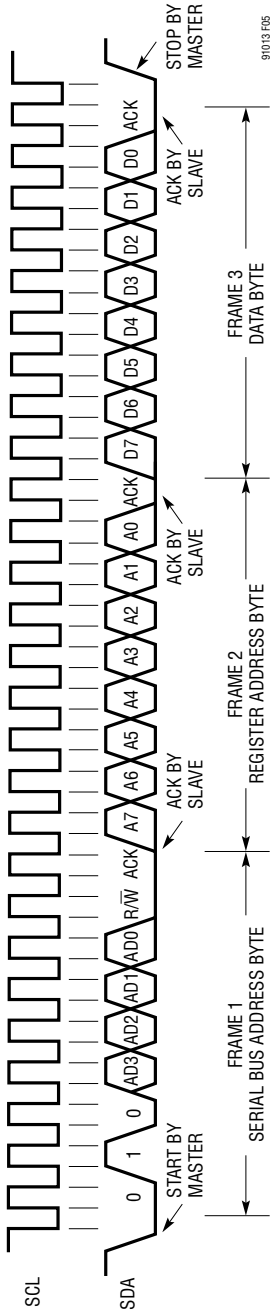


Figure 5. Writing to a Register (Note 11)

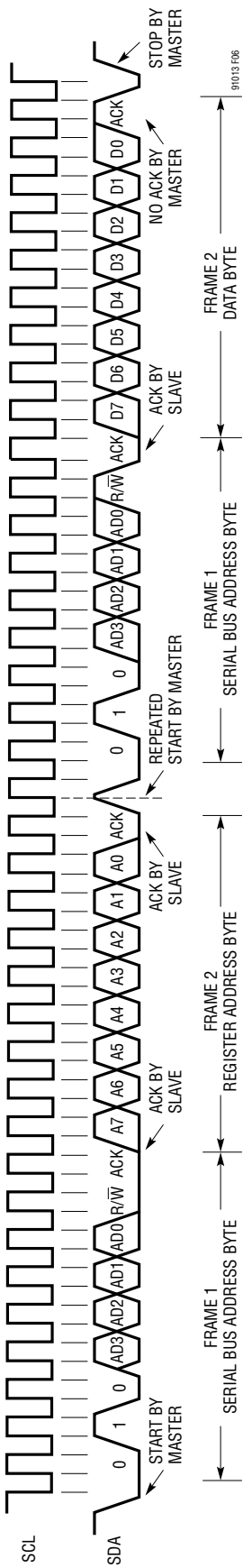


Figure 6. Reading from a Register (Note 11)

APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet, or PoE, is a standard protocol for sending DC power over copper Ethernet data wiring. The IEEE group that administers the 802.3 Ethernet data standards added PoE powering capability in 2003. This original PoE spec, known as 802.3af, allowed for 48V DC power at up to 13W. This initial specification was widely popular, but 13W was not adequate for some requirements. In 2009, the IEEE released a new standard, known as 802.3at or PoE+, increasing the voltage and current requirements to provide 25W of power.

The IEEE standard also defines PoE terminology. A device that provides power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: Endpoints (typically network switches or routers), which provide data and power; and Midspans, which provide power but pass through data. Midspans are typically used to add PoE capability to existing non-PoE networks. PDs are typically IP phones, wireless access points, security cameras, and similar devices.

Power Management

The LTC9101-3 is designed to operate as a fully autonomous 802.3at compliant PSE system controller. No external host processor control is required.

The following power management functions are provided:

- System power budget
- Port priorities
- Supply Overload LED

The system power budget is set to a fixed value upon LTC9101-3 reset, according to either CFG pins or optional configuration package overrides. The LTC9101-3 will track the total power usage across all powered ports and manage port power status by granting, revoking, or denying power based on relative port priorities and power availability.

Port priority is pre-defined. Port 1 has the highest power priority, port 2 has the second highest priority. The highest numbered port in the system has the lowest port priority.

System power consumption is monitored by the LTC9101-3 based on dynamic power usage. When a valid PD is connected, the PD is powered based on available power and port priority. When a new PD is connected, physical layer classification identifies the PD requested power. The following algorithm is performed:

```
// Attempt to power on port based on available power
if ((system power consumption + PD requested power) < system power budget)
  power port on
else
  // Power down one or more lower priority ports to free power budget
  revoke lower priority powered ports
  system power consumption = system power consumption – revoked PD power
  // Try to power port on again based on freed power from revoked ports
  if ((system power consumption + PD requested power) < system power budget)
        power port on
```

APPLICATIONS INFORMATION

In addition, the dynamic system power consumption is periodically policed by the power management algorithm. If the system power consumption exceeds the system power budget, low priority port power will be revoked until the usage is within the system power budget. Re-powering of revoked ports is subsequently governed by the power on algorithm shown previously.

The Supply Overload LED is off when system power consumption is less than the Near Power Limit threshold. The Supply Overload LED is on when system power consumption is greater than the Near Power Limit threshold. The Supply Overload LED stays on until power consumption becomes lower than the Near Power Limit Reset threshold. If system power consumption exceeds the system power budget power will be denied from the lowest priority port and the Supply Overload LED will blink. The port status LED will blink for the respective port which is denied power. See Table 1 Default Device Configuration Options.

System power budget, near power limit trigger/reset thresholds and port priorities are configurable via eFlash-programmable configuration packages. Contact Analog Devices Applications for support with LTC9101-3 configuration packages.

PoE BASICS

Common Ethernet data connections consist of two or four twisted pairs of copper wire (commonly known as Ethernet cable), transformer-coupled at each end to avoid ground loops. PoE systems take advantage of this coupling arrangement by applying voltage between the center-taps of the data transformers to transmit power from the PSE to the PD without affecting data transmission. Figure 7 shows a high level PoE system schematic.

To avoid damaging legacy data equipment that does not expect to see DC voltage, the PoE specification defines a protocol that determines when the PSE may apply and remove power. Valid PDs are required to have a specific 25k common-mode resistance at their input. When such a PD is connected to the cable, the PSE detects this signature resistance and turns on the power. When the PD is later disconnected, the PSE senses the open circuit and turns power off. The PSE also turns off power in the event of a current fault or short circuit.

When a PD is detected, the PSE optionally looks for a classification signature that tells the PSE the maximum power the PD will draw. The PSE can use this information to allocate power among several ports, to police the current consumption of the PD, or to reject a PD that will draw more power than the PSE has available. The classification step is optional; if a PSE chooses not to classify a PD, it must assume that the PD is a 13W (full 802.3af power) device.

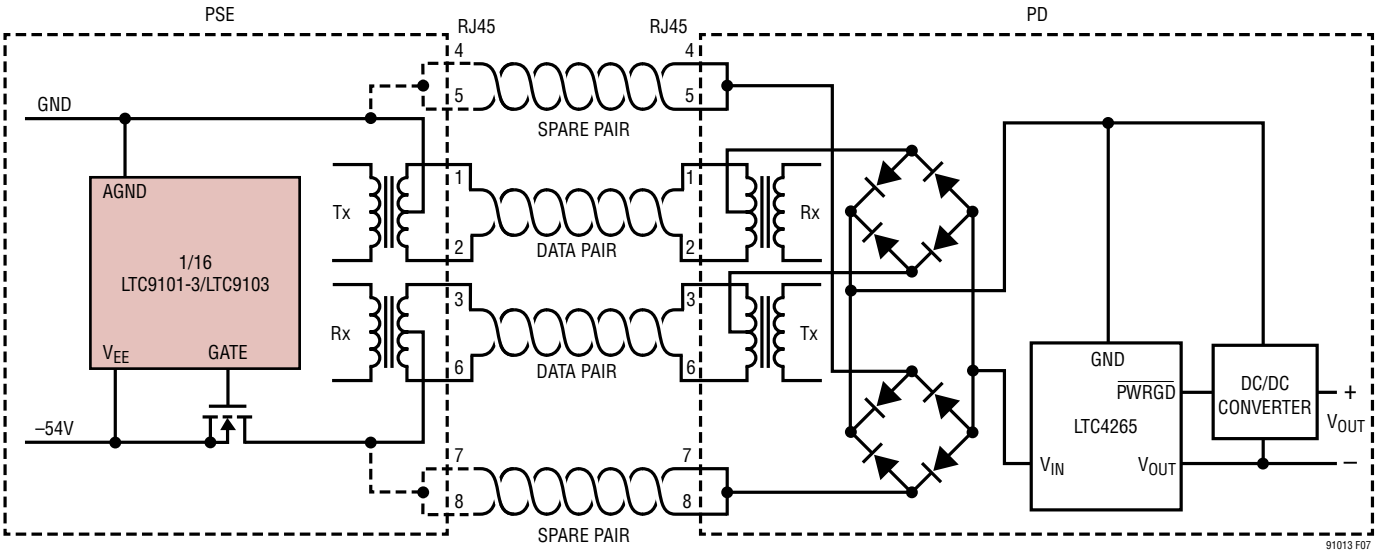


Figure 7. Power Over Ethernet System Diagram, Spare or Data Pairs

APPLICATIONS INFORMATION

Table 1. Default Device Configuration Options

CFG [2:0]		LTC9103 DEVICE COUNT	TOTAL NUMBER OF PORTS	SYSTEM POWER BUDGET	SET POWER WARNING	POWER WARNING RESET
0	000	1	8	64W	49W	45W
2	010	2	16	128W	113W	109W

DEVICE CONFIGURATION

An LTC9101-3 can control either one or two LTC9103s. Each LTC9103 controls 8 ports. Thus, each LTC9101-3 can control up to 16 power ports. Note that CFG0 and CFG2 must always be tied low. See Table 1.

DETECTION

Detection Overview

To avoid damaging network devices that were not designed to tolerate DC voltage, a PSE must determine whether the connected device is a valid PD before applying power. The IEEE specification requires that a valid PD have a common-mode resistance of 25k ±5% at any port voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k (shaded regions in Figure 8). The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer network ports, many of which have 150Ω common-mode termination resistors that will be damaged if power is applied to them (the black region at the left of Figure 8).

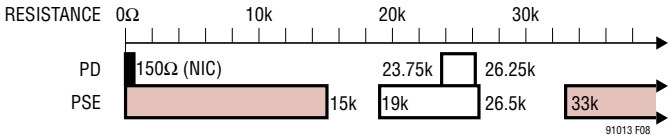


Figure 8. IEEE 802.3af Signature Resistance Ranges

4-Point Detection

The LTC9101-3/LTC9103 uses a 4-point detection method to discover PDs. False-positive detections are minimized by checking for signature resistance with both forced-current and forced-voltage measurements.

Initially, two test currents are forced onto the port (via the OUTn pin) and the resulting voltages are measured. The detection circuitry subtracts the two V-I points to determine the resistive slope while removing offset caused by series diodes or leakage at the port (see Figure 9). If the forced-current detection yields a valid signature resistance, two test voltages are then forced onto the port and the resulting currents are measured and subtracted. Both methods must report valid resistances for the port to acknowledge a valid detection. PD signature resistances between 17k and 29k (typically) are detected as valid. See Table 2.

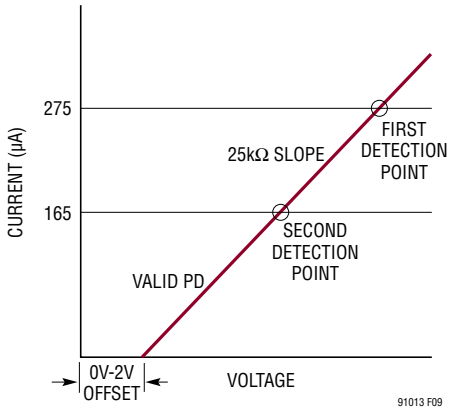


Figure 9. PD Detection

Table 2. Detection Status

MEASURED PD SIGNATURE	DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
< 2.4k	Short Circuit
Capacitance > 2.7µF	C_{PD} too High
2.4k < R_{PD} < 17k	R_{SIG} too Low
17k < R_{PD} < 29k	Detect Good
< 29k < R_{PD} < 50k	R_{SIG} too High
> 50k	Open Circuit
Voltage > 10V	Port Voltage Outside Detect Range

APPLICATIONS INFORMATION

Detection of Legacy PDs

Proprietary PDs that predate the original IEEE 802.3af standard are commonly referred to today as legacy devices. One type of legacy PD uses a large common-mode capacitance (>10µF) as the detection signature. Note that PDs in this range of capacitance are defined as invalid, so a PSE that powers legacy PDs is technically noncompliant with the IEEE spec. The LTC9101-3/LTC9103 can be configured to detect this type of legacy PD using the $\overline{\text{LEGACY}}$ pin. When enabled, the port will accept the detection result as valid when it sees either a valid IEEE PD or a high-capacitance legacy PD. With legacy mode disabled, only valid IEEE PDs will be powered.

CLASSIFICATION

802.3af Classification

A PD may optionally present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 15.5V and 20.5V), with the current level indicating one of 5 possible PD class signatures. Figure 10 shows a typical PD load line, starting with the slope of the 25k signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the V_{CLASS} range. Table 3 shows the possible classification values.

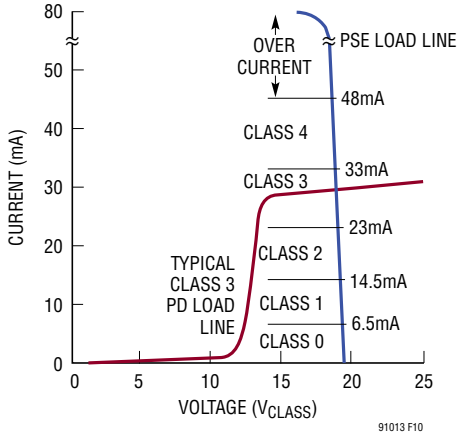


Figure 10. PD Classification

Table 3. 802.3af and 802.3at Classification Values

CLASS	RESULT
0	No Class Signature Present; Treat Like Class 3
1	3W
2	7W
3	13W
4	25.5W (Type 2)

If classification is enabled, the PSE will classify the PD immediately after a successful detection cycle. It measures the PD classification signature by applying 18V for 12ms (both values typical) via the OUTn pin and measures the resulting current. The LTC9101-3/LTC9103 uses the classification result to set the I_{CUT}, I_{LIM}, and P_{CUT} thresholds as shown in Table 4.

Table 4. I_{CUT}, I_{LIM} and P_{CUT} Values

PSE ASSIGNED CLASS	I_{CUT}	I_{LIM}	P_{CUT}
1	94mA	425mA	4.86W
2	150mA	425mA	7.56W
3	338mA	425mA	16.2W
4	638mA	850mA	32.4W

802.3at 2-Event Classification

In 802.3at, 802.3af classification is named Type 1 classification. The 802.3at standard introduces an extension of Type 1 classification: Type 2 (2-event) classification. Type 2 PSEs are required to perform classification.

A Type 2 PD requesting 25.5W presents class signature 4 during all class events. If a Type 2 PSE with 25.5W of available power measures class signature 4 during the first class event, it forces the PD to V_{MARK} (9V typical), pauses briefly, and issues a second class event as shown in Figure 12. The second class event informs the PD that the PSE has allocated 25.5W.

Note that the second classification event only runs if required by the IEEE classification procedure. For example, a single-signature Class 0 to 3 PD will only be issued a single class event as shown in Figure 11.

APPLICATIONS INFORMATION

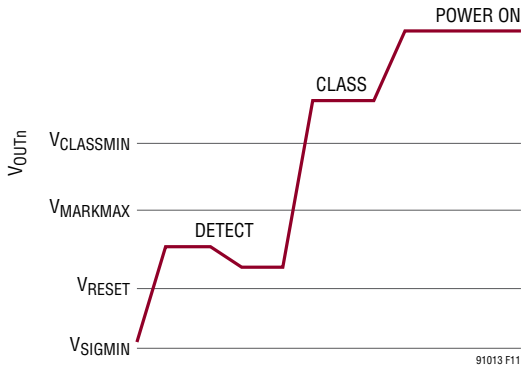


Figure 11. Type 1 or 2 PSE, 1-Event Class Sequence

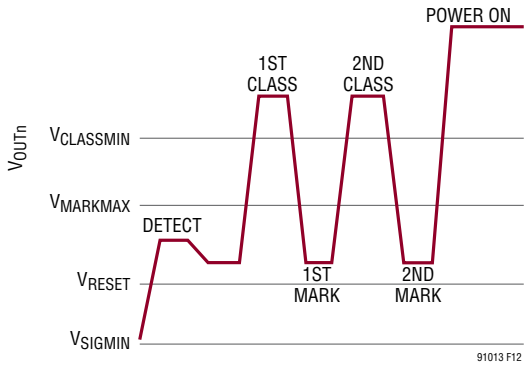


Figure 12. Type 2 PSE, 2-Event Class Sequence

The concept of demotion is introduced in 802.3at. A Type 2 PD may be connected to a PSE only capable of delivering 13W, perhaps due to power management limitations. In this case, the PSE will perform a single classification event as shown in Figure 11, and note that 25.5W is requested. Due to the limited power availability, the PSE will not issue a second event and proceeds directly to power on the PD. The presence of a single class event informs the Type 2 PD it has been demoted to 13W. If demoted, the PD is subject to power limitations and may operate in a reduced power mode.

Invalid Type 2 Class Combinations

The 802.3at specification defines a Type 2 PD class signature as two consecutive Class 4 results; a Class 4 followed by a Class 0-3 is not a valid signature. The LTC9101-3/LTC9103 will not provide power to a PD with an invalid class signature.

POWER CONTROL

The primary function of the LTC9101-3/LTC9103 is to control power delivery to the PSE port. It does this by controlling the gate drive voltage of an external power MOSFET while monitoring the current (through an external sense resistor) and the output voltage (across the OUT pin).

The LTC9101-3/LTC9103 connects the V_{EE} power supply to the PSE port in a controlled manner, meeting the power demands of the PD while minimizing power dissipation in the external MOSFET and disturbances to the V_{EE} backplane.

Inrush Control

When commanded to apply power to a port, the LTC9101-3/LTC9103 ramps up the GATE pin, raising the external MOSFET gate voltage in a controlled manner.

During a typical inrush, the MOSFET gate voltage will rise until the external MOSFET is fully enhanced or the port reaches the inrush current limit (I_{INRUSH}). I_{INRUSH} is set automatically by the PSE. The GATE pin will be servoed if port current exceeds I_{INRUSH}, actively limiting current to I_{INRUSH}. When the GATE pin is not being servoed, the final V_{GS} is 12V (typical).

During inrush, the port runs a timer (t_{START}). The port stays in inrush until t_{START} expires. When t_{START} expires, the PSE inspects port voltage and current. When the PSE is applying power to a PD, inrush is successful if the port is drawing current below I_{INRUSH}. If inrush is not successful, power is removed and a t_{START} fault is set. Otherwise, the port advances to power on and the programmed current limiting thresholds are used as described in the Current Cutoff and Limit section.

Port Power Policing

The power policing threshold (P_{CUT}) is monitored on a per-port basis per Table 4. When the total output power over 100ms moving average exceeds the specified threshold, power is removed from the port.

APPLICATIONS INFORMATION

Current Cutoff and Limit

Each LTC9101-3/LTC9103 port includes two current limiting thresholds (I_{CUT} and I_{LIM}), each with a corresponding timer (t_{CUT} and t_{LIM}). The thresholds are set based on the classification result as shown in Table 3.

Per the IEEE specification, the LTC9101-3/LTC9103 allows the port current to exceed I_{CUT} for a limited period of time before removing power from the port, whereas it will actively control the MOSFET gate drive to keep the port current below I_{LIM}. The port does not take any action to limit the current when only the I_{CUT} threshold is exceeded, but does start the t_{CUT} timer. If the current drops below the I_{CUT} current threshold before its timer expires, the t_{CUT} timer counts back down, but at 1/16 the rate that it counts up. If the t_{CUT} timer reaches 65ms (typical) the port is turned off and the port. This allows the current limit circuitry to tolerate intermittent overload signals with duty cycles below about 6%; longer duty cycle overloads will turn the port off.

The I_{LIM} current limiting circuit is always enabled and actively limiting port current. The t_{LIM} timer starts when the I_{LIM} threshold is exceeded. When the t_{LIM} timer reaches 15ms (typical) the port is turned off. The current limit timer threshold is reconfigurable by way of embedded flash configuration.

I_{LIM} Foldback

The LTC9101-3/LTC9103 I_{LIM} threshold is implemented as a two-stage foldback circuit that reduces the port current if the port voltage falls below the normal operating voltage. This keeps MOSFET power dissipation at safe levels.

MOSFET Fault Detection

LTC9101-3/LTC9103 PSE ports are designed to tolerate significant levels of abuse, but in extreme cases it is possible for an external MOSFET to be damaged. A failed MOSFET may short source to drain, which will make the port appear to be on when it should be off; this condition may also cause the sense resistor to fuse open, turning off the port but causing SENSE to rise to an abnormally high voltage. A failed MOSFET may also short from gate to drain, causing GATE to rise to an abnormally high voltage. OUT, SENSE and GATE are designed to tolerate up to 80V faults without damage.

If the LTC9101-3/LTC9103 detects any of these conditions for more than 4ms (typical), it disables all functionality on the affected port, reduces the gate drive pull-down current MOSFET. This is typically a permanent fault, but the user can attempt to recover by resetting the entire chip. If the MOSFET is in fact bad, the port will disable itself again. The remaining ports of the LTC9101-3/LTC9103 are unaffected.

Disconnect

The LTC9101-3/LTC9103 monitors powered ports to ensure the PD continues to draw the minimum specified current. A disconnect timer counts up whenever port current is below 7mA (V_{HOLD} typ), indicating that the PD has been disconnected. If the t_{DIS} timer expires, the port will be turned off. If the current returns before the t_{DIS} timer runs out, the timer resets. As long as the PD exceeds the minimum current level more often than t_{DIS}, the port will remain powered.

The LTC9101-3/LTC9103 does not include AC disconnect circuitry.

Fast Surge Recovery

High reliability systems demand excellent surge recovery. It is increasingly important for a PSE to minimize power disruption to the PDs during extreme power transients. Furthermore, PDs that do not meet minimum bulk capacitance requirements are particularly vulnerable to power brownouts with traditional PSE solutions. The LTC9101-3/LTC9103 provides industry-leading hot swap responsiveness with excellent recovery from surge events.

During a surge event, the LTC9103 GATE pin quickly turns off the external MOSFET current flow to protect the PSE, the MOSFET, and downstream circuitry.

As the surge dissipates, the LTC9103 quickly turns the MOSFET back on in a safe, current limited manner while minimizing power disruption to the PD. The LTC9103 fast MOSFET turn off and power recovery better support both IEEE compliant PDs and PDs with lower bulk capacitance in high reliability applications.

APPLICATIONS INFORMATION

LED Power On Self Test

After reset the Supply Overload and all port LEDs will implement a two phase power on self test. The first phase lasts four seconds during which the Supply Overload LED blinks, the port status LED is on, and the port fault LED is off. The second phase also lasts four seconds during which the Supply Overload LED blinks, the port status LED is off, and the port fault LED is on.

Port operation will have already begun during this eight second period. After the LED power on self test, LED behaviors will transition to normal system and port status.

System Telemetry

The LTC9101-3 features an interface to control an external serial LED driver for per-port status and fault LEDs, and a dedicated pin to control a Supply Overload LED. Using these features the LTC9101-3 can display complex system and port status telemetry. Telemetry is broken up into two components: port operation and power management.

Port operation is displayed via per-port status and fault LEDs. The LTC9101-3 displays port power status via that port's status LED and conveys a list of port faults via blink codes on that port's fault LED. A list of status and fault conditions and their factory-default LED responses are shown in Table 5.

Power management information is displayed via the Supply Overload LED and secondarily via per-port fault and status LEDs. The LTC9101-3 conveys conditions such as system power near-limit warning, system power limit, and port power revoked via the Supply Overload LED and blink codes on the corresponding port fault LED(s). A list of power management conditions and their factory-default LED responses are shown in Table 6.

LED behaviors are configurable via user-defined settings in the eFlash-programmable configuration package. Contact Analog Devices Applications for support with generating and downloading configuration packages for use with LTC9101-3/LTC9103.

Overtemperature Protection

Overtemperature protection automatically removes power from affected ports when LTC9103 temperature exceeds a preset threshold (150°C, typ). Ports are prevented from resuming operation until the die temperature drops below a preset recovery threshold (125°C, typ).

Table 5. PoE Operation vs. Port LEDs

	LED	
CONDITION	**PORT STATUS**	**PORT FAULT**
Detect Open	Off	Off
Port Powered	On	Off
Detect Invalid	Off	Blink
Class Invalid	Off	Blink
Inrush Fault*	Off	Blink
P_{CUT}, I_{CUT} and I_{LIM}*	Off	Blink
DC Disconnect*	Off	Blink

* These blink faults persist for 2-3 secs, then a new detection cycle begins and the port LED is updated based on the latest results..

Notes:
- Supply Overload LED is not affected by PoE Operation conditions.
- Blink rate is 800ms on and 800ms off.

Table 6. Power Management vs. LEDs

	LED		
CONDITION	**SUPPLY OVERLOAD**	**PORT STATUS**	**PORT FAULT**
Power Available	Off	N/A	N/A
Near Power Limit	On	N/A	N/A
Power Denied	Blink	Blink	Off
Power Revoked	Blink	Blink	Off

Note: Blink rate is 800ms on and 800ms off.

SERIAL DIGITAL INTERFACE

Overview

The serial interface allows configuration downloads but is not required during normal operation. The LTC9101-3 communicates with the flash programmer using a standard SMBus/I^2C 2-wire interface. The LTC9101-3 is a slave-only device, and communicates with the flash programmer master using standard SMBus protocols. The timing diagrams (Figure 5 and Figure 6) show typical communication waveforms and their timing relationships. More information about the SMBus data protocols can be found at www.smbus.org.

APPLICATIONS INFORMATION

Code Download

LTC9101-3 firmware is field-upgradeable by downloading and executing firmware images.

Contact Analog Devices for code download procedures and firmware images.

Two complete copies of firmware images are maintained under separate ECC and CRC protection for maximum data protection.

Bus Addressing and Restrictions

The LTC9101-3's I^2C address base is 0x20. Address 0x20 through 0x30 are restricted for use by the LTC9101-3.

LED Indicators

The LTC9101-3 provides Shift Register Data (SD), Shift Register Clock (SC), and Parallel Capture Clock (PC) to the external shift registers that drive the port LED indicators. Two 8-bit shift registers drive an 8-port application while four 8-bit shift registers drive a 16-port application. Each port has two LEDs, typically a green LED for port status and orange for port faults.

Figure 13 shows the hardware connections for the indicator LED serial driver in a 16-port system.

Figure 14 shows the timing waveform of SD, SC, and PC. Table 7 shows the data variables A0 through A15, and what port LED they correspond to.

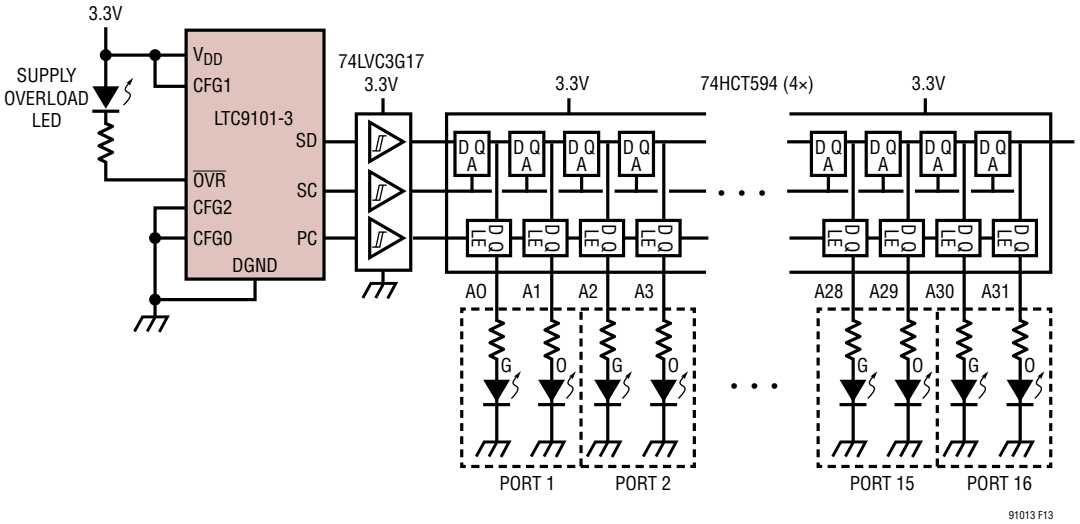


Figure 13. LTC9101-3/LTC9103 Shift Register to LED Connectivity in a 16-Port Application

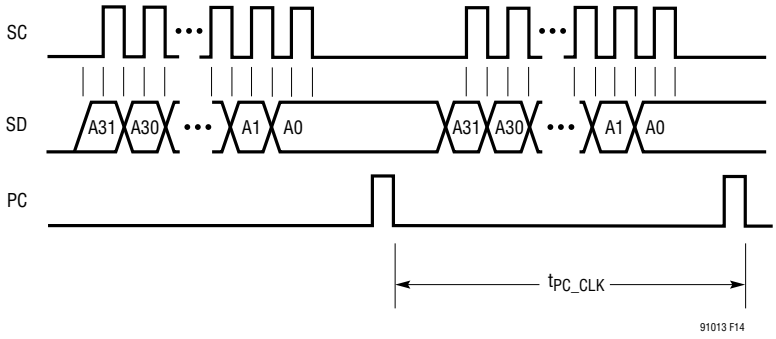


Figure 14. LTC9101-3/LTC9103 SC, SD, and PC Waveform

APPLICATIONS INFORMATION

Table 7. Port LEDs and Corresponding LED Data Variables for an 8-Port System

PORT	PORT LED	SERIAL DATA
1	Status	A0
	Fault	A1
2	Status	A2
	Fault	A3
3	Status	A4
	Fault	A5
4	Status	A6
	Fault	A7
5	Status	A8
	Fault	A9
6	Status	A10
	Fault	A11
7	Status	A12
	Fault	A13
8	Status	A14
	Fault	A15

Note: This sequence is continued for a 16-port application.

In addition, the LTC9101-3 also provides a Supply Overload LED bit through the $\overline{OVR}$ pin, which gives indication that the LTC9101-3/LTC9103 PSE application has either denied power, revoked power, or is near the power limit. The Supply Overload LED fault conditions are detailed in the Power Management and System Telemetry sections.

ISOLATION REQUIREMENTS

IEEE 802.3 Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, network segments are not required to be isolated from each other, provided that the segments are connected to devices residing within a single building on a single power distribution system.

If the PSE is part of a larger system, contains additional external non-Ethernet ports, or must be referenced to protective ground for some other reason, the PoE subsystem must be electrically isolated from the rest of the system.

The LTC9101-3/LTC9103 chipset simplifies PSE isolation by allowing the LTC9101-3 chip to reside on the non-isolated side. There it can receive power from the main logic supply. Isolation between the LTC9101-3 and LTC9103 is implemented using a proprietary transformer-based communication protocol. Additional details are provided in the High-Speed Data Interface section of this data sheet.

For autonomously managed PoE switches, the isolation requirement can be met by using an isolated main power supply for the entire device. This strategy can be used if the device has no electrically conducting ports other than twisted-pair Ethernet. The LTC9101-3 may directly connect to the LTC9103s in the above circumstances, or if the system already provides isolation.

EXTERNAL COMPONENT SELECTION

Power Supplies

The LTC9101-3/LTC9103 requires two supply voltages to operate. V_{DD} requires 3.3V (nominally) relative to DGND. V_{EE} requires a negative voltage of between –51V to –57V.

Digital Power Supply

V_{DD} provides digital power for the LTC9101-3 processor. A ceramic decoupling cap of at least 0.1µF should be placed from each V_{DD} to DGND, as close as practical to each LTC9101-3. In addition, each LTC9101-3 must include a bulk cap of 10µF for robust surge immunity. A 1.2V core voltage supply is generated internally and requires a 1µF ceramic decoupling cap between the CAP1 pin and DGND and between CAP2 and DGND.

In systems using ADI's proprietary isolation, V_{DD} should be delivered by the system's non-isolated 3.3V supply. To maintain required isolation, LTC9103 AGND and LTC9101-3 DGND must not be connected. If using the direct connection scheme, the LTC9101-3 DGND must be connected to LTC9103 V_{EE}.

APPLICATIONS INFORMATION

Main PoE Power Supply

V_{EE} is the main isolated PoE supply that provides power to the PDs. Because it supplies a relatively large amount of power and is subject to significant current transients, it requires more design care than a simple logic supply. For minimum IR loss and best system efficiency, set V_{EE} near maximum amplitude (57V), leaving enough margin to account for transient over or undershoot, temperature drift, and the line regulation specifications of the particular power supply used.

A bypass capacitor and a transient voltage suppressor (TVS) between each LTC9103 AGND and V_{EE} are very important for reliable operation. If a short circuit occurs at one of the output ports it can take as long as 1µs for the LTC9103 to begin regulating the current. During this time the current is limited only by the small impedances in the circuit; a high current spike typically occurs, causing a voltage transient on the V_{EE} supply and possibly causing the LTC9101-3/LTC9103 to reset due to a UVLO fault. A 1µF, 100V X7R capacitor and an SMAJ58A near each LTC9103 are recommended to minimize spurious resets. An electrolytic bulk capacitor of at least 47µF, 100V and a bulk TVS are also recommended per system.

LTC9103 Low Voltage Power Supplies

The LTC9103 includes internal voltage regulators that generate low voltage supplies directly from the main PoE power supply. At startup, an internal regulator generates 6V at PWRIN, drawing power from AGND. Internal 4.3V and 3.3V rails are sub-regulated from PWRIN. The PWRIN pin requires a local 1µF, 100V bypass capacitor.

Pull-up resistors can be connected from PWRIN to AGND to dissipate heat outside the LTC9103 package. Optionally, an external power supply can be connected to PWRIN to override the startup regulator and reduce power dissipation.

Figure 15 shows a pull-up resistor configuration with the internal 3.3V regulator. Bypass resistors R1, R2, R3, and R4 draw heat away from the LTC9103s. Note that the voltage of the PWRIN pin changes based on the LTC9103 operating mode and its corresponding current consumption. If more current is consumed than the bypass resistors provide, the startup regulator maintains the voltage at 6V typical. The LTC9103 can operate without the pull-up resistors in space-constrained applications.

In applications with an external PWRIN supply, a 6.5V regulator provides an optimum voltage to override the internal 6V start-up regulator, while minimizing the LTC9103 device heating. The external supply may be shared across both LTC9103s.

A 3.3V power supply can be connected directly to the CAP3 pin, as shown in Figure 16. This provides the most power efficient sleep mode. When supplying external 3.3V power, tie the EXT3 pin to CAP3. This will disable the internal 3.3V regulator and prevent power back-feed. The 3.3V regulator must power up within $t_{CAP3EXT}$ specified in the Electrical Characteristics table.

If using the direct connection scheme, the 3.3V regulator that supplies the LTC9101-3 can also supply the LTC9103s. This is the preferred option when the LTC9101-3 and LTC9103 are on the same side of the system isolation barrier.

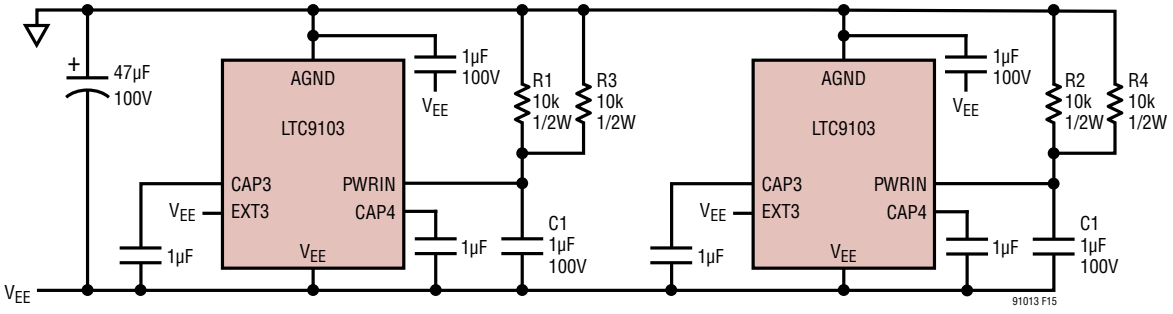


Figure 15. Power Supply Configuration with Internal 3.3V Supply

APPLICATIONS INFORMATION

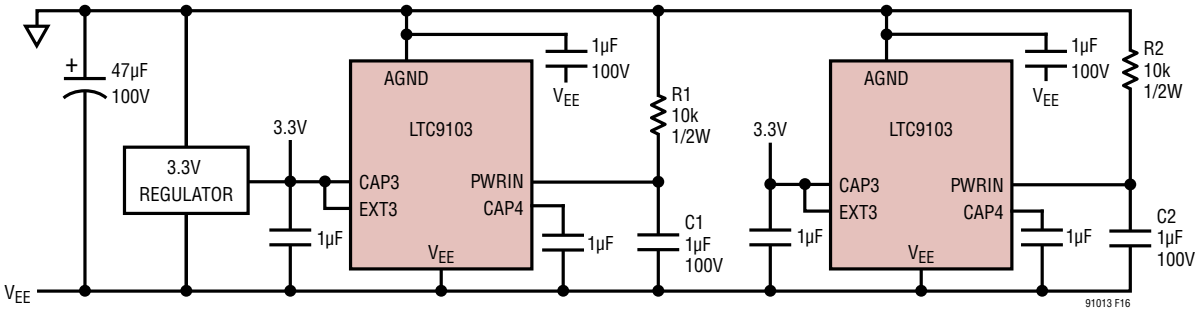


Figure 16. Power Supply Configuration with External 3.3V Regulators

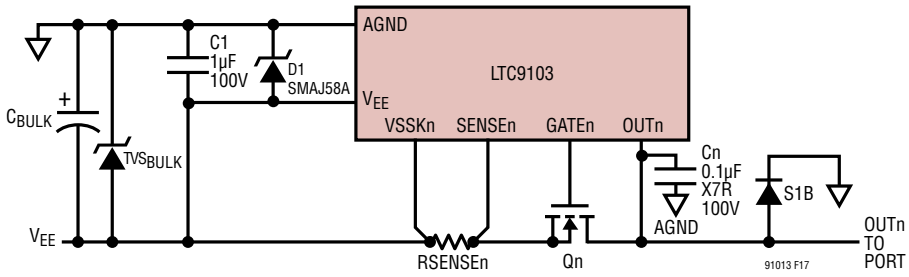


Figure 17. LTC9103 Surge Protection

Sense Resistors

The LTC9101-3/LTC9103 is designed for a low 0.1Ω current sense resistance per port, laid out as shown in the Layout Requirements section, Figure 18. In order to meet the I_{HOLD}, I_{CUT}, and I_{LIM} accuracy required by the IEEE specification, the sense resistors should have ±1% tolerance or better, and no more than ±200ppm/°C temperature coefficient.

Port Output Cap

Each port requires a 0.1µF cap across OUTn to AGND (see Figure 17) to keep the LTC9103 stable while in current limit during startup or overload. Common ceramic capacitors often have significant voltage coefficients; this means the capacitance is reduced as the applied voltage increases. To minimize this problem, X7R ceramic capacitors rated for at least 100V are recommended and must be located close to the LTC9103.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 17, are required at the main supply, at the LTC9103 supply pins, and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply and should be sized to accommodate system level surge requirements.

Across each LTC9103 AGND pin and V_{EE} pin is a SMAJ58A 58V TVS (D1) and a 1µF, 100V bypass capacitor (C1). These components must be placed close to the LTC9103 pins.

Each port requires an S1B clamp diode from OUTn to supply AGND. This diode steers harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance.

APPLICATIONS INFORMATION

High-Speed Data Interface

The communication between the LTC9101-3 and LTC9103s is through a high-speed data interface over either a proprietary isolation scheme or direct connection scheme.

In the proprietary isolation scheme, the LTC9101-3/LTC9103 chipset uses transformers to isolate the LTC9101-3 from one or two LTC9103s (see Figure 19). The transformers should be 10BASE-T or 10/100BASE-T with a 1:1 turns ratio. These transformers typically provide 1500V of isolation between the LTC9101-3 and the LTC9103s. Optimally, the selected transformers do not have common-mode chokes. If a transformer with chokes must be used, the chokes should be on the LTC9103 side of the isolation.

In the direct connection scheme, the LTC9101-3/LTC9103 chipset relies on pre-existing system isolation. In this scheme, the LTC9101-3 connects directly to one or two LTC9103s using a proprietary communication protocol (see Figure 20).

See High-Speed Data Interface Layout for layout requirements.

External MOSFET

Careful selection of the power MOSFET is critical to system reliability. Choosing a MOSFET requires extensive analysis and testing of the MOSFET SOA curve against the various PSE current limit conditions. ADI recommends the PSMN075-100MSE for PSEs configured to deliver up to 25.5W maximum port power This MOSFET is selected for its proven reliability in PoE applications. Contact ADI Applications before using a MOSFET other than one of these recommended parts.

Shift Register and LED Interface

The LTC9101-3 SD, PC, and SC pins must be buffered with a Schmitt trigger such as the 74LVC3G17 to drive downstream shift register(s) such as the 74HCT594. The outputs of the 74HCT594 can drive RJ45 port LEDs as shown in the front and back page Typical Application circuits.

LAYOUT REQUIREMENTS

Strict adherence to board layout, parts placement and routing requirements is critical for IEEE compliance, parametric measurement accuracy, system robustness and thermal dissipation. Refer to the EVAL-LTC9101-3-AZ-KIT demo kit for example layout references.

Kelvin Sense

Proper connection of the port current Kelvin sense lines is important for current threshold accuracy and IEEE compliance. Refer to Figure 18 for an example layout of these Kelvin sense lines. The LTC9103 VSSKn pin is Kelvin connected to the sense resistor (V_{EE} side) pad and is not other-wise connected to V_{EE} copper areas. Similarly, the LTC9103 SENSEn pin is Kelvin connected to the sense resistor (SENSEn side) pad and is not otherwise connected in the power path. Figure 18 shows the two Kelvin traces from the LTC9103 to the sense resistor (RSENSEn).

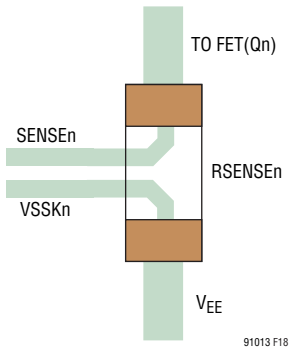


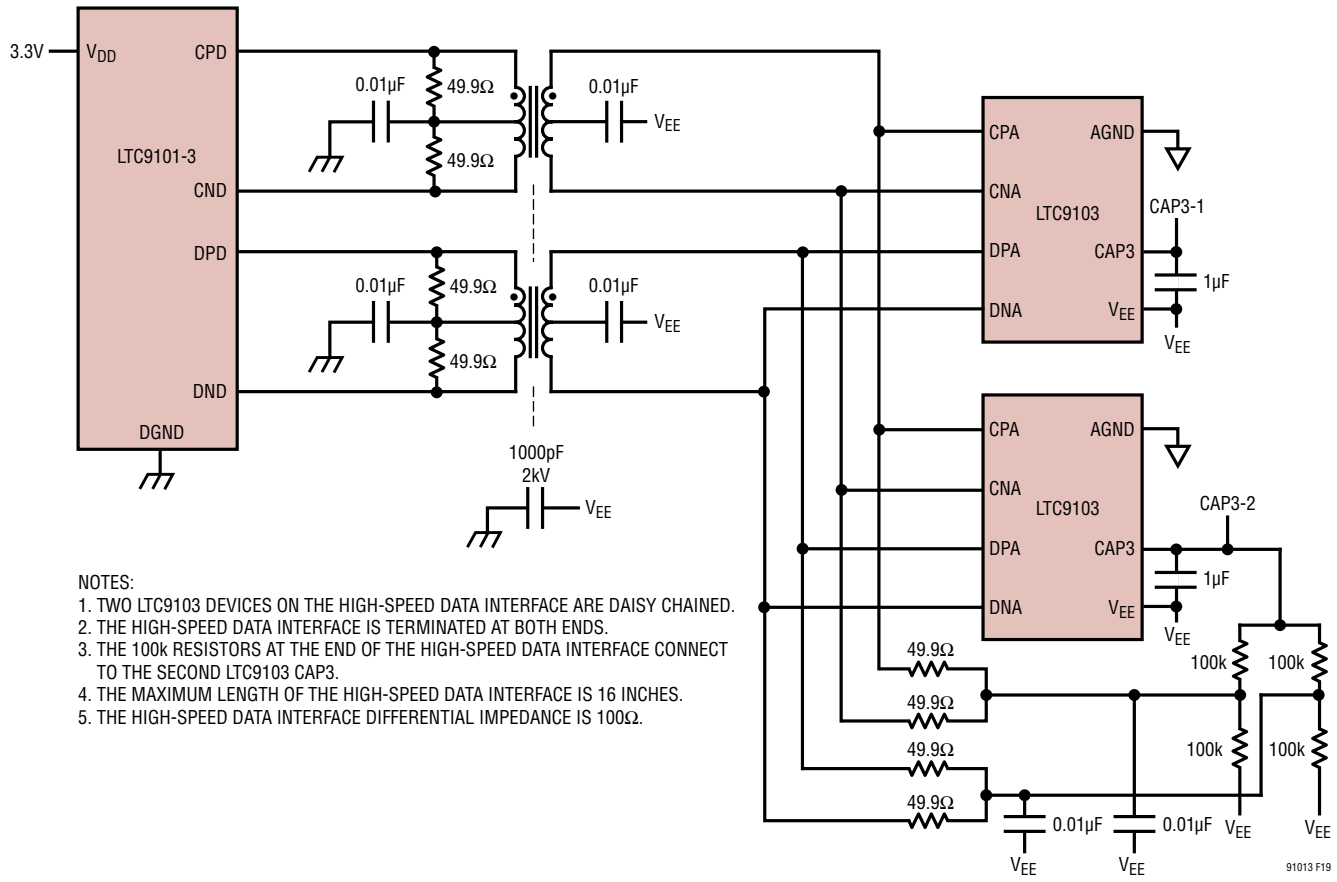
Figure 18. R_{SENSE} Kelvin Connections

APPLICATIONS INFORMATION

High-Speed Data Interface Layout

The LTC9101-3/LTC9103 chipset communicates across a proprietary high-speed, multi-drop data interface. This allows for a single LTC9101-3 to control up to two LTC9103s.

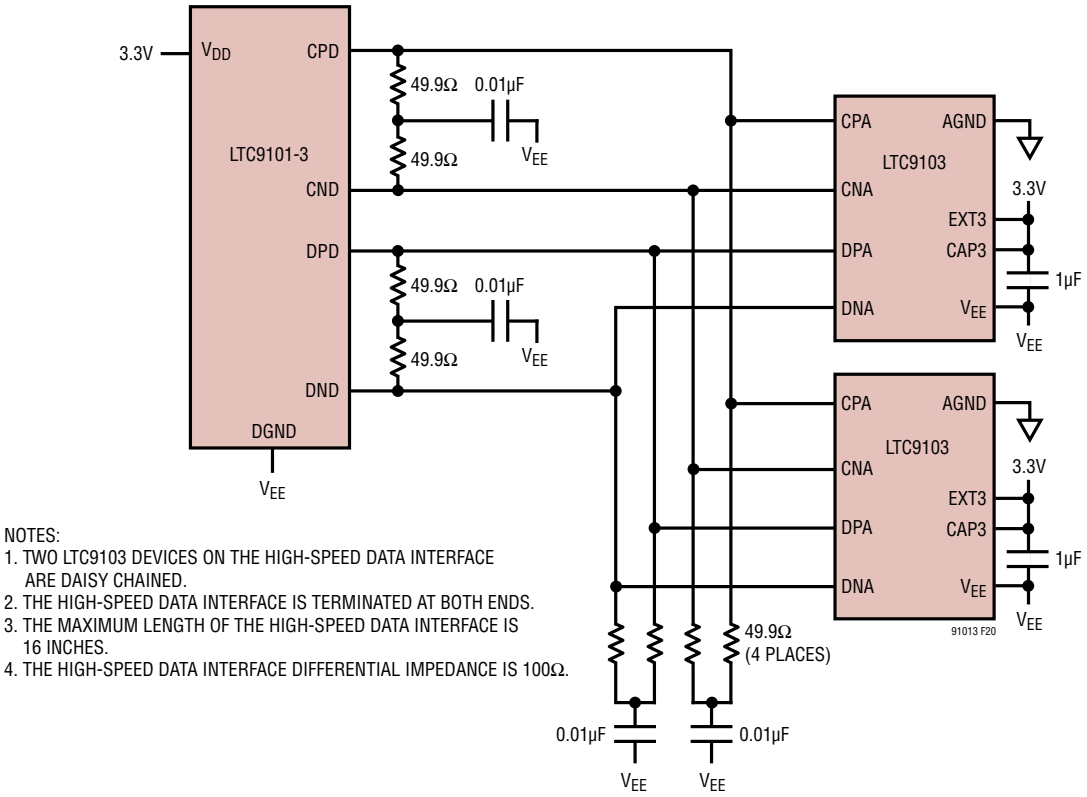
The data-lines require impedance matched traces to each LTC9103. The data bus termination resistors must be located at the LTC9103 farthest away from the isolation transformers. For isolated applications, the DC biasing resistors must connect to the LTC9103 CAP3 pin, farthest away from the isolation transformers. As shown in Figure 19 and Figure 20, design the interface with 100Ω differential transmission lines, and terminate 100Ω differentially. Limit the high-speed data interface line length to 16 inches. Minimize the transmission stubs between the LTC9103s and the high-speed data interface.



NOTES:
1. TWO LTC9103 DEVICES ON THE HIGH-SPEED DATA INTERFACE ARE DAISY CHAINED.
2. THE HIGH-SPEED DATA INTERFACE IS TERMINATED AT BOTH ENDS.
3. THE 100k RESISTORS AT THE END OF THE HIGH-SPEED DATA INTERFACE CONNECT TO THE SECOND LTC9103 CAP3.
4. THE MAXIMUM LENGTH OF THE HIGH-SPEED DATA INTERFACE IS 16 INCHES.
5. THE HIGH-SPEED DATA INTERFACE DIFFERENTIAL IMPEDANCE IS 100Ω.

Figure 19. LTC9101-3/LTC9103 Proprietary Isolation Scheme

APPLICATIONS INFORMATION

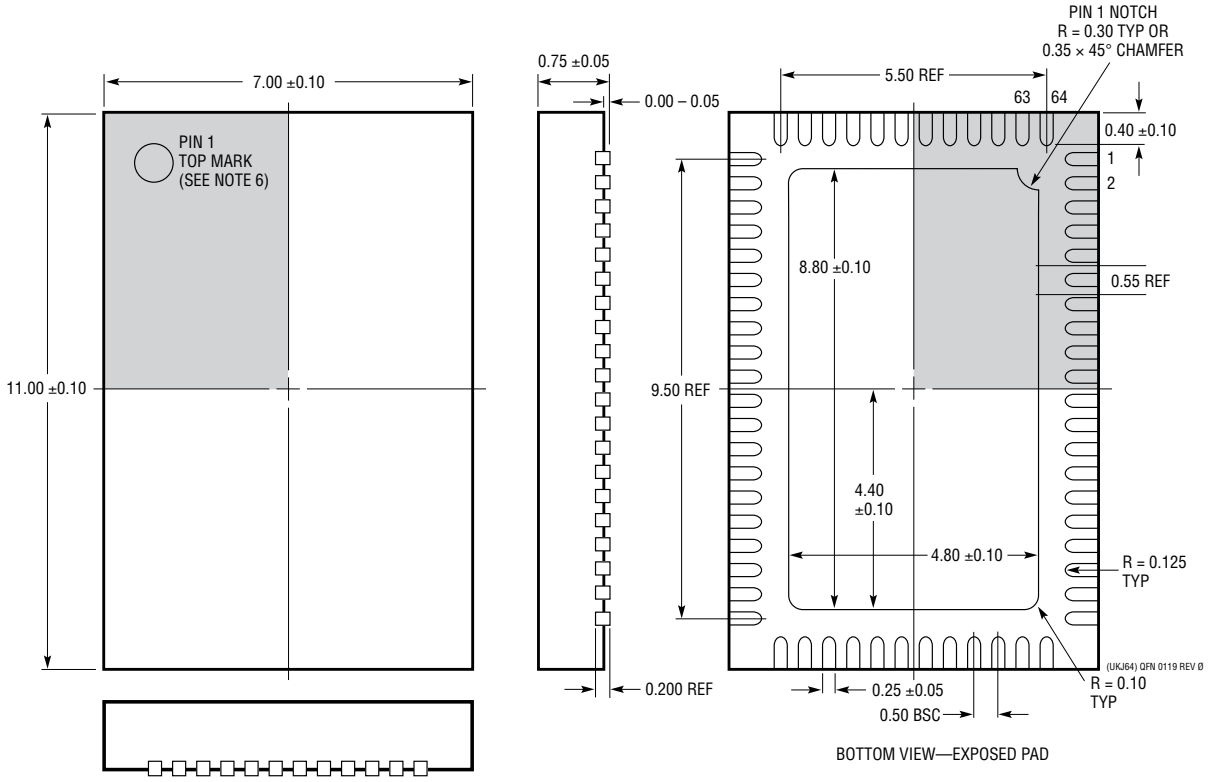


NOTES:
1. TWO LTC9103 DEVICES ON THE HIGH-SPEED DATA INTERFACE ARE DAISY CHAINED.
2. THE HIGH-SPEED DATA INTERFACE IS TERMINATED AT BOTH ENDS.
3. THE MAXIMUM LENGTH OF THE HIGH-SPEED DATA INTERFACE IS 16 INCHES.
4. THE HIGH-SPEED DATA INTERFACE DIFFERENTIAL IMPEDANCE IS 100Ω.

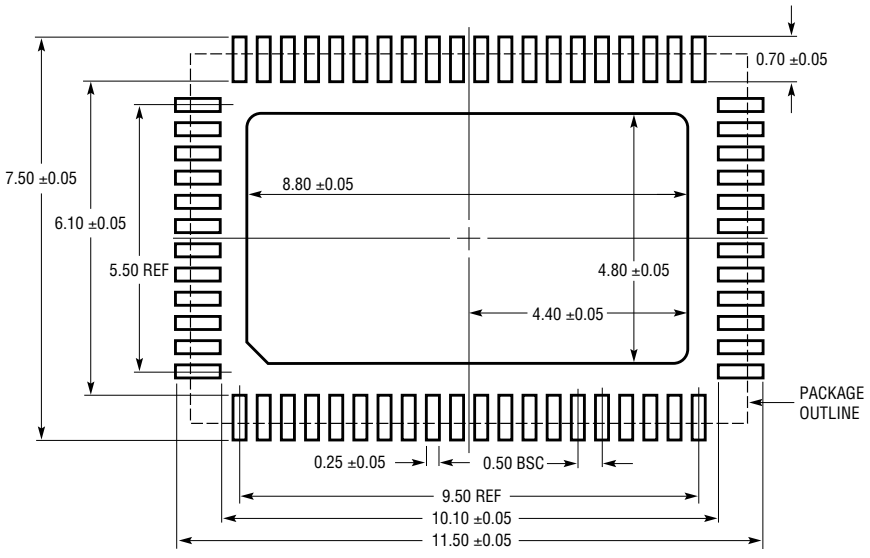
Figure 20. LTC9101-3/LTC9103 Proprietary Direct Connection Scheme

PACKAGE DESCRIPTION

UKJ Package
64-Lead Plastic QFN (7mm × 11mm)
(Reference LTC DWG # 05-08-1780 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

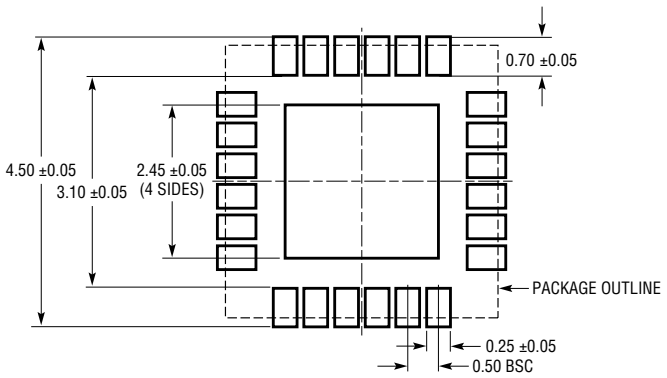


APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

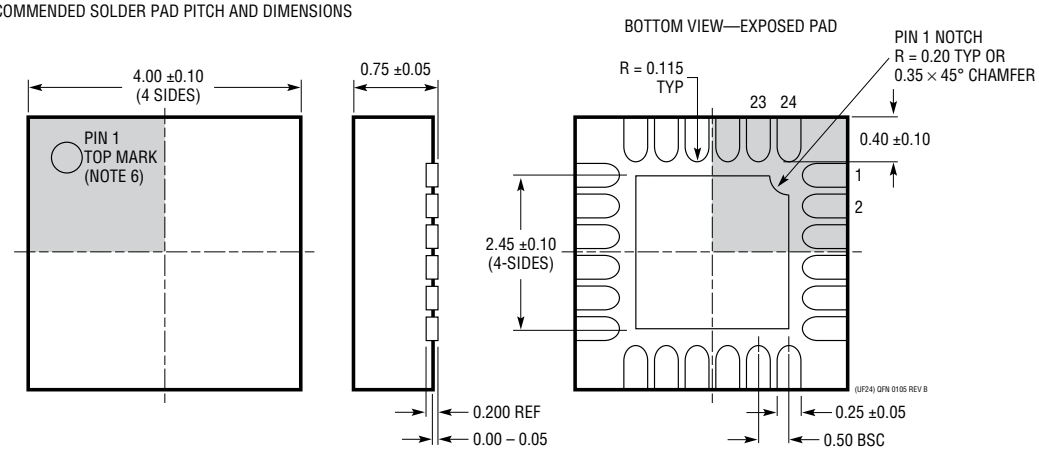
Rev. 0

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

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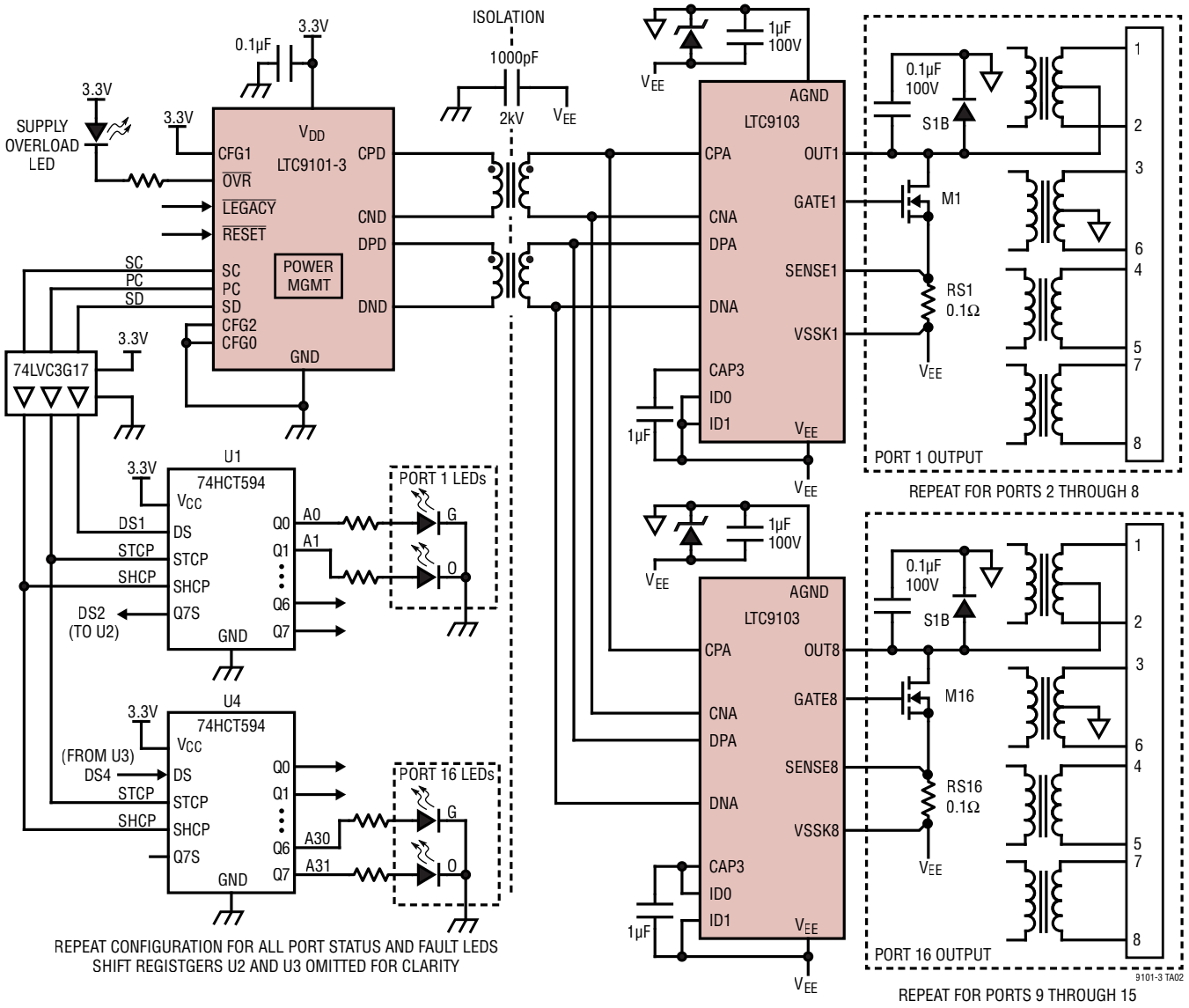
TYPICAL APPLICATION

16-Port Power-Managed IEEE 802.3at PSE with Port Status and Fault LEDs



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC9101-1/LTC9102/ LTC9103	48-Port IEEE 802.3bt PoE PSE Controller	Transformer Isolation, 14-bit current monitoring/programmable limit per port. Supports Type 1-4 PDs.
LTC4292/LTC4291-1	4-Port IEEE 802.3bt PoE PSE Controller	Transformer Isolation, 14-bit current monitoring per port with programmable current limit. Supports Type 1-4 PDs.
LT4294	IEEE 802.3bt PD Controller	External Switch, IEEE 802.3bt Support, Configurable Class and AUX Support
LTC4271/LTC4270	12-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs
LTC4267/LTC4267-1/ LTC4267-3	IEEE 802.3af PD Interface with Integrated Switching Regulator	Internal 100V, 400mA Switch, Dual Inrush Current, Programmable Class, 200/300kHz Constant Frequency PWM
LTC4278	IEEE 802.3at PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V, Aux Support

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