40V USB Type-C Power Delivery Buck-Boost Controller

FEATURES

- **Proprietary Low-EMI Buck-Boost Architecture**
- **Wide Input Range: 4V to 40V**
- **Synchronous Switching: Up to 98% Efficiency**
- **±1.5% Output Voltage Regulation**
- **Single Output supports 1 Type-C Port up to 100W**
- Output Channel Enable Function
- Programmable Switching Frequency with External Synchronization and Spread Spectrum
- Over-Current, Over-Voltage, Short-Circuit Protection
- Available in 28-Lead Side Solderable QFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive USB-C Power Delivery
- General Purpose Voltage Regulator

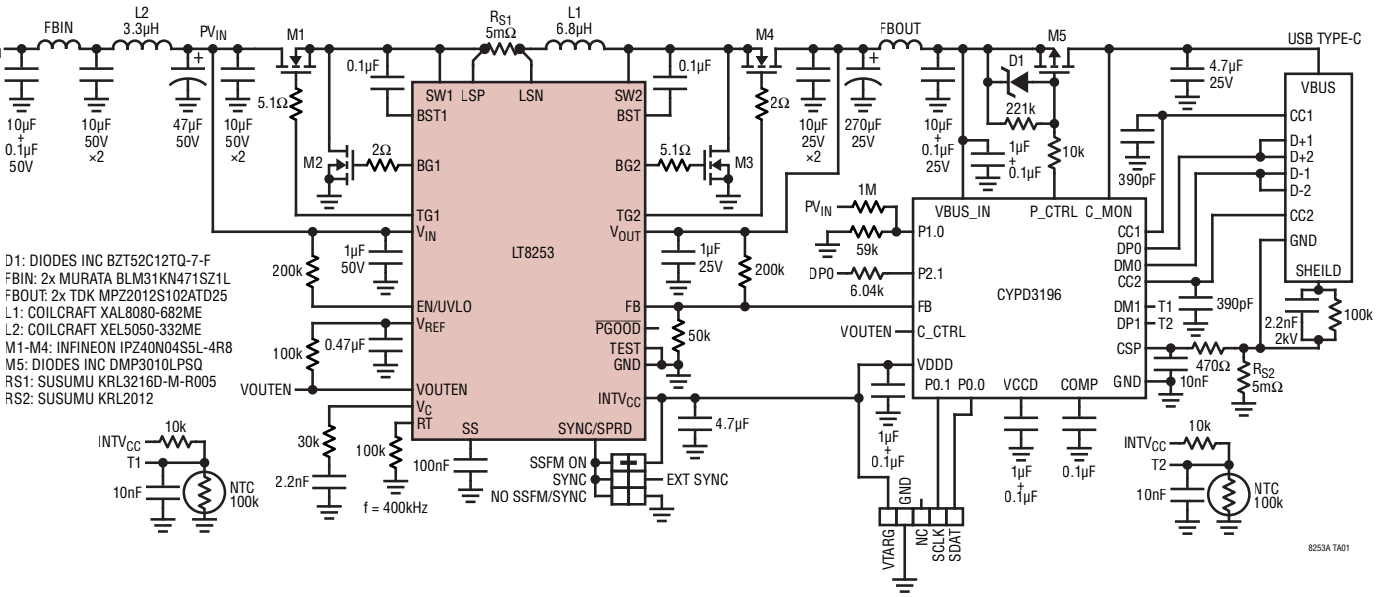
DESCRIPTION

The LT®8253/LT8253A are synchronous 4-switch buck-boost controllers optimized for automotive USB-C power delivery. The LT8253/53A are fully compliant to the USB Power Delivery (PD) specification when used in conjunction with a USB Type-C or PD port controller. The output voltage slew rate can be controlled through the FB pin. The LT8253 can deliver up to 100W output power with 98% peak efficiency when running below the AM band. The LT8253A can deliver up to 60W output power with 95% peak efficiency when running above the AM band.

The LT8253/8253A support single buck-boost output for 1 Type-C port with power good flag. Over-current, over-voltage, and short-circuit protections are also available.

TYPICAL APPLICATION

Automotive 60W USB-C Power Delivery Charger (400kHz)

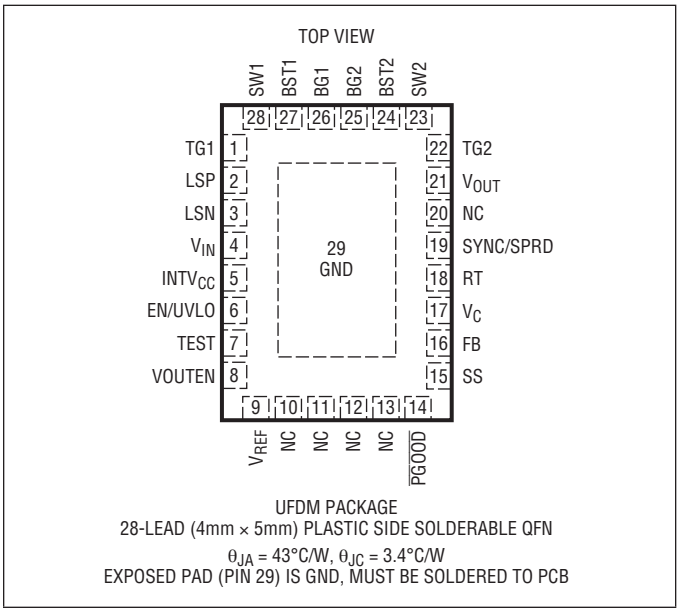


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO.....42V
V_{OUT}.....30V
BST1.....48V
BST2.....36V
SW1, LSP, LSN..... –6V to 42V
SW2..... –6V to 30V
$INTV_{CC}$, (BST1-SW1), (BST2-SW2) 6V
(BST1-LSP), (BST1-LSN) 6V
FB, VOUTEN, SYNC/SPRD, $\overline{PGOOD}$.....6V
Operating Junction Temperature Range (Notes 2, 3)
LT8253E, LT8253AE ..... –40°C to 125°C
LT8253J, LT8253AJ..... –40°C to 150°C
LT8253H, LT8353AH ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFDM PACKAGE
28-LEAD (4mm × 5mm) PLASTIC SIDE SOLDERABLE QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8253EUFDM#PBF	LT8253EUFDM#TRPBF	8253	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 125°C
LT8253JUFDM#PBF	LT8253JUFDM#TRPBF	8253	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8253HUFDM#PBF	LT8253HUFDM#TRPBF	8253	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8253AEUFDM#PBF	LT8253AEUFDM#TRPBF	8253A	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 125°C
LT8253AJUFDM#PBF	LT8253AJUFDM#TRPBF	8253A	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8253AHUFDM#PBF	LT8253AHUFDM#TRPBF	8253A	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8253JUFDM#WPBF	LT8253JUFDM#WTRPBF	8253	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8253HUFDM#WPBF	LT8253HUFDM#WTRPBF	8253	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8253AJUFDM#WPBF	LT8253AJUFDM#WTRPBF	8253A	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C
LT8253AHUFDM#WPBF	LT8253AHUFDM#WTRPBF	8253A	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by aLabel on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact yourLocal Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
	V_{IN} Operating Voltage Range		●	4		40	V
	V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.5V			1 2.1	2 3	µA mA
	V_{OUT} Voltage Range		●	1		25	V
Linear Regulators							
	$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = 20mA		4.8	5	5.2	V
	$INTV_{CC}$ Current Limit	V_{INTVCC} = 4.5V (LT8253) V_{INTVCC} = 4.5V (LT8253A)		80 110	110 145	160 190	mA mA
	$INTV_{CC}$ Undervoltage Lockout Threshold	Falling		3.44	3.54	3.64	V
	$INTV_{CC}$ Undervoltage Lockout Hysteresis				0.24		V
	V_{REF} Regulation Voltage	I_{VREF} = 100uA		1.96	2	2.04	V
	V_{REF} Current Limit	V_{REF} = 1.8V		2	2.5	3.2	mA
Control Inputs							
	EN/UVLO Shutdown Threshold			0.3	0.6	1	V
	EN/UVLO Enable Threshold	Falling		1.196	1.22	1.244	V
	EN/UVLO Enable Hysteresis				13		mV
	EN/UVLO Hysteresis Current	$V_{EN/UVLO}$ = 1.1V $V_{EN/UVLO}$ = 1.3V		2 –0.1	2.5 0	3 0.1	µA µA
	VOUTEN Threshold			1		1.6	V
Error Amplifier							
	FB Regulation Voltage		●	0.985	1	1.015	V
	FB Voltage Regulation Amplifier g_m				660		µS
Current Comparator							
	Maximum Current Sense Threshold $V_{(LSP-LSN)}$	Buck, V_{FB} = 0.8V Boost, V_{FB} = 0.8V		35 35	50 50	65 65	mV mV
Fault							
	FB Short Threshold	Falling		0.2	0.25	0.3	V
	FB Short Hysteresis			30	50	70	mV
	$\overline{PGOOD}$ Upper Threshold from V_{FB}	Rising		8	10	12	%
	$\overline{PGOOD}$ Lower Threshold from V_{FB}	Falling		–12	–10	–8	%
	$\overline{PGOOD}$ Pull-Down Resistance				100	200	Ω
	SS Hard Pull-Down Resistance	$V_{EN/UVLO}$ = 1.1V			100	200	Ω
	SS Pull-Up Current	V_{FB} = 0.4V, V_{SS} = 0V			12.5		µA
	SS Pull-Down Current	V_{FB} = 0.1V, V_{SS} = 2V			1.25		µA
	SS Fault High Threshold				1.7		V
	SS Fault Low Threshold				0.2		V
Oscillator							
	Oscillator Frequency	$V_{SYNC/SPRD}$ = 0V, RT = 100kΩ (LT8253) $V_{SYNC/SPRD}$ = 0V, RT = 59.0kΩ (LT8253A)	● ●	380 1900	400 2000	420 2100	kHz kHz
	SYNC/SPRD Clock SYNC Frequency	(LT8253) (LT8253A)		150 600		650 2000	kHz kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	SYNC/SPRD Clock SYNC Threshold			0.4		1.5	V
NMOS Drivers							
	TG1, TG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	$V_{(BST-SW)}$ = 5V			2.6 1.7		Ω Ω
	BG1, BG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	V_{INTVCC} = 5V			 3 1.2		Ω Ω
	TG Off to BG On Delay Time	LT8253 LT8253A			60 25		ns ns
	BG Off to TG On Delay Time	LT8253 LT8253A			60 25		ns ns

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LT8253E/LT8253AE are guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8253J/LT8253AJ and LT8253H/LT8253AH are guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3. The LT8253/LT8253A include overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

PIN FUNCTIONS

BG1: Buck Side Bottom Gate Drive. Drives the gate of buck side bottom N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

BG2: Boost Side Bottom Gate Drive. Drives the gate of boost side bottom N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

BST1: Buck Side Bootstrap Floating Driver Supply. The BST1 pin has an integrated bootstrap diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW1 pin.

BST2: Boost Side Bootstrap Floating Driver Supply. The BST2 pin has an integrated bootstrap diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW2 pin.

EN/UVLO: Enable and Undervoltage Lockout. Force the pin below 0.3V to shut down the part and force the pin above 1.23V for normal operation. The 1.22V falling threshold and 2.5µA pull-down current can be used to program V_{IN} UVLO with hysteresis. If neither function is used, tie this pin directly to V_{IN}.

FB: Voltage Loop Feedback Input. The FB pin is used for output voltage regulation and output fault protection.

GND (Exposed Pad): Ground. Solder the exposed pad directly to the ground plane.

$INTV_{CC}$: Internal 5V Linear Regulator Output. The $INTV_{CC}$ linear regulator is supplied from the V_{IN} pin and powers the internal control circuitry and gate drivers. Locally bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

LSN: Negative Terminal of the Buck Side Inductor Current Sense Resistor. Ensure accurate current sense with Kelvin connection.

LSP: Positive Terminal of the Buck Side Inductor Current Sense Resistor. Ensure accurate current sense with Kelvin connection.

$\overline{PGOOD}$: Power Good Open Drain Output. The $\overline{PGOOD}$ pin is pulled low when the FB pin is within ±10% of its regulation voltage. To function, the pin requires an external pull-up resistor.

RT: Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency.

SS: Soft-Start Timer Setting. The SS pin is used to set soft-start timer by connecting a capacitor to ground. An internal 12.5µA pull-up current charging the external SS capacitor gradually ramps up FB regulation voltage.

SW1: Buck Side Switch Node.

SW2: Boost Side Switch Node.

SYNC/SPRD: External Clock Frequency Synchronization or Spread Spectrum. Ground this pin for switching at internal oscillator frequency. Apply a clock signal for external frequency synchronization. Tie to $INTV_{CC}$ for spread spectrum frequency modulation.

TEST: Factory Test. This pin is for factory testing purpose only and must be directly connected to ground for proper operation.

TG1: Buck Side Top Gate Drive. Drives the gate of buck side top N-Channel MOSFET with a voltage swing from SW1 to BST1.

TG2: Boost Side Top Gate Drive. Drives the gate of boost side top N-Channel MOSFET with a voltage swing from SW2 to BST2.

VC: Error Amplifier Output. The VC pin is used to compensate the control loop with an external RC network.

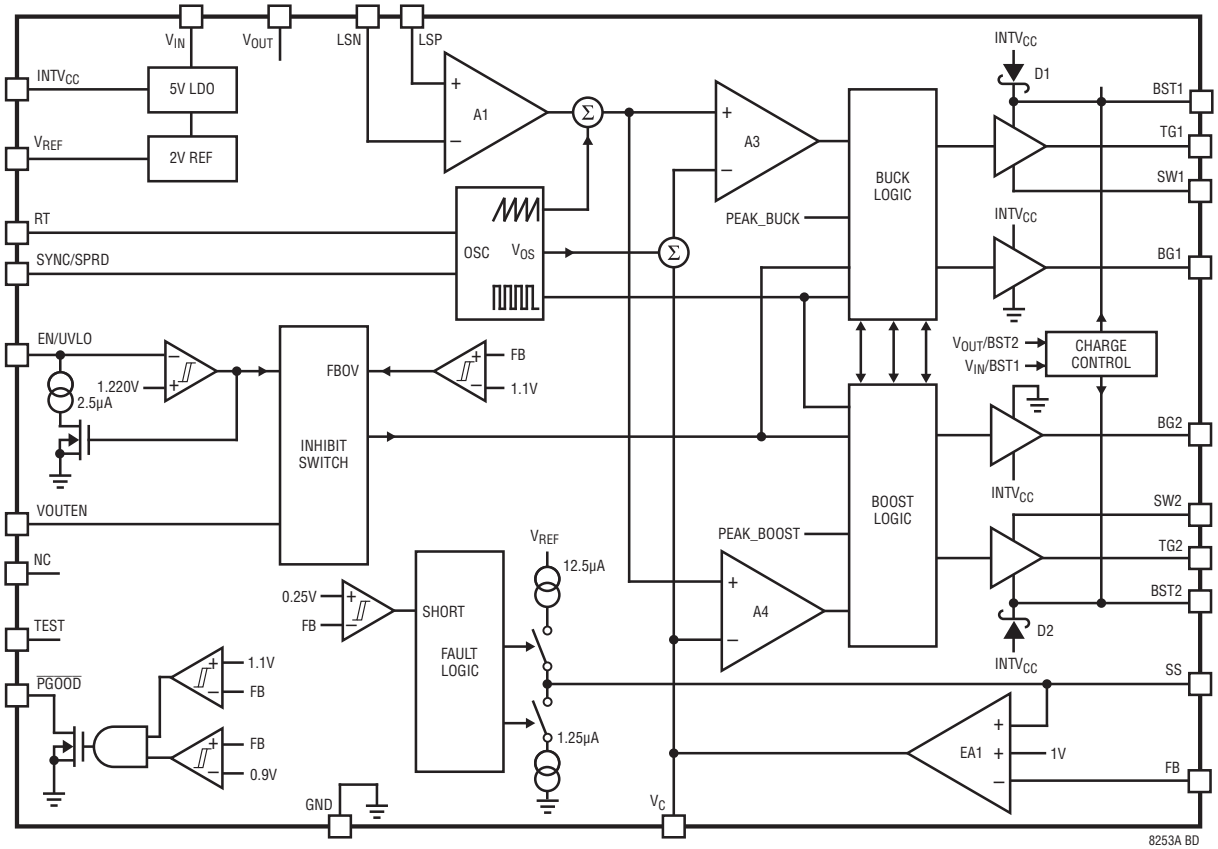
V_{IN}: Input Supply. The V_{IN} pin must be tied to the power input to determine its operation regions. Locally bypass this pin to ground with a minimum 0.1µF ceramic capacitor.

V_{OUT}: Output Pin. The V_{OUT} pin must be tied to the power output to determine its operation regions. Locally bypass this pin to ground with a minimum 0.1µF ceramic capacitor.

VOUTEN: Output Enable. The VOUTEN pin is used to enable buck-boost switching and deliver output power.

V_{REF}: Voltage Reference Output. The V_{REF} pin provides an accurate 2V reference capable of supplying 1mA current. Locally bypass this pin to ground with a 0.47µF ceramic capacitor.

BLOCK DIAGRAM



OPERATION

The LT8253/LT8253A are current mode DC/DC controllers that can regulate output voltage from an input voltage above, below, or equal to the output voltage. The proprietary peak-buck peak-boost current mode control scheme uses a single current sense resistor and provides smooth transition between buck region, buck-boost region, and boost region. Its operation is best understood by referring to the Block Diagram.

Power Switch Control

Figure 1 shows a simplified diagram of how the four power switches A, B, C, and D are connected to the inductor L, the current sense resistor R_{SENSE}, power input V_{IN}, power output V_{OUT}, and ground. The current sense resistor R_{SENSE} connected to the LSP and LSN pins provides inductor current information for both peak current mode control and reverse current detection in buck region, buck-boost region, and boost region.

There are total four states: (1) peak-buck current mode control in buck region, (2) peak-buck current mode control in buck-boost region, (3) peak-boost current mode control in buck-boost region, and (4) peak-boost current mode control in boost region. The following sections give detailed description for each state with waveforms, in which the shoot-through protection dead time between switches A and B, between switches C and D are ignored for simplification.

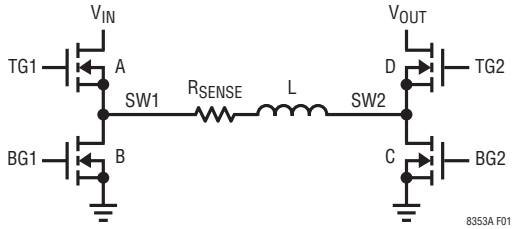


Figure 1. Simplified Diagram of the Power Switches

OPERATION

(1) Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

When V_{IN} is much higher than V_{OUT}, the LT8253/LT8253A use peak-buck current mode control in buck region (Figure 2). Switch C is always off and switch D is always on. At the beginning of every cycle, switch A is turned on and the inductor current ramps up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator.

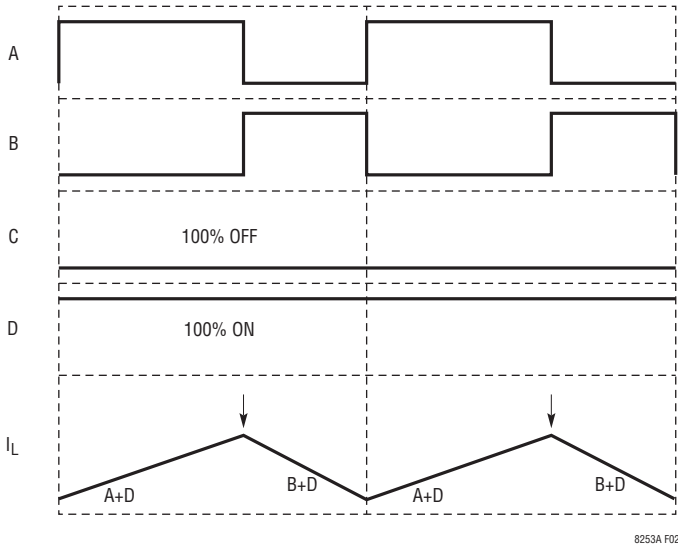


Figure 2. Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

(2) Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

When V_{IN} is slightly higher than V_{OUT}, the LT8253/LT8253A use peak-buck current mode control in buck-boost region (Figure 3). Switch C is always turned on for the beginning preset cycle and switch D is always turned on for the remaining cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. After preset cycle, switch C is turned off and switch D is turned on, and the inductor keeps ramping up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle.

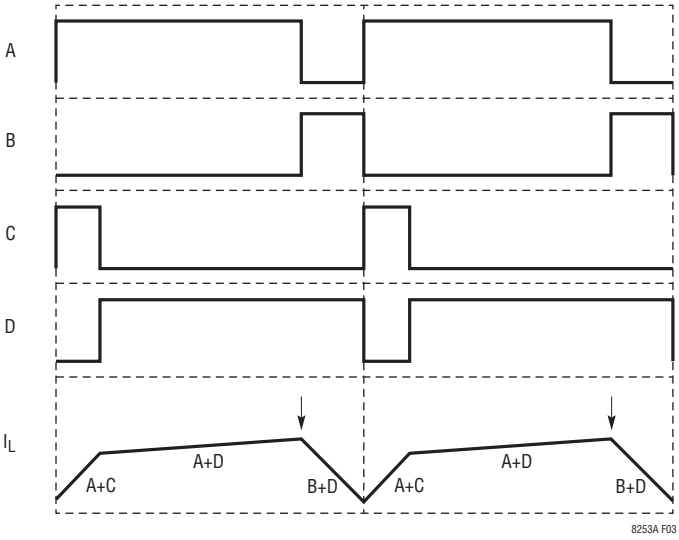


Figure 3. Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

OPERATION

(3) Peak-Boost in Buck-Boost Region (V_{IN} <~ V_{OUT})

When V_{IN} is slightly lower than V_{OUT}, the LT8253/LT8253A use peak-boost current mode control in buck-boost region (Figure 4). Switch A is always turned on for the beginning preset cycle and switch B is always turned on for the remaining cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. After preset cycle, switch A is turned off and switch B is turned on for the rest of the cycle.

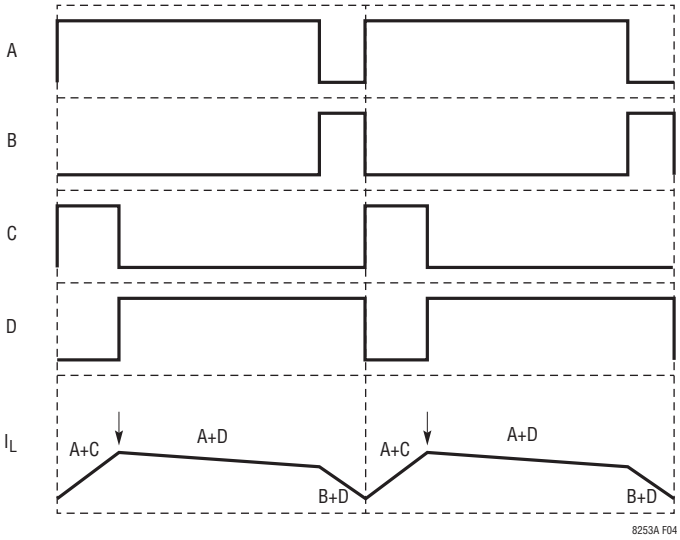


Figure 4. Peak-Boost in Buck-Boost Region (V_{IN} <~ V_{OUT})

(4) Peak-Boost in Boost Region (V_{IN} << V_{OUT})

When V_{IN} is much lower than V_{OUT}, the LT8253/LT8253A use peak-boost current mode control in boost region (Figure 5). Switch A is always on and switch B is always off. At the beginning of every cycle, switch C is turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

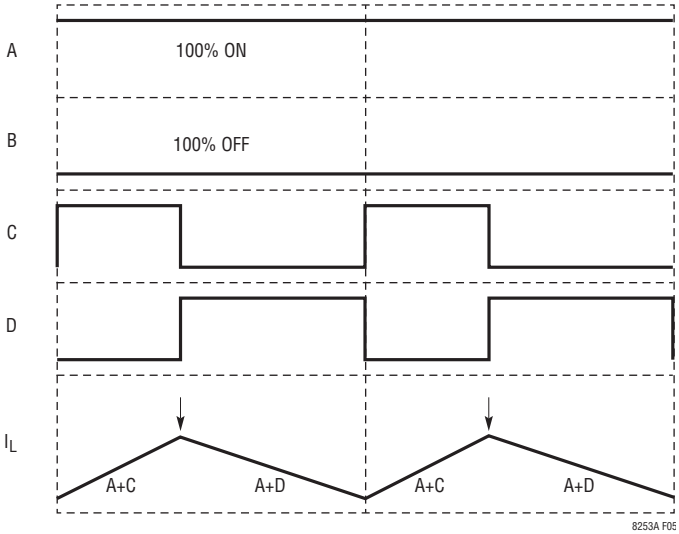


Figure 5. Peak-Boost in Boost Region (V_{IN} << V_{OUT})

OPERATION

Main Control Loop

The LT8253/LT8253A are fixed frequency current mode controllers. The inductor current is sensed through the inductor sense resistor between the LSP and LSN pins. The current sense voltage is gained up by amplifier A1 and added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A3 and boost current comparator A4. The negative terminals of A3 and A4 are controlled by the voltage on the V_C pin, which is the output of error amplifier EA1.

Depending on the state of the peak-buck peak-boost current mode control, either the buck logic or the boost logic is controlling the four power switches so that the FB voltage is regulated to 1V.

Light Load Current Operation

At light load, the LT8253/LT8253A typically run at discontinuous conduction mode, to maintain the regulation and improve the efficiency.

Shutdown and Power-On-Reset

The LT8253/LT8253A enter shutdown mode and drain less than 2μA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (1V maximum), the LT8253/LT8253A wake up startup circuitry, generate bandgap reference, and power up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. Then the LT8253/LT8253A enter undervoltage lockout (UVLO) mode with a hysteresis current (2.5μA typical) pulled into the EN/UVLO pin. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (3.78V typical), the EN/UVLO pin passes its rising enable threshold (1.233V typical), and the junction temperature is less than its thermal shutdown (165°C typical), the LT8253/LT8253A enter enable mode, in which the EN/UVLO hysteresis current is turned off and the voltage reference V_{REF} is being charged up from ground. From the time of entering enable mode to the time of V_{REF} passing its rising UVLO threshold (1.89V typical), the LT8253/LT8253A are going through a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions. After the POR, the LT8253/LT8253A start switching.

OPERATION

Start-Up and Fault Protection

Figure 6 shows the start-up and fault sequence for the LT8253/LT8253A. During the POR state, the SS pin is hard pulled down with a 100Ω to ground. In a pre-biased condition, the SS pin has to be pulled below 0.2V to enter the INIT state, where the LT8253/LT8253A wait 10µs so that the SS pin can be fully discharged to ground. After the 10µs, the LT8253/LT8253A enter the UP/PRE state when the VOUTEN signal goes high.

During the UP/PRE state, the SS pin is charged up by a 12.5µA pull-up current while the switching is disabled. Once the SS pin is charged above 0.25V, the LT8253/LT8253A enter the UP/TRY state. After 10µs in the UP/TRY state, the LT8253/LT8253A enter the UP/RUN state.

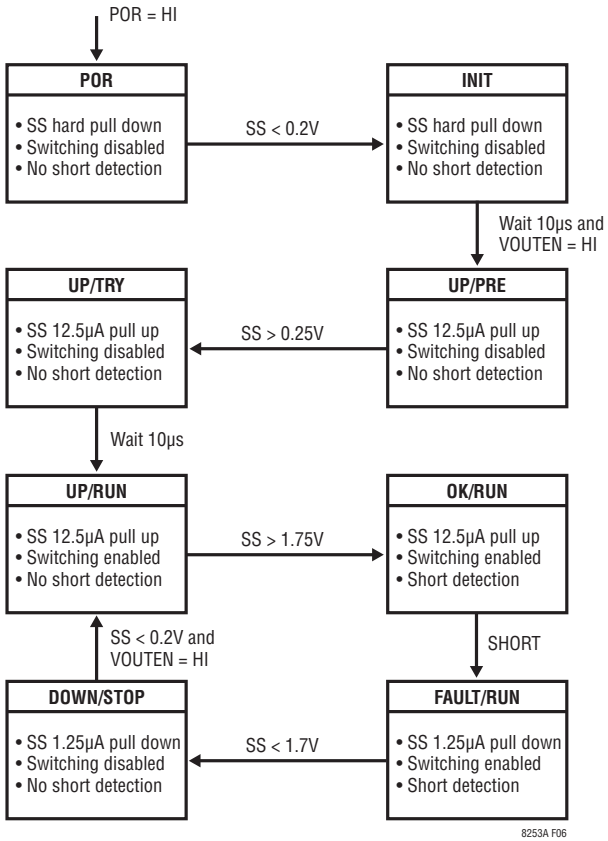


Figure 6. Start-Up and Fault Sequence

During the UP/RUN state, the switching is enabled and the start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT8253/LT8253A regulate the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to program soft-start by connecting an external capacitor from the SS pin to GND. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V and above, the output voltage V_{OUT} rises smoothly to its final regulation voltage.

Once the SS pin is charged above 1.75V, the LT8253/LT8253A enter the OK/RUN state, where the output short detection is activated. The output short means V_{FB} < 0.25V. When the output short happens, the LT8253/LT8253A enter the FAULT/RUN state, where a 1.25µA pull-down current slowly discharges the SS pin with the other conditions the same as the OK/RUN state. Once the SS pin is discharged below 1.7V, the LT8253/LT8253A enter the DOWN/STOP state, where the switching is disabled and the short detection is deactivated with the previous fault latched. Once the SS pin is discharged below 0.2V and the VOUTEN signal is still high, the LT8253/LT8253A go back to the UP/RUN state.

In an output short condition, the LT8253/LT8253A can be set to hiccup, latch-off, or keep-running fault protection mode with a resistor between the SS and V_{REF} pins. Without any resistor, the LT8253/LT8253A will hiccup between 0.2V and 1.75V and go around the UP/RUN, OK/RUN, FAULT/RUN, and DOWN/STOP states until the fault condition is cleared. With a 499k resistor, the LT8253/LT8253A will latch off until the EN/UVLO is toggled. With a 100kΩ resistor, the LT8253/LT8253A will keep running regardless of the fault.The front page shows a typical LT8253/LT8253A application circuit. This Applications Information section serves as a guideline of selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Switching Frequency Selection

The LT8253/LT8253A use a constant frequency control scheme, 150kHz-650kHz for LT8253 and 600kHz-2MHz

APPLICATIONS INFORMATION

for LT8253A. Selection of the switching frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size.

In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The switching frequency of the LT8253/LT8253A can be set by the internal oscillator. With the SYNC/SPRD pin pulled to ground, the switching frequency is set by a resistor from the RT pin to ground. Table 1 and Table 2 show R_T resistor values of common switching frequencies for LT8253 and LT8253A, respectively.

Table 1. LT8253 Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (kHz)	R_T (k)
150	309
200	226
300	140
400	100
500	75
600	59
650	51.1

Table 2. LT8253A Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (MHz)	R_T (k)
0.6	267
0.8	191
1.0	147
1.2	118
1.4	97.6
1.6	82.5
1.8	66.5
2.0	59.0

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT8253/LT8253A implement a triangle spread spectrum frequency modulation scheme. With the SYNC/SPRD pin tied to $INTV_{CC}$, the LT8253 spreads its switching frequency ±15% around and the LT8253A spreads its switching frequency 25% above the internal oscillator frequency.

Frequency Synchronization

The LT8253/LT8253A switching frequency can be synchronized to an external clock using the SYNC/SPRD pin. Driving the SYNC/SPRD with a 50% duty cycle waveform is always a good choice, otherwise maintain the duty cycle between 10% and 90%.

Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $V_{IN(MAX)}$, and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $V_{IN(MIN)}$. For any given ripple allowance set by customers, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L\% \bullet V_{IN(MAX)}}$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L\% \bullet V_{OUT}^2}$$

where:

$$\Delta I_L\% = \frac{\Delta I_L}{I_{L(AVG)}}$$

f is switching frequency

$V_{IN(MIN)}$ is minimum input voltage

$V_{IN(MAX)}$ is maximum input voltage

V_{OUT} is output voltage

$I_{OUT(MAX)}$ is maximum output current

APPLICATIONS INFORMATION

Slope compensation provides stability in constant frequency current mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability when duty cycles are larger than 50% can be calculated as:

$$L > \frac{10 \bullet V_{OUT} \bullet R_{SENSE}}{f}$$

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

R_{SENSE} Selection and Maximum Output Current

R_{SENSE} is chosen based on the required output current. The duty cycle independent maximum current sense thresholds (50mV in peak-buck and 50mV in peak-boost) set the maximum inductor peak current in buck region, buck-boost region, and boost region.

In boost region, the lowest maximum average load current happens at $V_{IN(MIN)}$ and can be calculated as:

$$I_{OUT(MAX\_BOOST)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BOOST)}}{2} \right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

where $\Delta I_{L(BOOST)}$ is peak-to-peak inductor ripple current in boost region and can be calculated as:

$$\Delta I_{L(BOOST)} = \frac{V_{IN(MIN)} \bullet \left(V_{OUT} - V_{IN(MIN)} \right)}{f \bullet L \bullet V_{OUT}}$$

In buck region, the lowest maximum average load current happens at $V_{IN(MAX)}$ and can be calculated as:

$$I_{OUT(MAX\_BUCK)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BUCK)}}{2} \right)$$

where $\Delta I_{L(BUCK)}$ is peak-to-peak inductor ripple current in buck region and can be calculated as:

$$\Delta I_{L(BUCK)} = \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT} \right)}{f \bullet L \bullet V_{IN(MAX)}}$$

The maximum current sense R_{SENSE} in boost region is:

$$R_{SENSE(BOOST)} = \frac{2 \bullet 50mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX)} \bullet V_{OUT} + \Delta I_{L(BOOST)} \bullet V_{IN(MIN)}}$$

The maximum current sense R_{SENSE} in buck region is

$$R_{SENSE(BUCK)} = \frac{2 \bullet 50mV}{2 \bullet I_{OUT(MAX)} + \Delta I_{L(BUCK)}}$$

The final R_{SENSE} value should be lower than the calculated R_{SENSE} in both buck and boost regions. A 20% to 30% margin is usually recommended. Always choose a low ESL current sense resistor.

Power MOSFET Selection

The LT8253/LT8253A require four external N-channel power MOSFETs, two for the top switches (switches A and D shown in Figure 1) and two for the bottom switches (switches B and C shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

To achieve 2MHz operation, the power MOSFET selection is critical. With typical 25ns shoot-through protection deadtime, high performance power MOSFETs with low Q_g and low $R_{DS(ON)}$ must be used.

Since the gate drive voltage is set by the 5V $INTV_{CC}$ supply, logic-level threshold MOSFETs must be used in LT8253/LT8253A applications. Switching four MOSFETs at higher frequency like 2MHz, the substantial gate charge current from $INTV_{CC}$ can be estimated as:

$$I_{INTVCC} = f \bullet \left(Q_{gA} + Q_{gB} + Q_{gC} + Q_{gD} \right)$$

where:

f is the switching frequency

Q_{gA}, Q_{gB}, Q_{gC}, Q_{gD} are the total gate charges of MOSFETs A, B, C, D

Make sure the total required $INTV_{CC}$ current does not exceed the $INTV_{CC}$ current limit in the datasheet. Typically, MOSFETs with less than 10nC Q_g are recommended.

APPLICATIONS INFORMATION

The LT8253/LT8253A use the V_{IN}/V_{OUT} ratio to transition between modes and regions. Bigger IR drop in the power path caused by improper MOSFET and inductor selection may prevent the LT8253/LT8253A from smooth transition. To ensure smooth transitions between buck, buck-boost, and boost modes of operation, choose low $R_{DS(ON)}$ MOSFETs and low DCR inductor to satisfy:

$$I_{OUT(MAX)} \leq \frac{0.025 \bullet V_{OUT}}{R_{A,B} + R_{C,D} + R_{SENSE} + R_L}$$

where:

$R_{A,B}$ is the maximum $R_{DS(ON)}$ of MOSFETs A or B at 25°C

$R_{C,D}$ is the maximum $R_{DS(ON)}$ of MOSFETs C or D at 25°C

R_L is the maximum DCR resistor of inductor at 25°C

The $R_{DS(ON)}$ and DCR increase at higher junction temperatures and the process variation have been included in the calculation above.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A(BOOST)} = \left(\frac{I_{OUT(MAX)} \bullet V_{OUT}}{V_{IN}} \right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where ρ_T is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C as shown in Figure 7. For a maximum junction temperature of 125°C, using a value of ρ_T = 1.5 is reasonable.

Switch B operates in buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Switch C operates in boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C(BOOST)} = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

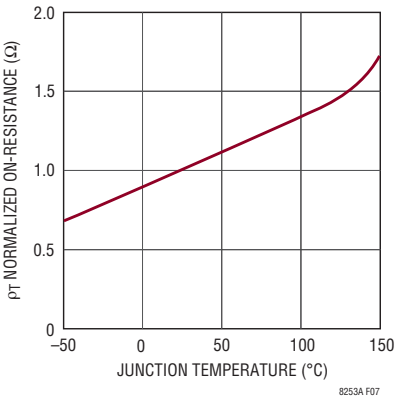


Figure 7. Normalized $R_{DS(ON)}$ vs Temperature

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D(BOOST)} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The junction-to-ambient thermal resistance $R_{TH(JA)}$ includes the junction-to-case thermal resistance $R_{TH(JC)}$ and the case-to-ambient thermal resistance $R_{TH(CA)}$. This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. Ceramic capacitors, of at least 1µF, should also be placed from V_{IN} to GND and V_{OUT} to GND as close to the LT8253/LT8253A pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance C_{IN}: Discontinuous input current is highest in the buck region due to the switch A toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Output Capacitance C_{OUT}: Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{8 \bullet L \bullet f^2 \bullet C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \bullet I_{OUT(MAX)}}{V_{IN(MIN)}} \bullet ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{L \bullet f} \bullet ESR$$

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ powers internal circuitry and gate drivers in the LT8253/LT8253A. The $INTV_{CC}$ regulator must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good local bypass is necessary to supply the high transient current required by MOSFET gate drivers.

Higher input voltage applications with large MOSFETs being driven at higher switching frequencies may cause the maximum junction temperature rating for the LT8253/LT8253A to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ also needs to be taken into account for the power dissipation calculation. The total LT8253/LT8253A power dissipation in this case is $V_{IN} \bullet I_{INTVCC}$, and overall efficiency is lowered. The junction temperature can be estimated by using the equation:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where θ_{JA} (in °C/W) is the package thermal resistance.

APPLICATIONS INFORMATION

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V_{IN}.

Top Gate MOSFET Driver Supply (C_{BST1}, C_{BST2})

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged through internal bootstrap diodes when the respective top MOSFET is turned off. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. The bootstrap capacitors C_{BST1} and C_{BST2}, need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.220V with 13mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.220V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.233V \bullet \frac{R1+R2}{R2} + 2.5\mu A \bullet R1$$

$$V_{IN(UVLO-)} = 1.220V \bullet \frac{R1+R2}{R2}$$

Figure 8 shows the implementation of external shut-down control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT8253/LT8253A in shutdown with quiescent current less than 2µA.

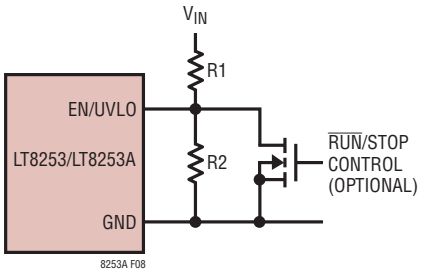


Figure 8. V_{IN} Undervoltage Lockout (UVLO)

Programming Output Voltage and Thresholds

The LT8253/LT8253A have a voltage feedback pin FB that can set the output voltage with R3 and R4 (Figure 9) according to the following equation:

$$V_{OUT} = 1V \bullet \frac{R3+R4}{R4}$$

In addition, the FB pin also sets output overvoltage threshold, output power good thresholds, and output short threshold. For an application with small output capacitors, the output voltage may overshoot a lot during load transient event. Once the FB pin hits its overvoltage

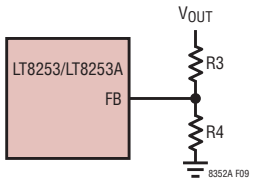


Figure 9. Feedback Resistor Connection

threshold 1.1V, the LT8253/LT8253A stop switching by turning off TG1, BG1, TG2, and BG2. The output overvoltage threshold can be set as:

$$V_{OUT(OVP)} = 1.1V \bullet \frac{R3+R4}{R4}$$

To provide the output short-circuit detection and protection, the output short falling threshold can be set as:

$$V_{OUT(SHORT)} = 0.25V \bullet \frac{R3+R4}{R4}$$

Power GOOD ($\overline{PGOOD}$) Pin

The LT8253/LT8253A provide an open-drain status pin, $\overline{PGOOD}$, which is pulled low when V_{FB} is within ±10% of the 1.00V regulation voltage. The $\overline{PGOOD}$ pin is allowed to be pulled up by an external resistor to $INTV_{CC}$ or an external voltage source of up to 6V.

APPLICATIONS INFORMATION

Soft-Start and Short-Circuit Protection

As shown in Figure 6 and explained in the Operation section, the SS pin can be used to program the output voltage soft-start by connecting an external capacitor from the SS pin to ground. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly into its final voltage regulation. The soft-start time can be calculated as:

$$t_{SS} = 1V \bullet \frac{C_{SS}}{12.5\mu A}$$

Make sure the C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin for a well-controlled output voltage soft-start.

The SS pin is also used as a fault timer. Once an output short-circuit fault is detected, a 1.25µA pull-down current source is activated. Using a single resistor from the SS pin to the V_{REF} pin, the LT8253/LT8253A can be set to three different fault protection modes: hiccup (no resistor), latch-off (499k), and keep-running (100k).

With a 100k resistor in keep-running mode, the LT8253/LT8253A continue switching normally and regulates the current into ground. With a 499k resistor in latch-off mode, the LT8253/LT8253A stop switching until the EN/UVLO pin is pulled low and high to restart. With no resistor in hiccup mode, the LT8253/LT8253A enter low duty cycle auto-retry operation. The 1.25µA pull-down current discharges the SS pin to 0.2V and then 12.5µA pull-up current charges the SS pin up. If the output short-circuit condition has not been removed when the SS pin reaches 1.75V, the 1.25µA pull-down current turns on again, initiating a new hiccup cycle. This will continue until the fault is removed. Once the output short-circuit condition is removed, the output will have a smooth short-circuit recovery due to soft-start.

Loop Compensation

The LT8253/LT8253A use an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT8253/LT8253A circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.
4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck region. The output capacitor has the difficult job of filtering the large RMS output current in boost region. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

APPLICATIONS INFORMATION

5. Other losses. Schottky diode D_B and D_D are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch A causes reverse recovery current loss in buck region, and switch C causes reverse recovery current loss in boost region.

   When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

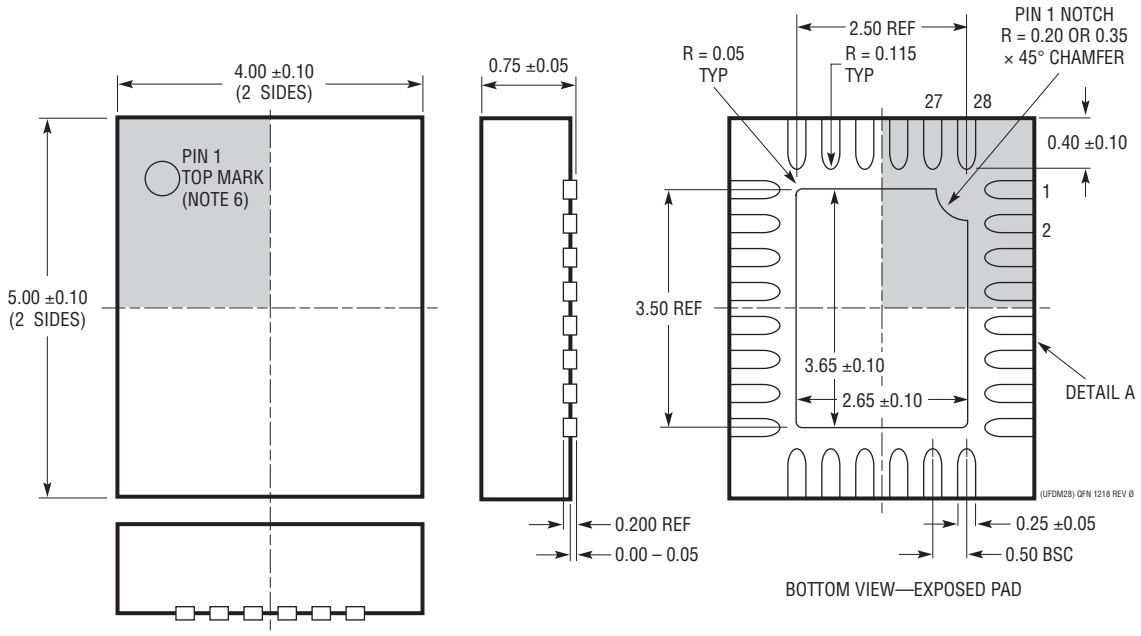
PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

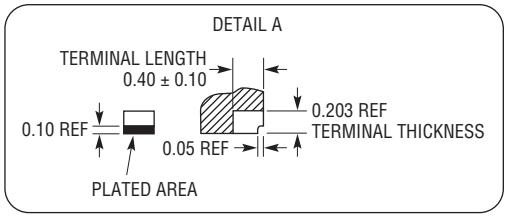
- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, switch A, switch B and D_B in one compact area. Place C_{OUT}, switch C, switch D and D_D in one compact area.
- Use immediate vias to connect the components to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the sources of switch B and switch C.
- Place switch A and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D_B and the C_{IN} capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, D_D and the C_{OUT} capacitor also should have short leads and PCB trace lengths.
- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
- Connect the top driver bootstrap capacitor C_{BST1} closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor C_{BST2} closely to the BST2 and SW2 pins.
- Connect the input capacitors C_{IN} and output capacitors C_{OUT} closely to the power MOSFETs. These capacitors carry the MOSFET AC current.
- Route LSP and LSN traces together with minimum PCB trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. The filter capacitor between LSP and LSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistor. Low ESL sense resistor is recommended.
- Connect the V_C pin compensation network close to the IC, between V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and the power ground. This capacitor carries the MOSFET drivers' current peaks.

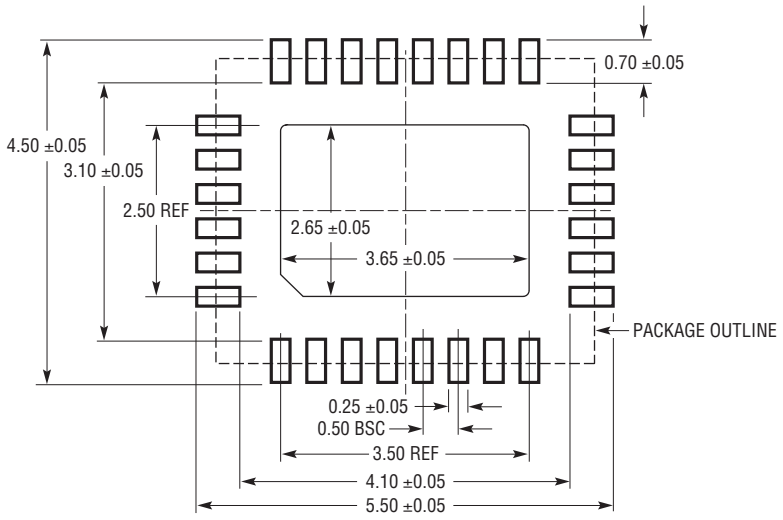
PACKAGE DESCRIPTION

UFDM Package
28-Lead Plastic Side Wettable QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1682 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/22	Added AEC-Q100 Qualified.	1
		Added Revision History Page.	19

TYPICAL APPLICATION

Automotive 45W USB-C Power Delivery Charger (2MHz)