LM49120 Boomer® Audio Power Amplifier Series Audio Sub-System with Mono Class AB Loudspeaker Amplifier and Stereo OCL/SE Headphone Amplifier

Check for Samples: LM49120, LM49120TLEVAL

FEATURES

- **RF Immunity**
- **Selectable OCL/SE Headphone Drivers**
- **32 Step Volume Control**
- **Click and Pop Suppression**
- **Independent Speaker and Headphone Gain Settings**
- **Minimum External Components**
- **Thermal Over Load Protection**
- **Micro-power Shutdown**
- **Space Saving 16–bump DSBGA Package**
- **Thermal Shutdown Protection**
- **Micro-power Shutdown**
- **I^2C Control Interface**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronics**

KEY SPECIFICATIONS

- **Output Power at VDD = 5V:**
  - **Speaker: RL = 8Ω BTL, THD+N ≤ 1%: 1.3W (typ)**
  - **Headphone: RL = 32Ω, SE, THD+N ≤ 1%: 85mW (typ)**
- **Output Power at VDD = 3.6V:**
  - **Speaker: RL = 8Ω, BTL, THD+N ≤ 1%: 632mW (typ)**
- **Output Power at VDD = 3.3V:**
  - **Speaker: RL = 8Ω, BTL, THD+N ≤ 1%: 540mW (typ)**
  - **Headphone: RL = 32Ω, OCL/SE, THD+N ≤ 1%: 35mW (typ)**

DESCRIPTION

The LM49120 is a compact audio subsystem designed for portable handheld applications such as cellular phones. The LM49120 combines a mono 1.3W speaker amplifier, stereo 85mW/ch output capacitorless headphone amplifier, 32 step volume control, and an input mixer/multiplexer into a single 16–bump DSBGA package.

The LM49120 has three input channels: two single-ended stereo inputs and a differential mono input. Each input features a 32-step digital volume control. The headphone output stage features an 8 step (-18dB – 0dB) attenuator, while the speaker output stage has two selectable (0dB/+6dB) gain settings. The digital volume control and mode control are programmed through a two-wire I^2C compatible interface.

Typical Application

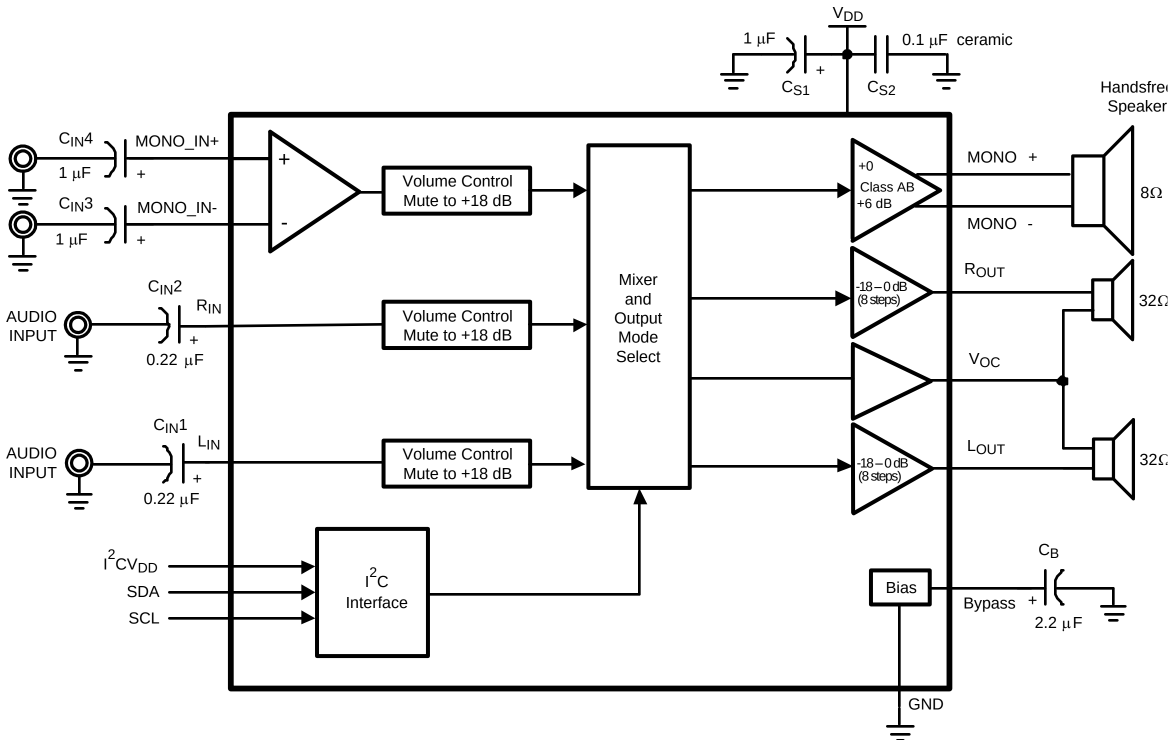
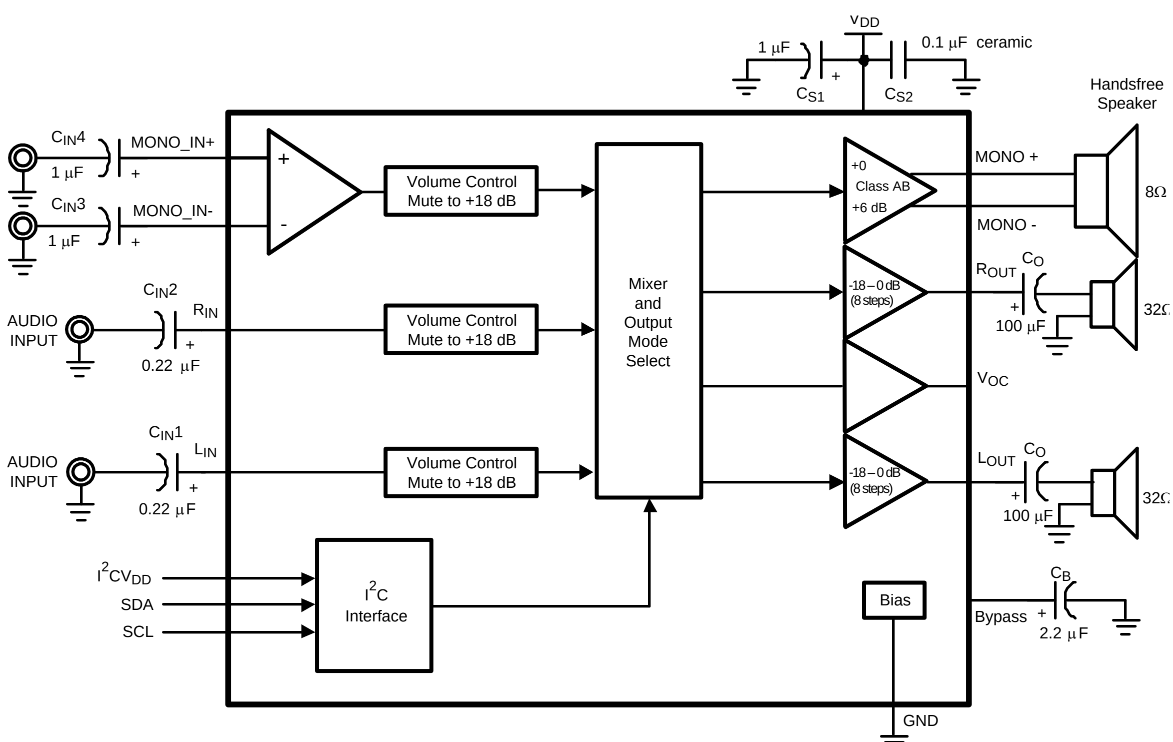


Figure 1. Output Capacitor-Less Configuration



The 6dB speaker gain applies only to the differential input path.

Figure 2. Single-Ended Configuration

Connection Diagram

Top View

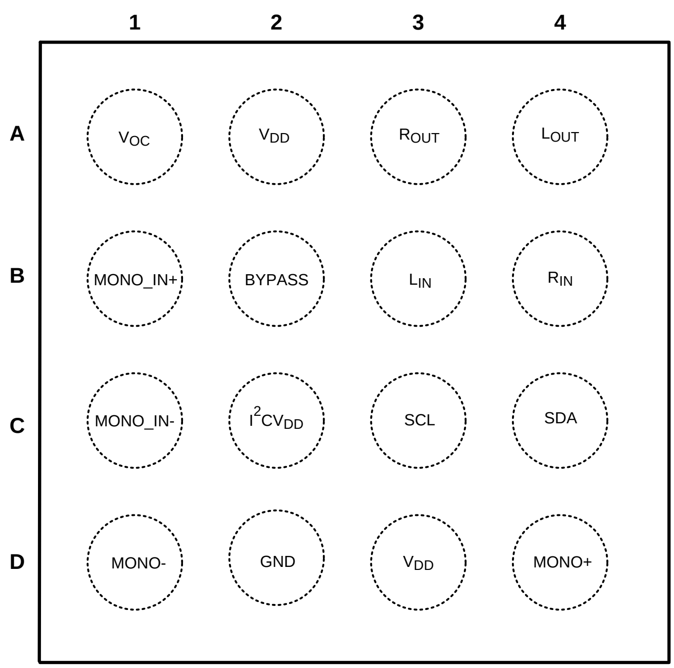


Figure 3. 16 Bump DSBGA Package (Bump-Side Down) See Package Number YZR0016

PIN DESCRIPTIONS

Bump	Name	Description
A1	V_{OC}	Headphone Center Amplifier Output
A2	V_{DD}	Headphone Power Supply
A3	R_{OUT}	Right Channel Headphone Output
A4	L_{OUT}	Left Channel Headphone Output
B1	MONO_IN+	Mono Non-inverting Input
B2	BYPASS	Bias Bypass
B3	L_{IN}	Left Channel Input
B4	R_{IN}	Right Channel Input
C1	MONO_IN-	Mono Inverting Input
C2	I^2CV_{DD}	I^2C Interface Power Supply
C3	SCL	I^2C Clock Input
C4	SDA	I^2C Data Input
D1	MONO-	Loudspeaker Inverting Output
D2	GND	Ground
D3	V_{DD}	Power Supply
D4	MONO+	Loudspeaker Non-inverting Output

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2) (3)

Supply Voltage (1)		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3 to V_{DD} +0.3
Power Dissipation (4)		Internally Limited
ESD Rating (5)		2000V
ESD Rating (6)		200V
Junction Temperature		150°C
Solder Information	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JA} (typ) - YZR0016	62.3°C/W

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(2) The *Electrical Characteristics* tables list spacified specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
(5) Human body model, applicable std. JESD22-A114C.
(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range	−40°C to 85°C
Supply Voltage (V_{DD})	2.7V ≤ V_{DD} ≤ 5.5V
Supply Voltage (I^2CV_{DD})	1.7V ≤ I^2CV_{DD} ≤ 5.5V

Electrical Characteristics 3.3V(1)(2)

The following specifications apply for V_{DD} = 3.3V, T_A = 25°C, all volume controls set to 0dB, unless otherwise specified.

Parameter		Test Conditions	LM49120		Units (Limits)
			Typ (3)	Limits (4)	
I_{DD}	Supply Current	V_{IN} = 0, No Load			
		Output mode 5, 6, 7, 9, 10, 11, 13, 14, 15 OCL Headphone	6.2	8.0	mA (max)
		Output mode 5, 6, 7, 9, 10, 11, 13, 14, 15 SE Headphone	5.5		mA
		Output mode 1, 2, 3 OCL Headphone	4.1	5.3	mA (max)
		Output mode 1, 2, 3 SE Headphone	5.5		mA
		Output mode 4, 8, 12 OCL Headphone	3.7	4.7	mA (max)
		Output mode 4, 8, 12 SE Headphone	3.0		mA
I_{SD}	Shutdown Current	Shutdown Mode 0	0.01	1	µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Output Mode 10, LS output	10		mV
		V_{IN} = 0V, Output Mode 10, HP output, (OCL), 0dB (HP Output Gain)	1.5	5	mV (max)
P_O	Output Power	LS_{OUT}; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	540	500	mW (min)
		L_{OUT} and R_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, OCL, Mode 8	35	30	mW (min)
THD+N	Total Harmonic Distortion + Noise	$MONO_{OUT}$ f = 1kHz P_{OUT} = 250mW; R_L = 8Ω, BTL, Mode 1	0.05		%
		L_{OUT} and R_{OUT}, f = 1kHz P_{OUT} = 12mW; R_L = 32Ω, SE, Mode 8	0.015		%
		L_{OUT} and R_{OUT}, f = 1kHz P_{OUT} = 12mW; R_L = 32Ω, OCL, Mode 8	0.015		%
e_{OUT}	Output Noise	A-weighted, inputs terminated to GND, Output referred			
		Speaker Amplifier; Mode 1	15		µV
		Speaker Amplifier; Mode 2	24		µV
		Speaker Amplifier; Mode 3	29		µV
		Headphone Amplifier; SE, Mode 4	8		µV
		Headphone Amplifier; SE, Mode 8	8		µV
		Headphone Amplifier; SE, Mode 12	11		µV
		Headphone Amplifier; OCL, Mode 4	8		µV
		Headphone Amplifier; OCL, Mode 8	9		µV
		Headphone Amplifier; OCL, Mode 12	12		µV

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(2) The *Electrical Characteristics* tables list spacified specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured
(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

Electrical Characteristics 3.3V(1)(2) (continued)

The following specifications apply for V_{DD} = 3.3V, T_A = 25°C, all volume controls set to 0dB, unless otherwise specified.

Parameter		Test Conditions	LM49120 Typ(3)	LM49120 Limits(4)	Units (Limits)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}; f_{RIPPLE} = 217Hz, R_L = 8Ω (Speaker); R_L = 32Ω (Headphone) C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		Speaker Output; Speaker Output Gain 6dB			
		Speaker Amplifier; Mode 1	79		dB
		Speaker Amplifier; Mode 2	63		dB
		Speaker Amplifier; Mode 3	62		dB
		Speaker Amplifier Output; Speaker Output Gain 0dB			
		Speaker Amplifier; Mode 1	84		dB
		Speaker Amplifier; Mode 2	63		dB
		Speaker Amplifier; Mode 3	62		dB
		Headphone Amplifier Output			
		Headphone Amplifier; SE, Mode 4	83		dB
		Headphone Amplifier; SE, Mode 8	84		dB
		Headphone Amplifier; SE, Mode 12	78		dB
		Headphone Amplifier; OCL, Mode 4	83		dB
		Headphone Amplifier; OCL, Mode 8	80		dB
		Headphone Amplifier; OCL, Mode 12	77		dB
VOL_{ϵ}	Volume Control Step Size Error		±0.2		dB
VOL_{RANGE}	Digital Volume Control Range	Maximum Attenuation	–86	–91 –81	dB (min) dB (max)
		Maximum Gain	18	17.4 18.6	dB (min) dB (max)
$A_{u(HP)}$	HP (SE) Mute Attenuation	Output Mode 1, 2, 3	96		dB
Z_{IN}	MONO_IN Input Impedance L_{IN} and R_{IN} Input Impedance	Maximum gain setting	12.5	10 15	kΩ (min) kΩ (max)
		Maximum attenuation setting	110	90 130	kΩ (min) kΩ (max)
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = 1V_{PP}, Speaker, BTL, Mode 1, R_L = 8Ω Differential Input	61		dB
		f = 217Hz, V_{CM} = 1V_{PP}, Headphone, OCL, Mode 4, R_L = 32Ω Stereo Input	66		dB
X_{TALK}	Crosstalk	Headphone; P_{OUT} = 12mW f = 1kHz, OCL. Mode 8	–60		dB
		Headphone; P_{OUT} = 12mW f = 1kHz, SE, Mode 8	–72		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 4.7µF, OCL	35		ms
		C_B = 2.2µF, SE, Normal Turn On Mode Turn_On_Time = 1	120		ms
		C_B = 2.2µF, OCL	30		ms
		C_B = 4.7µF, SE, Fast Turn On Mode Turn_On_Time = 0	130		ms

Electrical Characteristics 5.0V(1)(2)

The following specifications apply for V_{DD} = 5.0V, T_A = 25°C, all volume controls set to 0dB, unless otherwise specified.

Parameter		Test Conditions	LM49120 Typ(3)	LM49120 Limits(4)	Units (Limits)
I_{DD}	Supply Current	V_{IN} = 0, No Load			
		Output mode 5, 6, 7, 9, 10, 11, 13, 14, 15 OCL Headphone	7.2		mA
		Output mode 5, 6, 7, 9, 10, 11, 13, 14, 15 SE Headphone	6.4		mA
		Output mode 1, 2, 3 OCL Headphone	6.4		mA
		Output mode 1, 2, 3 SE Headphone	4.8		mA
		Output mode 4, 8, 12 OCL Headphone	4.4		mA
		Output mode 4, 8, 12 SE Headphone	3.5		mA
I_{SD}	Shutdown Current	Shutdown Mode 0	0.01		µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Output Mode 10, LS output	10		mV
		V_{IN} = 0V, Output Mode 10, HP output, (OCL), 0dB (HP Output Gain)	1.5		mV
P_O	Output Power	LS $_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	1.3		W
		L_{OUT} and R_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, OCL, Mode 8	85		mW
THD+N	Total Harmonic Distortion + Noise	LS_{OUT} f = 1kHz P_{OUT} = 250mW; R_L = 8Ω, BTL, Mode 1	0.05		%
		L_{OUT} and R_{OUT}, f = 1kHz P_{OUT} = 12mW; R_L = 32Ω, SE, Mode 8	0.015		%
		L_{OUT} and R_{OUT}, f = 1kHz P_{OUT} = 12mW; R_L = 32Ω, OCL, Mode 8	0.015		%
e_{OUT}	Output Noise	A-weighted, inputs terminated to GND, Output referred			
		Speaker Amplifier; Mode 1	17		µV
		Speaker Amplifier; Mode 2	27		µV
		Speaker Amplifier; Mode 3	33		µV
		Headphone Amplifier; SE, Mode 4	8		µV
		Headphone Amplifier; SE, Mode 8	8		µV
		Headphone Amplifier; SE, Mode 12	12		µV
		Headphone Amplifier; OCL, Mode 4	9		µV
		Headphone Amplifier; OCL, Mode 8	9		µV
		Headphone Amplifier; OCL, Mode 12	12		µV

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(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

Electrical Characteristics 5.0V[1][2] (continued)

The following specifications apply for V_{DD} = 5.0V, T_A = 25°C, all volume controls set to 0dB, unless otherwise specified.

Parameter		Test Conditions	LM49120 Typ[3]	LM49120 Limits[4]	Units (Limits)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP}; f_{RIPPLE} = 217Hz, R_L = 8Ω (Speaker); R_L = 32Ω (Headphone) C_B = 2.2µF, BTL All audio inputs terminated to GND; output referred			
		Speaker Output; Speaker Output Gain 6dB			
		Speaker Amplifier; Mode 1	69		dB
		Speaker Amplifier; Mode 2	60		dB
		Speaker Amplifier; Mode 3	58		dB
		Speaker Amplifier Output; Speaker Output Gain 0dB			
		Speaker Amplifier; Mode 1	84		dB
		Speaker Amplifier; Mode 2	63		dB
		Speaker Amplifier; Mode 3	62		dB
		Headphone Amplifier Output			
		Headphone Amplifier; SE, Mode 4	75		dB
		Headphone Amplifier; SE, Mode 8	75		dB
		Headphone Amplifier; SE, Mode 12	72		dB
		Headphone Amplifier; OCL, Mode 4	75		dB
		Headphone Amplifier; OCL, Mode 8	75		dB
		Headphone Amplifier; OCL, Mode 12	72		dB
VOL_{ϵ}	Volume Control Step Size Error		±0.2		dB
VOL_{RANGE}	Digital Volume Control Range	Maximum Attenuation	–86	–91 –81	dB dB
		Maximum Gain	18		dB dB
$A_{u(HP)}$	HP (SE) Mute Attenuation	Output Mode 1, 2, 3	96		dB
Z_{IN}	MONO_IN Input Impedance L_{IN} and R_{IN} Input Impedance	Maximum gain setting	12.5		kΩ kΩ
		Maximum attenuation setting	110		kΩ kΩ
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = 1V_{PP}, Speaker, BTL, Mode 1, R_L = 8Ω Differential Input	61		dB
		f = 217Hz, V_{CM} = 1V_{PP}, Headphone, OCL, Mode 4, R_L = 32Ω Stereo Input	66		dB
X_{TALK}	Crosstalk	Headphone; P_{OUT} = 12mW f = 1kHz, OCL, Mode 8	–54		dB
		Headphone; P_{OUT} = 12mW f = 1kHz, SE, Mode 8	–72		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 4.7µF, OCL	28		ms
		C_B = 2.2µF, SE, Normal Turn On Mode Turn_On_Time = 1	151		ms
		C_B = 2.2µF, OCL	25		ms
		C_B = 4.7µF, SE, Fast Turn On Mode Turn_On_Time = 0	168		ms

I^2C Timing Characteristics 2.2V ≤ $I^2C\_V_{DD}$ ≤ 5.5V (1)(2)

The following specifications apply for V_{DD} = 5.0V and 3.3V, T_A = 25°C, 2.2V ≤ $I^2C\_V_{DD}$ ≤ 5.5V, unless otherwise specified.

Parameter		Test Conditions	LM49120		Units (Limits)
			Typ (3)	Limits (4)	
t_1	I^2C Clock Period			2.5	µs (min)
t_2	I^2C Data Setup Time			100	ns (min)
t_3	I^2C Data Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
t_6	I^2C Data Hold Time			100	ns (min)
V_{IH}	I^2C Input Voltage High			$0.7xI^2CV_{DD}$	V (min)
V_{IL}	I^2C Input Voltage Low			$0.3xI^2CV_{DD}$	V (max)

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(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

I^2C Timing Characteristics 1.7V ≤ $I^2C\_V_{DD}$ ≤ 2.2V (1)(2)

The following specifications apply for V_{DD} = 5.0V and 3.3V, T_A = 25°C, 1.7V ≤ $I^2C\_V_{DD}$ ≤ 2.2V, unless otherwise specified.

Parameter		Test Conditions	LM49120		Units (Limits)
			Typ (3)	Limits (4)	
t_1	I^2C Clock Period			2.5	µs (min)
t_2	I^2C Data Setup Time			250	ns (min)
t_3	I^2C Data Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	I^2C Data Hold Time			250	ns (min)
V_{IH}	I^2C Input Voltage High			$0.7xI^2CV_{DD}$	V (min)
V_{IL}	I^2C Input Voltage Low			$0.3xI^2CV_{DD}$	V (max)

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(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

Typical Performance Characteristics

Filter BW = 22kHz

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW, f = 1kHz, Mode 8, OCL

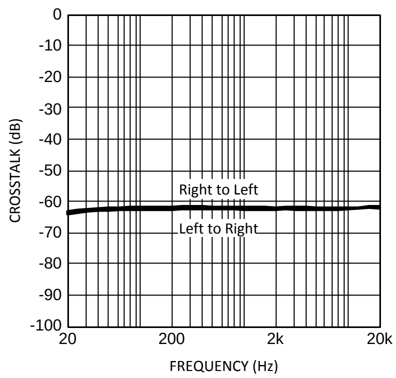

Figure 4.

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW, f = 1kHz, Mode 8, SE

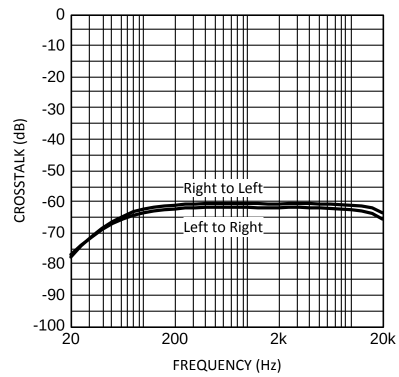

Figure 5.

Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW, f = 1kHz, Mode 8, OCL

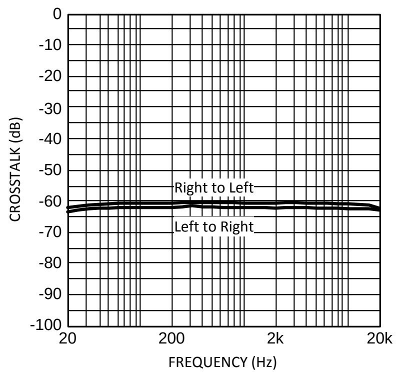

Figure 6.

Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW, f = 1kHz, Mode 8, SE

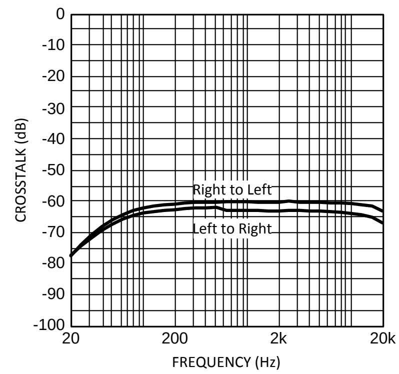

Figure 7.

Output Power vs Supply Voltage
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Mode 8, OCL

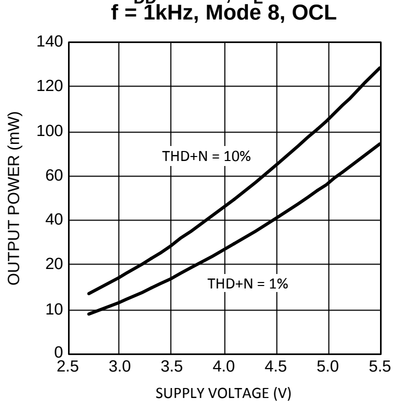

Figure 8.

Output Power vs Supply Voltage
V_{DD} = 5V, R_L = 8Ω, f = 1kHz, Mode 1, Speaker

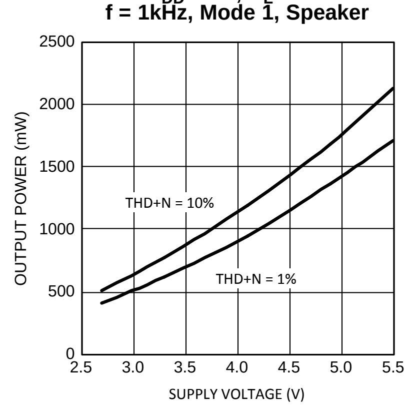

Figure 9.

Typical Performance Characteristics (continued)

Filter BW = 22kHz

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω
f = 1kHz, Mode 8, OCL

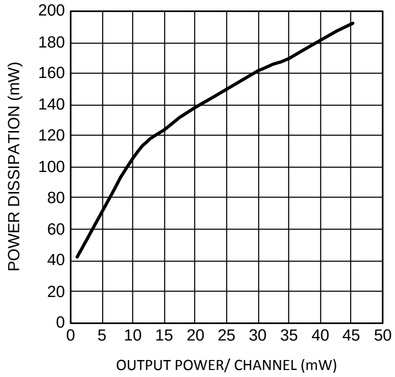

Figure 10.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 8Ω
f = 1kHz, Mode 1, Speaker

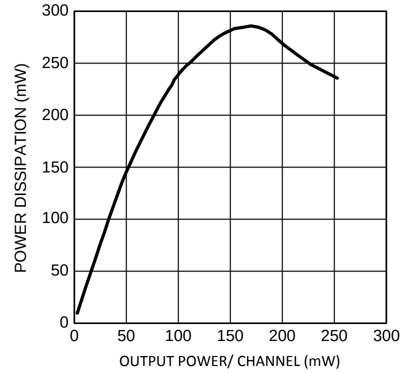

Figure 11.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω
f = 1kHz, Mode 8, OCL

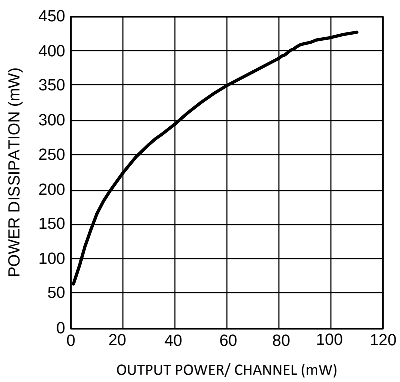

Figure 12.

Power Dissipation vs Output Power
V_{DD} =5V, R_L = 8Ω
f = 1kHz, Mode 1, Speaker

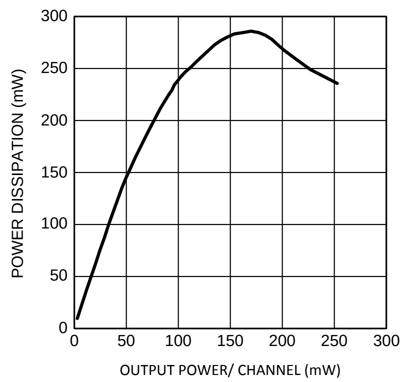

Figure 13.

Supply Current vs Supply Voltage
V_{IN}= GND, No load

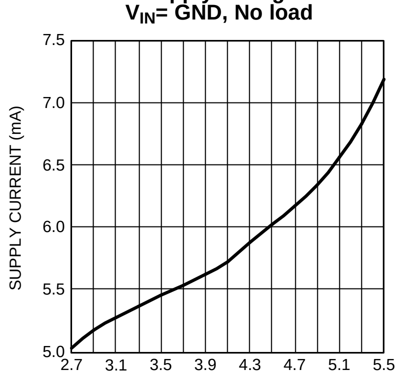

Figure 14.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
f = 22kHz, Mode 8, OCL

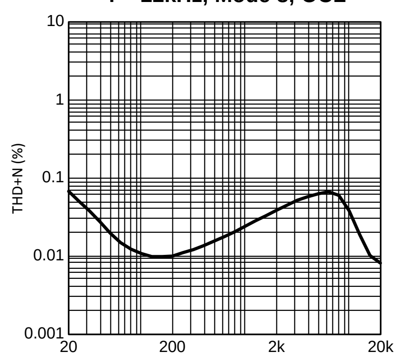

Figure 15.

Typical Performance Characteristics (continued)

Filter BW = 22kHz

THD+N vs Frequency V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW f = 22kHz, Mode 8, SE

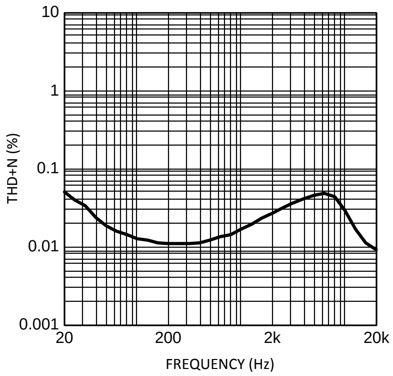

Figure 16.

THD+N vs Frequency V_{DD} = 3.3V, R_L = 64Ω, P_O = 24mW f = 22kHz, Mode 4, BTL

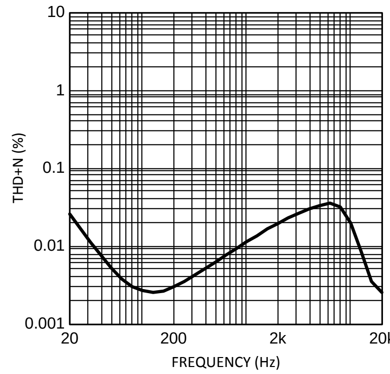

Figure 17.

THD+N vs Frequency V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW f = 1kHz, Mode 1, Speaker

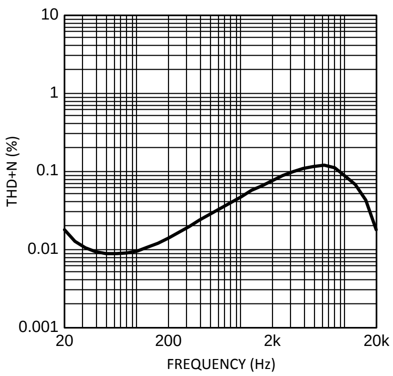

Figure 18.

THD+N vs Frequency V_{DD} = 5V, R_L = 32Ω, P_O = 30mW f = 22kHz, Mode 8, OCL

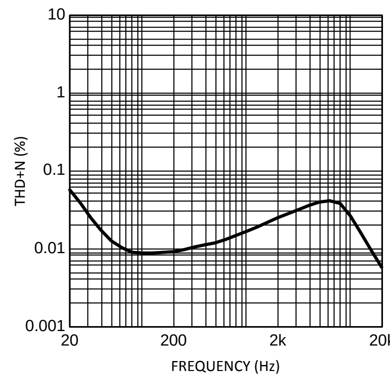

Figure 19.

THD+N vs Frequency V_{DD} = 5V, R_L = 32Ω, P_O = 30mW f = 22kHz, Mode 8, SE

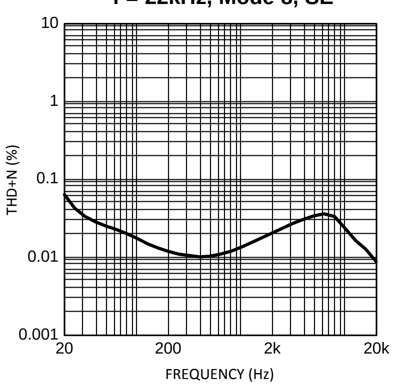

Figure 20.

THD+N vs Frequency V_{DD} = 5V, R_L = 64Ω, P_O = 72mW f = 22kHz, Mode 4, BTL

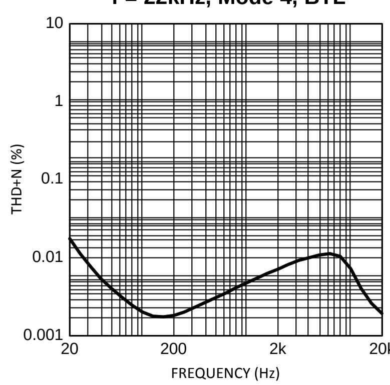

Figure 21.

Typical Performance Characteristics (continued)

Filter BW = 22kHz

THD+N vs Frequency V_{DD} = 5V, R_L = 8Ω, P_O = 500mW f = 1kHz, Mode 1, Speaker

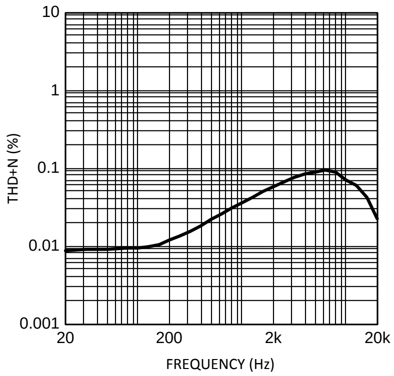

Figure 22.

THD+N vs Output Power V_{DD} = 3.3V, R_L = 32Ω f = 1kHz, Mode 8, OCL

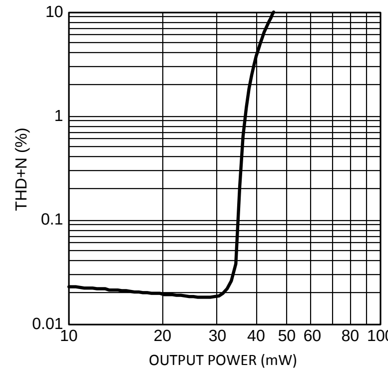

Figure 23.

THD+N vs Output Power V_{DD} = 3.3V, R_L = 32Ω f = 1kHz, Mode 8, SE

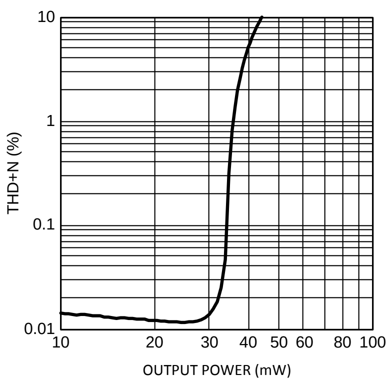

Figure 24.

THD+N vs Output Power V_{DD} = 3.3V, R_L = 64Ω f = 1kHz, Mode 4, BTL

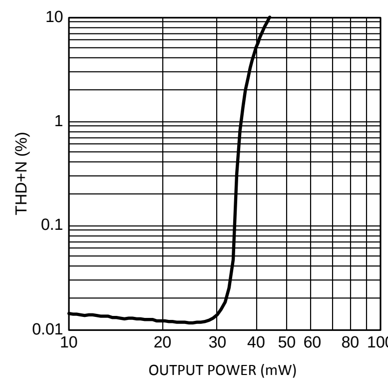

Figure 25.

THD+N vs Output Power V_{DD} = 3.3V, R_L = 8Ω f = 1kHz, Mode 1, Speaker

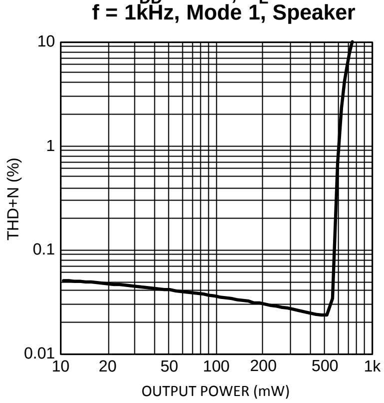

Figure 26.

THD+N vs Output Power V_{DD} = 5V, R_L = 32Ω f = 1kHz, Mode 8, OCL

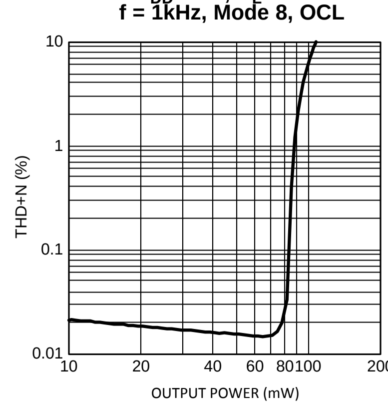

Figure 27.

Typical Performance Characteristics (continued)

Filter BW = 22kHz

THD+N vs Output Power V_{DD} = 5V, R_L = 32Ω f = 1kHz, Mode 8, SE

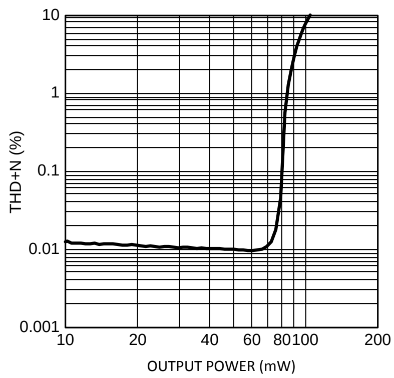

Figure 28.

THD+N vs Output Power V_{DD} = 5V, R_L = 64Ω f = 1kHz, Mode 4, BTL

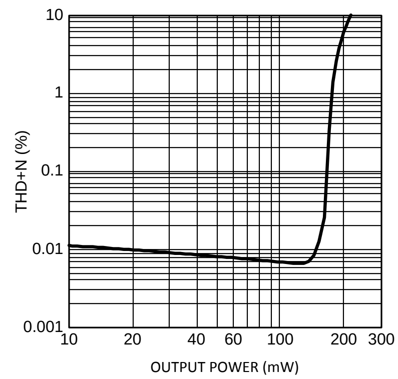

Figure 29.

THD+N vs Output Power V_{DD} = 5V, R_L = 8Ω f = 1kHz, Mode 1, Speaker

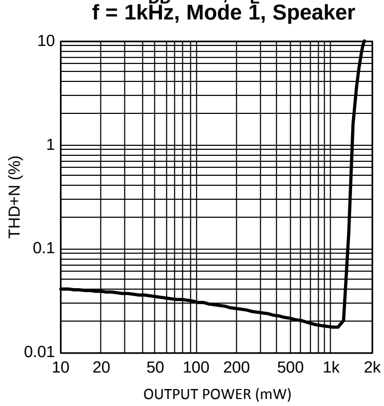

Figure 30.

PSRR vs Frequency V_{DD} = 3.3V, R_L = 8Ω, C_{BYP} = 2.2µF V_{RIPPLE} = 200mV_{P-P}, MODE 1

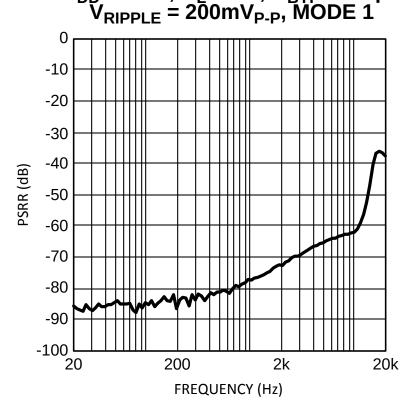

Figure 31.

PSRR vs Frequency V_{DD} = 3.3V, R_L = 8Ω, C_{BYP} = 4.7µF V_{RIPPLE} = 200mV_{P-P}, MODE 1

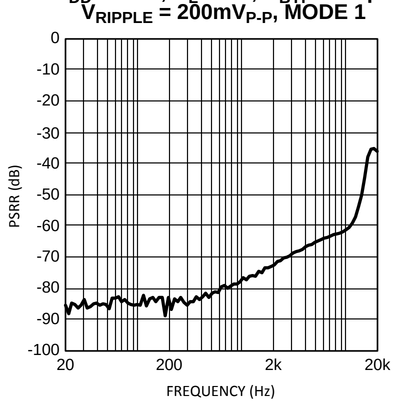

Figure 32.

PSRR vs Frequency V_{DD} = 3.3V, R_L = 32Ω, C_{BYP} = 2.2µF V_{RIPPLE} = 200mV_{P-P}, MODE 8, OCL

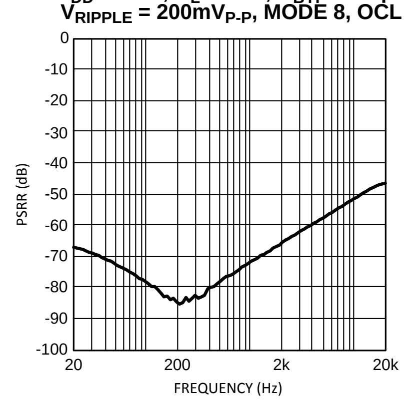

Figure 33.

Typical Performance Characteristics (continued)

Filter BW = 22kHz

PSRR vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, C_{BYP} = 2.2µF
V_{RIPPLE} = 200mV_{P-P}, MODE 8, SE

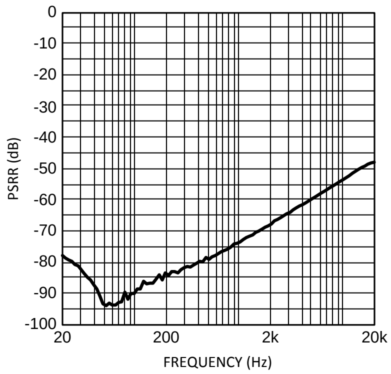

Figure 34.

PSRR vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, C_{BYP} = 4.7µF
V_{RIPPLE} = 200mV_{P-P}, MODE 8, OCL

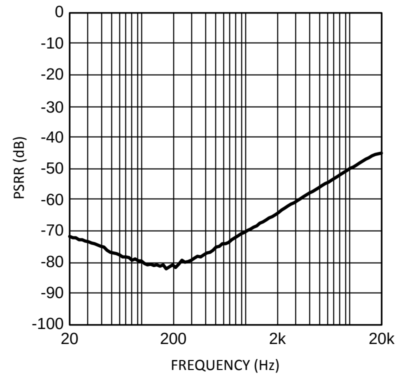

Figure 35.

PSRR vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, C_{BYP} = 2.2µF
V_{RIPPLE} = 200mV_{P-P}, MODE 4, BTL

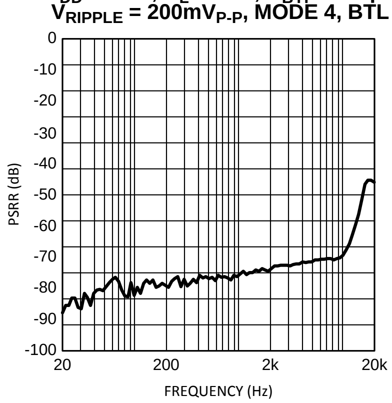

Figure 36.

PSRR vs Frequency
V_{DD} = 3.3V, R_L = 64Ω, C_{BYP} = 4.7µF
V_{RIPPLE} = 200mV_{P-P}, MODE 4, BTL

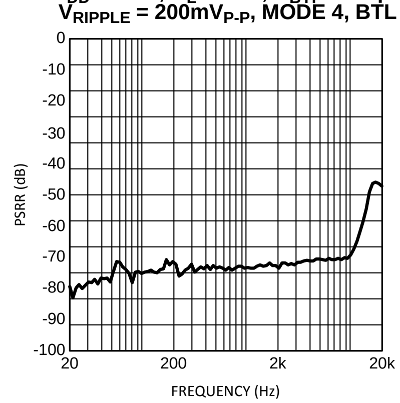

Figure 37.

PSRR vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, C_{BYP} = 2.2µF
V_{RIPPLE} = 200mV_{P-P}, MODE 1

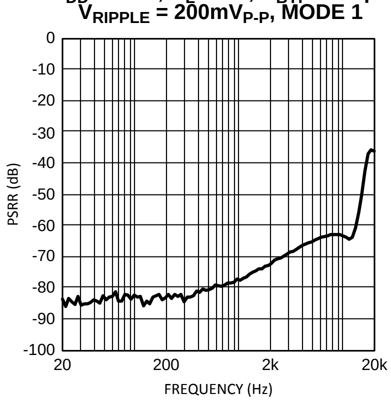

Figure 38.

PSRR vs Frequency
V_{DD} = 5V, R_L = 8Ω, C_{BYP} = 4.7µF
V_{RIPPLE} = 200mV_{P-P}, MODE 1

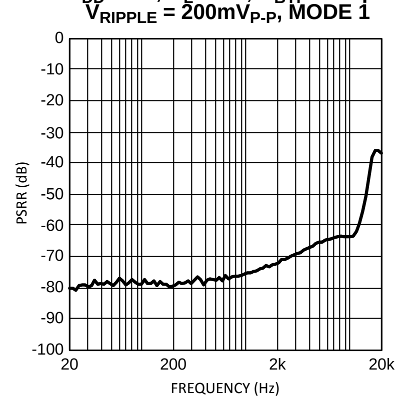

Figure 39.

Typical Performance Characteristics (continued)

Filter BW = 22kHz

PSRR vs Frequency
V_{DD} = 5V, R_L = 32Ω, C_{BYP} = 2.2µF
V_{RIPPLE} = 200mV_{P-P}, MODE 8, OCL

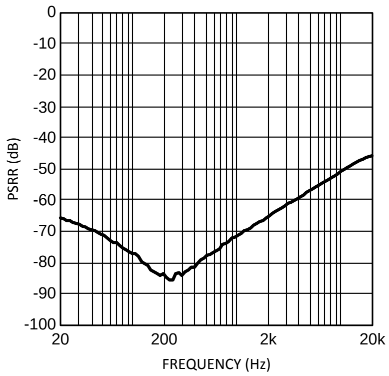

Figure 40.

PSRR vs Frequency
V_{DD} = 5V, R_L = 32Ω, C_{BYP} = 2.2µF
V_{RIPPLE} = 200mV_{P-P}, MODE 8, SE

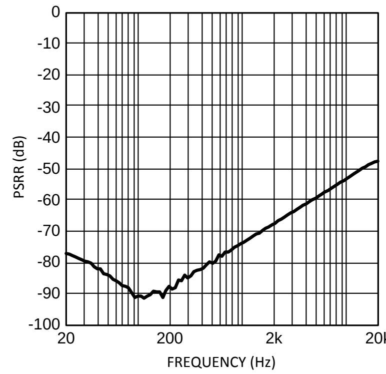

Figure 41.

PSRR vs Frequency
V_{DD} = 5V, R_L = 64Ω, C_{BYP} = 4.7µF
V_{RIPPLE} = 200mV_{P-P}, MODE 4, BTL

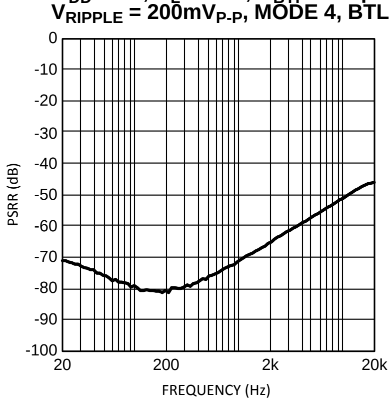

Figure 42.

PSRR vs Frequency
V_{DD} = 5V, R_L = 32Ω, C_{BYP} = 4.7µF
V_{RIPPLE} = 200mV_{P-P}, MODE 8, SE

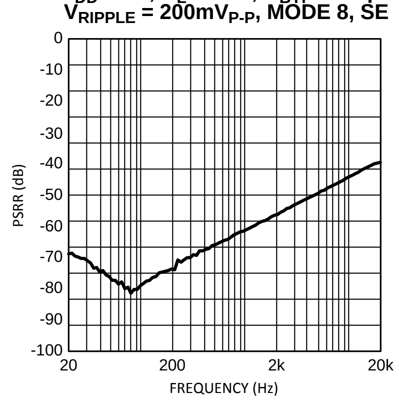

Figure 43.

APPLICATION INFORMATION

I²C COMPATIBLE INTERFACE

The LM49120 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM49120 and the master can communicate at clock rates up to 400kHz. Figure 44 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49120 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 45). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 46). The LM49120 device address is 1111100.

I²C BUS FORMAT

The I²C bus format is shown in Figure 46. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit. R/$\overline{W}$ = 0 indicates the master is writing to the slave device, R/$\overline{W}$ = 1 indicates the master wants to read data from the slave device. Set R/$\overline{W}$ = 0; the LM49120 is a WRITE-ONLY device and will not respond the R/$\overline{W}$ = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM49120 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM49120 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

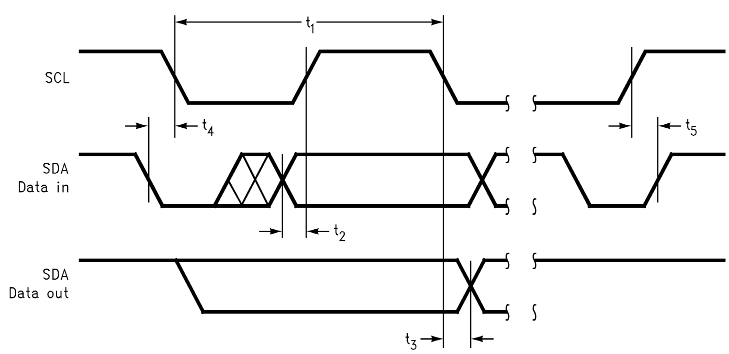

Figure 44. I²C Timing Diagram

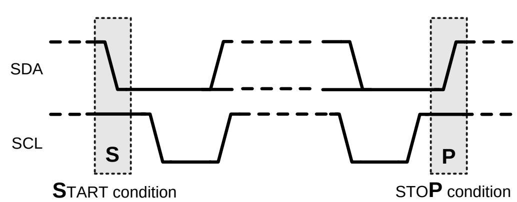

Figure 45. Start and Stop Diagram

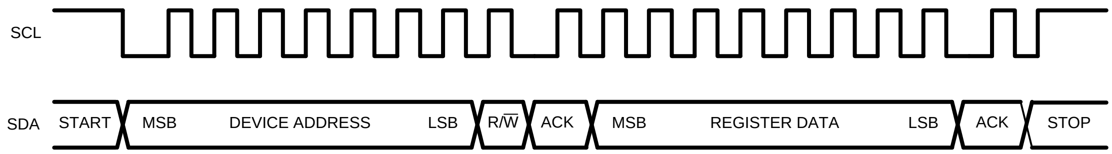

Figure 46. Example Write Sequence

Table 1. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 (R/$\overline{W}$)
Device Address	1	1	1	1	1	0	0	0

Table 2. Control Registers

	B7	B6	B5	B4	B3	B2	B1	B0
Shutdown Control	0	0	0	OCL/SE	HP/BTL	SD_I^{2}CV$_{DD}$	Turn_On _Time	PWR_On
Output Mode Control	0	1	0	0	MC3	MC2	MC1	MC0
Output Gain Control	1	0	0	0	LS_GAIN	HP_GAIN2	HP_GAIN1	HP_GAIN0
Mono Input Volume Control	1	0	1	MG4	MG3	MG2	MG1	MG0
Left Input Volume Control	1	1	0	LG4	LG3	LG2	LG1	LG0
Right Input Volume Control	1	1	1	RG4	RG3	RG2	RG1	RG0

Table 3. Shutdown Control Register

Bit	Name	Value	Description
B4	OSC/SE	0	Single-Ended headphone mode (Capacitively Coupled)
		1	Output Capacitor-less (OCL) headphone mode
B3	HP/BTL	0	Single-ended stereo headphone output mode
		1	Mono, BTL output mode.
B2	SD_I^{2}CVDD	0	I^{2}CV$_{DD}$ acts as an active low RESET input. If I^{2}CV$_{DD}$ drops below 1.1V, the device is reset and the I2C registers are restored to their default state.
		1	Normal Operation. I^{2}CV$_{DD}$ voltage does not reset the device
B1	TURN_ON_TIME	0	Fast turn on time (120ms)
		1	Normal turn on time (130ms)
B0	PWR_ON	0	Device Disabled
		1	Device Enabled

Table 4. Output Mode Control (HP/BTL = 0)

Output Mode Number	MC3	MC2	MC1	MC0	LS Output	HP R Output	HP L Output
0	0	0	0	0	SD	SD	SD
1	0	0	0	1	G_M x M	Mute	Mute
2	0	0	1	0	2 x (G_L x L + G_R x R)	Mute	Mute
3	0	0	1	1	2 x (G_L x L + G_R x R) + G_M x M	Mute	Mute
4	0	1	0	0	SD	G_M x M/2	G_M x M/2
5	0	1	0	1	G_M x M	G_M x M/2	G_M x M/2
6	0	1	1	0	2 x (G_L x L + G_R x R)	G_M x M/2	G_M x M/2

Table 4. Output Mode Control (HP/BTL = 0) (continued)

Output Mode Number	MC3	MC2	MC1	MC0	LS Output	HP R Output	HP L Output
7	0	1	1	1	2 x (G_L x L + G_R x R) + G_M x M	G_M x M/2	G_M x M/2
8	1	0	0	0	SD	G_R x R	G_L x L
9	1	0	0	1	G_M x M	G_R x R	G_L x L
10	1	0	1	0	2 x (G_L x L + G_R x R)	G_R x R	G_L x L
11	1	0	1	1	2 x (G_L x L + G_R x R) + G_M x M	G_R x R	G_L x L
12	1	1	0	0	SD	G_R x R + G_M x M/2	G_L x L + G_M x M/2
13	1	1	0	1	G_M x M	G_R x R + G_M x M/2	G_L x L + G_M x M/2
14	1	1	1	0	2 x (G_L x L + G_R x R)	G_R x R + G_M x M/2	G_L x L + G_M x M/2
15	1	1	1	1	2 x (G_L x L + G_R x R) + G_M x M	G_R x R + G_M x M/2	G_L x L + G_M x M/2

Table 5. Output Mode Control (HP/BTL = 1)

Output Mode Number	MC3	MC2	MC1	MC0	LS Output	HP R Output	HP L Output
4	0	1	0	0	SD	G_M x M^+/2	G_M x M^-/2
5	0	1	0	1	G_M x M	G_M x M^+/2	G_M x M^-/2
6	0	1	1	0	2 x (G_L x L + G_R x R)	G_M x M^+/2	G_M x M^-/2
7	0	1	1	1	2 x (G_L x L + G_R x R) + G_P x P	G_M x M^+/2	G_M x M^-/2
12	1	1	0	0	SD	G_R x R + G_M x M^+/2	G_L x L + G_M x M^-/2
13	1	1	0	1	G_M x M	G_R x R + G_M x M^+/2	G_L x L + G_M x M^-/2
14	1	1	1	0	2 x (G_L x L + G_R x R)	G_R x R + G_M x M^+/2	G_L x L + G_M x M^-/2
15	1	1	1	1	2 x (G_L x L + G_R x R) + G_M x M	G_R x R + G_M x M^+/2	G_L x L + G_M x M^-/2

Table 6. Volume Control Table

Volume Step	_G4	_G3	_G2	_G1	_G0	Gain (dB)
1	0	0	0	0	0	Mute
2	0	0	0	0	1	–46.50
3	0	0	0	1	0	–40.50
4	0	0	0	1	1	–34.50
5	0	0	1	0	0	–30.00
6	0	0	1	0	1	–27.00
7	0	0	1	1	0	–24.00
8	0	0	1	1	1	–21.00
9	0	1	0	0	0	–18.00
10	0	1	0	0	1	–15.00
11	0	1	0	1	0	–13.50
12	0	1	0	1	1	–12.00
13	0	1	1	0	0	–10.50
14	0	1	1	0	1	–9.00
15	0	1	1	1	0	–7.50
16	0	1	1	1	1	–6.00
17	1	0	0	0	0	–4.50
18	1	0	0	0	1	–3.00

Table 6. Volume Control Table (continued)

Volume Step	_G4	_G3	_G2	_G1	_G0	Gain (dB)
19	1	0	0	1	0	–1.50
20	1	0	0	1	1	0.00
21	1	0	1	0	0	1.50
22	1	0	1	0	1	3.00
23	1	0	1	1	0	4.50
24	1	0	1	1	1	6.00
25	1	1	0	0	0	7.50
26	1	1	0	0	1	9.00
27	1	1	0	1	0	10.50
28	1	1	0	1	1	12.00
29	1	1	1	0	0	13.50
30	1	1	1	0	1	15.00
31	1	1	1	1	0	16.50
32	1	1	1	1	1	18.00

Table 7. Output Gain Control (Headphone)

HP_GAIN2	HP_GAIN1	HP_GAIN0	GAIN (dB)
0	0	0	0
0	0	1	–1.2
0	1	0	–2.5
0	1	1	–4.0
1	0	0	–6.0
1	0	1	–8.5
1	1	0	–12
1	1	1	–18

Table 8. Output Gain Control (Loudspeaker)

Bit	Value	Gain (dB) Differential Input	Gain (dB) Single-Ended Input
LS_GAIN	0	0	+6
	1	+6	+12

BRIDGE CONFIGURATION EXPLAINED

The LM49120 loudspeaker amplifier is designed to drive a load differentially, a configuration commonly referred to as a bridge-tied load (BTL). The BTL configuration differs from the single-ended configuration, where one side of the load is connected to ground. A BTL amplifier offers advantages over a single-ended device. By driving the load differentially, the output voltage is doubled, compared to a single-ended amplifier under similar conditions. This doubling of the output voltage leads to a quadrupling of the output power, for example, the theoretical maximum output power for a single-ended amplifier driving 8Ω and operating from a 5V supply is 390mW, while the theoretical maximum output power for a BTL amplifier operating under the same conditions is 1.56W. Since the amplifier outputs are both biased about $V_{DD}/2$, there is no net DC voltage across the load, eliminating the DC blocking capacitors required by single-ended, single-supply amplifiers.

Headphone Amplifier

The LM49120 headphone amplifier features two different operating modes, output capacitor-less (OCL) and single-ended (SE) capacitor coupled mode.

The OCL architecture eliminates the bulky, expensive output coupling capacitors required by traditional headphone amplifiers. In OCL mode, the LM49120 headphone section uses three amplifiers. Two amplifiers drive the headphones, while the third (V_{OC}) is set to the internally generated bias voltage (typically $V_{DD}/2$). The third amplifier is connected to the return terminal of the headphone jack (Figure 1). In this configuration, the signal side of the headphone is biased to $V_{DD}/2$, the return is biased to $V_{DD}/2$, thus there is no net DC voltage across the headphone, eliminating the need for an output coupling capacitor. Removing the output coupling capacitors from the headphone signal path reduces component count, reducing system cost and board space consumption, as well as improving low frequency performance.

In OCL mode, the headphone return sleeve is biased to $V_{DD}/2$. When driving headphones, the voltage on the return sleeve is not an issue. However, if the headphone output is used as a line out, the $V_{DD}/2$ can conflict with the GND potential that the line-in would expect on the return sleeve. When the return of the headphone jack is connected to GND the V_{OC} amplifier of the LM49120 detects an output short circuit condition and is disabled, preventing damage to the LM49120, and allowing the headphone return to be biased at GND.

Single-Ended, Capacitor Coupled Mode

In single-ended mode, the V_{OC} amplifier is disabled, and the headphone outputs are coupled to the jack through series capacitors, allowing the headphone return to be connected to GND (Figure 2). In SE mode, the LM49120 requires output coupling capacitors to block the DC component of the amplifier output, preventing DC current from flowing to the load. The output capacitor and speaker impedance form a high pass filter with a -3dB roll-off determined by:

$$f_{-3dB} = 1 / 2\pi R_L C_O \quad \text{(Hz)} \tag{1}$$

Where R_L is the headphone impedance, and C_O is the value of the output coupling capacitor. Choose C_O such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high results in poor low frequency performance. Select capacitor dielectric types with low ESR to minimize signal loss due to capacitor series resistance and maximize power transfer to the load.

Headphone Amplifier BTL Mode

The LM49120 headphone amplifiers feature a BTL mode where the two headphone outputs, L_{OUT} and R_{OUT} are configured to drive a mono speaker differentially. In BTL mode, the amplifier accepts audio signals from either the differential MONO inputs, or the single-ended stereo inputs, and converts them to a mono BTL output. However, if the stereo inputs are 180° out of phase, no audio will be present at the amplifier outputs. Bit B3 (HP/BTL) in the Shutdown Control Register determines the headphone output mode. Set HP/BTL = 0 for stereo headphone mode, set HP/BTL = 1 for BTL mode.

Input Mixer/Multiplexer

The LM49120 includes a comprehensive mixer multiplexer controlled through the I^2C interface. The mixer/multiplexer allows any input combination to appear on any output of the LM49120. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. Table 4 and Table 5 show how the input signals are mixed together for each possible input selection.

Audio Amplifier Gain Setting

Each channel of the LM49120 has two separate gain stages. Each input stage features a 32-step volume control with a range of -46dB to +18dB (Table 6). The loudspeaker output stage has two additional gain settings: 0dB and +6dB (Table 8) when the differential MONO input is selected, and +6dB and +12dB when the single-ended stereo inputs are selected. The headphone gain is not affected by the input mode. Each headphone output stage has 8 gain settings (Table 7). This allows for a maximum separation of 22dB between the speaker and headphone outputs when both are active.

Calculate the total gain of the given signal path as follows:

$$A_{VOL} + A_{VOS} = A_{VTOTAL} \quad \text{(dB)} \tag{2}$$

where

- A_{VOL} is the volume control level, A_{VOS} is the output stage gain setting
- A_{VTOTAL} is the total gain for the signal path.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM49120 has a pair of bridged-tied amplifiers driving a handsfree speaker, MONO. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation 2, assuming a 5V power supply and an 8Ω load, the maximum MONO power dissipation is 633mW.

$$P_{DMAX\text{-}SPKROUT} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridge Mode} \quad (3)$$

The LM49120 also has a pair of single-ended amplifiers driving stereo headphones, R_{OUT} and L_{OUT}. The maximum internal power dissipation for R_{OUT} and L_{OUT} is given by Equation 3 and Equation 4. From Equation 3 and Equation 4, assuming a 5V power supply and a 32Ω load, the maximum power dissipation for L_{OUT} and R_{OUT} is 40mW, or 80mW total.

$$P_{DMAX\text{-}LOUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (4)$$

$$P_{DMAX\text{-}ROUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (5)$$

The maximum internal power dissipation of the LM49120 occurs when all three amplifiers pairs are simultaneously on; and is given by Equation 5.

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}SPKROUT} + P_{DMAX\text{-}LOUT} + P_{DMAX\text{-}ROUT} \quad (6)$$

The maximum power dissipation point given by Equation 5 must not exceed the power dissipation given by Equation 6:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (7)$$

The LM49120's T_{JMAX} = 150°C. In the SQ package, the LM49120's θ_{JA} is 46°C/W. At any given ambient temperature T_A, use Equation 6 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 6 and substituting $P_{DMAX\text{-}TOTAL}$ for P_{DMAX}' results in Equation 7. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM49120's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX\text{-}TOTAL}\ \theta_{JA} \quad (8)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum mono power dissipation without exceeding the maximum junction temperature is approximately 121°C for the SQ package.

$$T_{JMAX} = P_{DMAX\text{-}TOTAL}\ \theta_{JA} + T_A \quad (9)$$

Equation 8 gives the maximum junction temperature T_{JMAX}. If the result violates the LM49120's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 5 is greater than that of Equation 6, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance). Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

PROPER SELECTION OF EXTERNAL COMPONENTS

Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49120. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation 10 below.

$$f = 1 / (2\pi R_{IN} C_{IN}) \quad \text{(Hz)} \tag{10}$$

Where the value of R_{IN} is given in the Electrical Characteristics Table.

High pass filtering the audio signal helps protect the speakers. When the LM49120 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

Bias Capacitor Selection

The LM49120 internally generates a $V_{DD}/2$ common-mode bias voltage. The BIAS capacitor C_{BIAS}, improves PSRR and THD+N by reducing noise at the BIAS node. Use a 2.2µF ceramic placed as close to the device as possible.

PCB LAYOUT GUIDELINES

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM49120 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents digital noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

REVISION HISTORY

Rev	Date	Description
1.0	06/26/08	Initial release.
1.01	07/15/08	Edited the Ordering Information table.
C	05/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM49120TL/NOPB	ACTIVE	DSBGA	YZR	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GK2	Samples
LM49120TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GK2	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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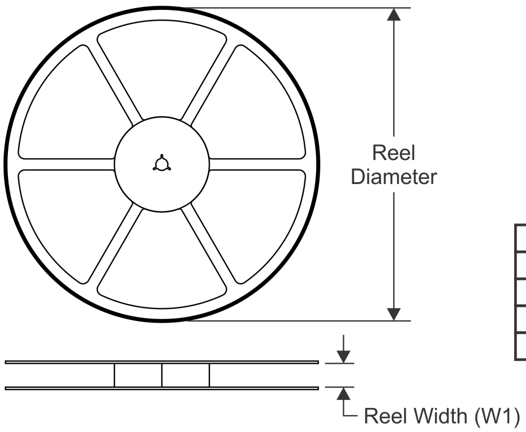
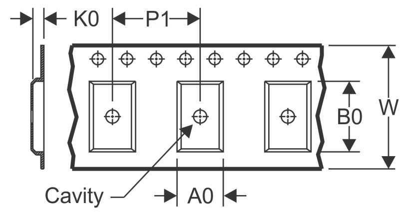
TAPE AND REEL INFORMATION

REEL DIMENSIONS

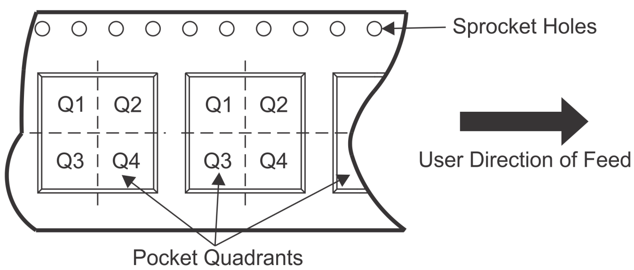


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

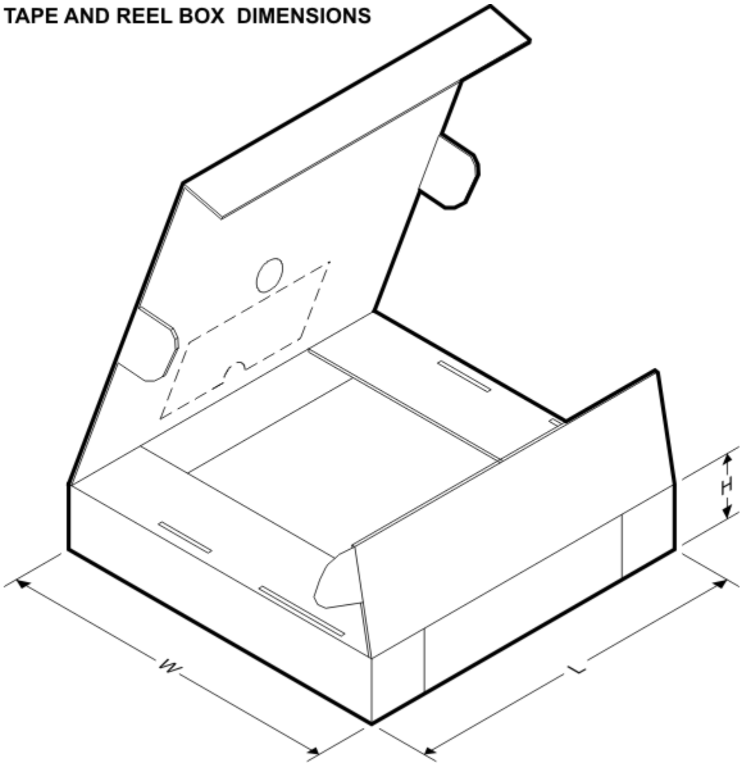
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

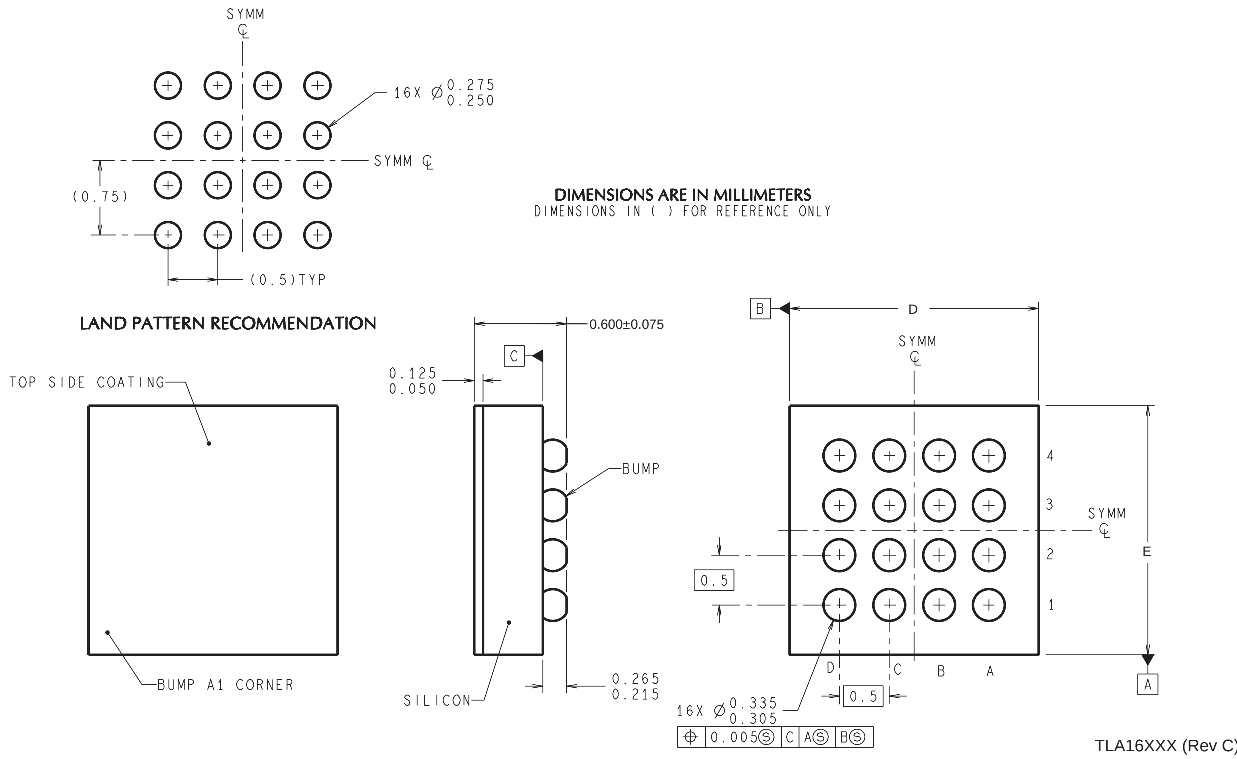
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49120TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM49120TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49120TL/NOPB	DSBGA	YZR	16	250	208.0	191.0	35.0
LM49120TLX/NOPB	DSBGA	YZR	16	3000	208.0	191.0	35.0



D: Max = 1.99 mm, Min = 1.93 mm	
E: Max = 1.99 mm, Min = 1.93 mm	

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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