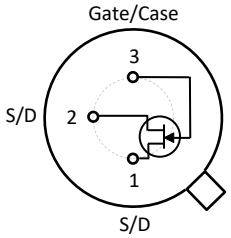
IF4500 N-Channel JFET

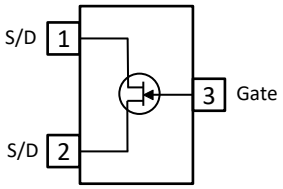
Features

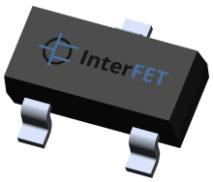
- InterFET N0450L Geometry
- Low noise: 0.85 nV/√Hz typical
- High gain: 65mS typical
- Low gate leakage: 1.5pA typical @10V
- Low $V_{GS(OFF)}$: -1.0 typical
- Typical I_{DSS}: 30mA
- Typical BV_{GSS}: -35V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: InterFET SPICE

TO-18 Bottom View



SOT23 Top View





NOTE: S/D pins are interchangeable Source Drain connections

Industry Standard Crosses

- J110, J110A, 2SK363, MMBFJ110

InterFET Similar Parts

- 2N6550, IF4510, IF4520, IFN363, SMPJ110

InterFET Dual Parts

- IFN860, SMP860

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -20V InterFET IF4500 JFET is targeted for low noise high gain amplifier designs. The IF4500 is ideal for low-voltage supply application with a cutoff voltage of less than -1.5V. The InterFET proprietary JFET recipes result in highest radiation tolerance and lowest leakage JFETs on the market. Custom binning options available.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF4500T72	Through-Hole	TO-72	Bulk
IF4500ST3	Surface Mount	SOT23	Bulk
IF4500ST3TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IF4500COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IF4500CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		TO-18	SOT-23	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	-20	V
I_{FG}	Continuous Forward Gate Current	50	50	mA
P_D	Continuous Device Power Dissipation[1]	500	350	mW
P	Power Derating[1]	3.3	2.8	mW/°C
T_J	Operating Junction Temperature	-65 to 175	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 175	-55 to 150	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

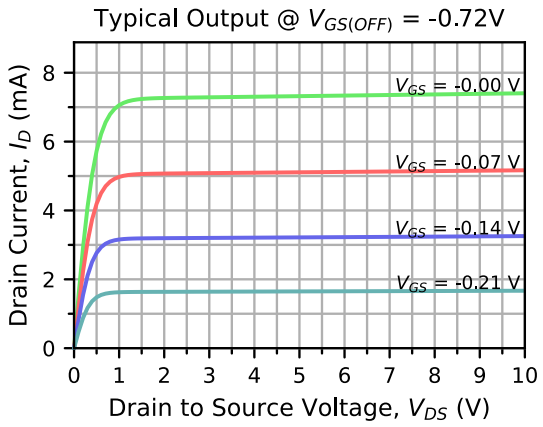
Static Characteristics (@ TA = 25°C, Unless otherwise specified)

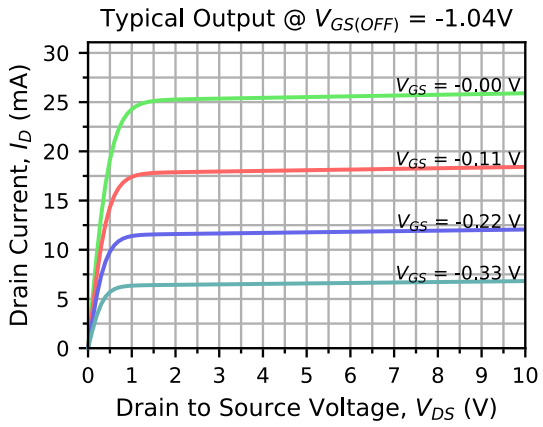
Parameters		Conditions	Min	Typ	Max	Unit
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-20			V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V			-0.1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.5nA	-0.35		-1.5	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 15V (Pulsed)	5	30		mA

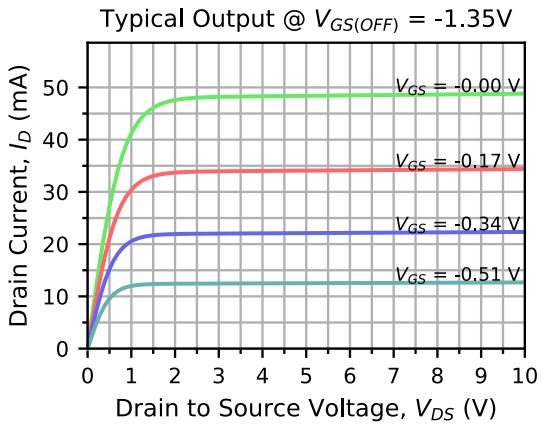
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

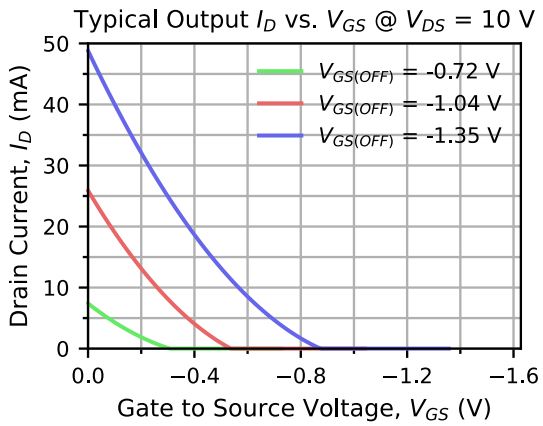
Parameters		Conditions	Min	Typ	Max	Unit
G_{FS}	Forward Transconductance	V_{DS} = 15V, I_D = 5mA, f = 1kHz	15	70		mS
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz			35	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz			15	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 4V, I_D = 5mA, f = 1kHz		0.85		nV/√Hz

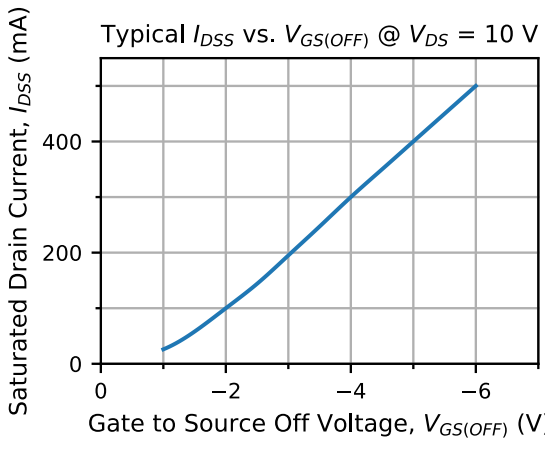
Typical IF4500 Characteristics

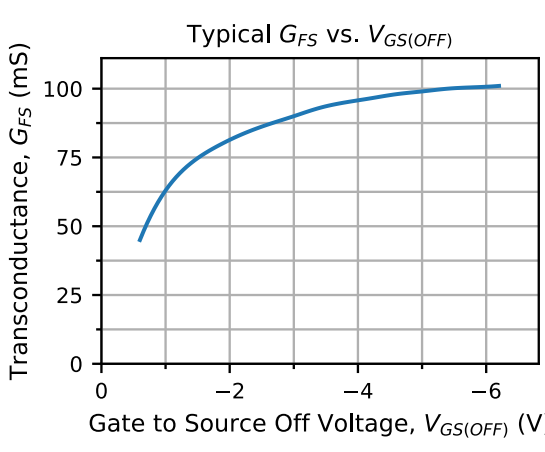




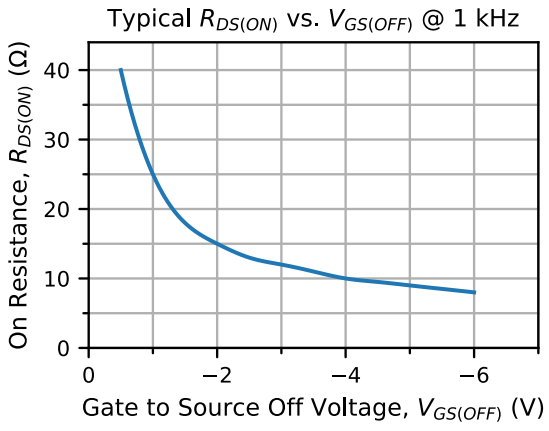


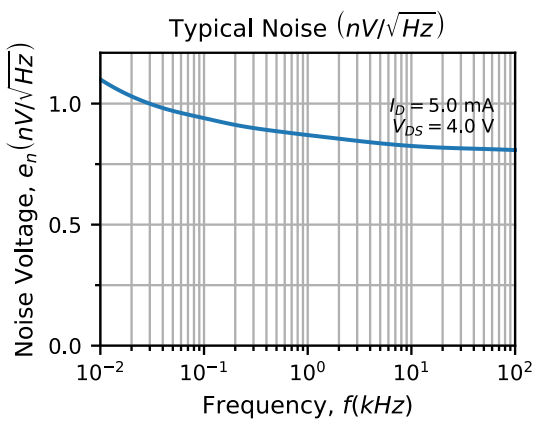


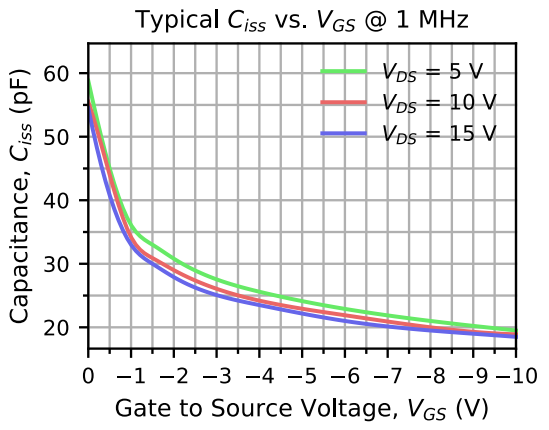


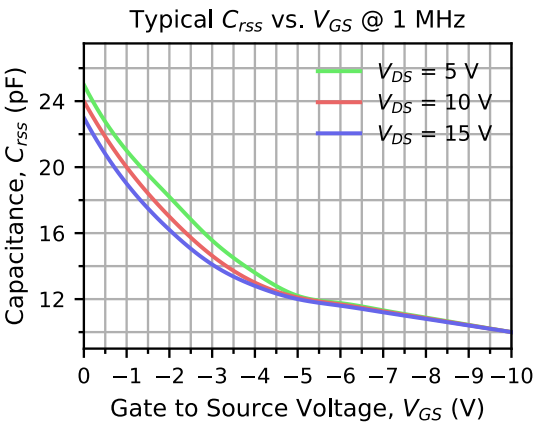


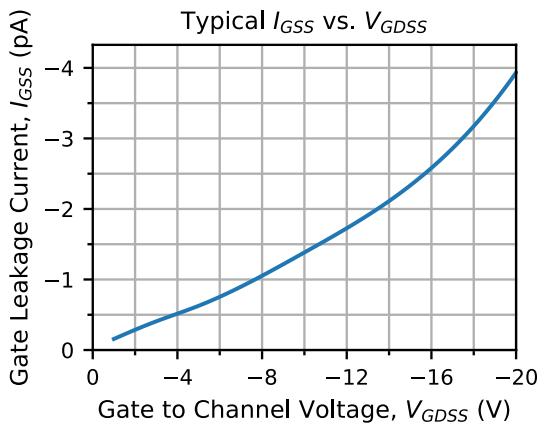
Typical IF4500 Characteristics (Continued)





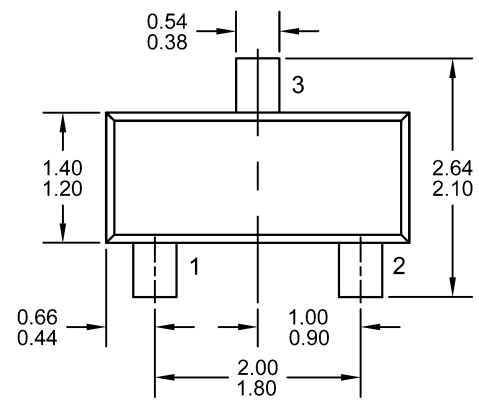


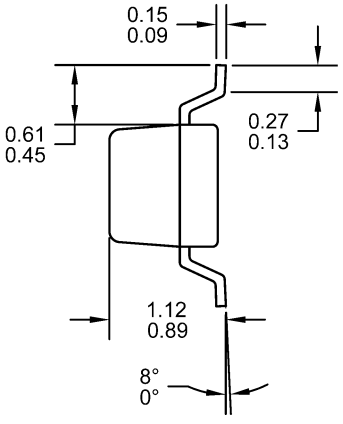


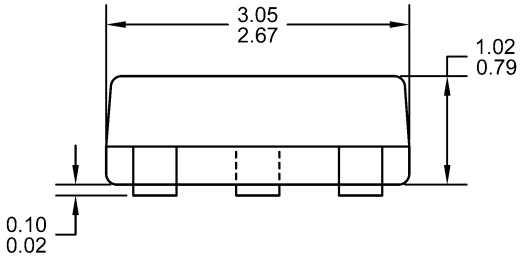


SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

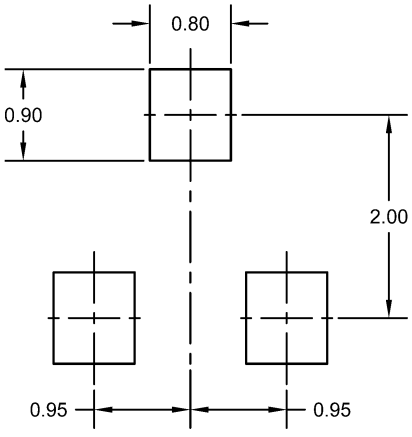






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

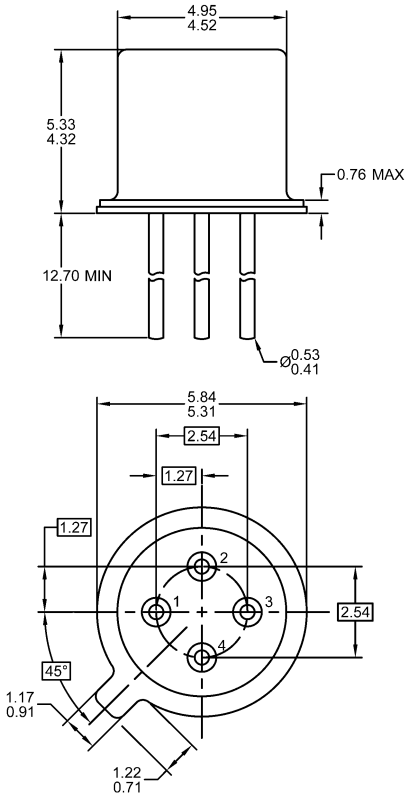
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

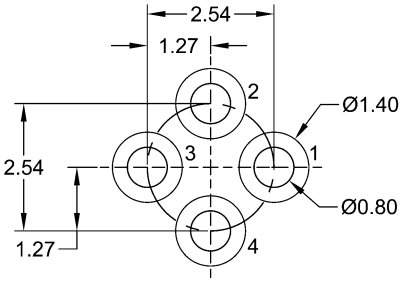
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM

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