## General Description

The 843S304I-100 is a PLL-based clock generator specifically designed for low phase noise applications. This device generates a 100MHz differential LVPECL clock from a input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference is applied to the PCLK pins.

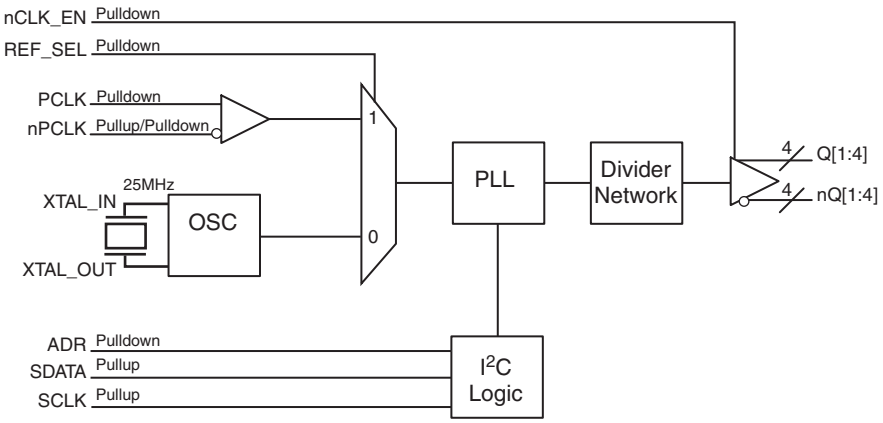
The nominal output frequency of 100MHz may be margined by approximately ±5% by changing the M divider value via the $I^2C$ interface.

The device offers spread spectrum clock output for reduced EMI applications. An $I^2C$ bus interface is used to enable or disable spread spectrum operation as well as set the amount of spread. The 843S304I-100 is available in a lead-free 32-Lead VFQFN package.

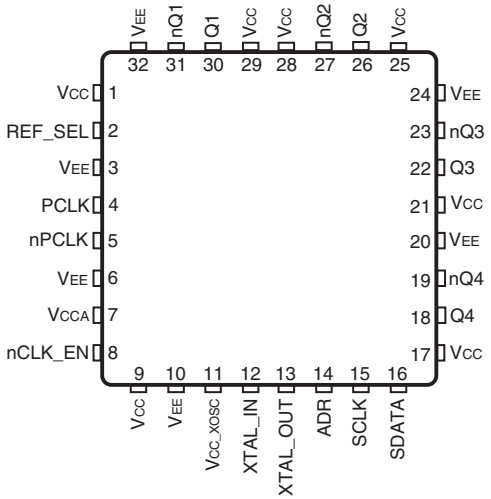
## Features

- Four LVPECL output pairs
- Crystal oscillator interface: 25MHz
- Output frequency: 100MHz
- PCI Express Gen 2 (5 Gb/s) Jitter compliant
- RMS phase jitter @ 100MHz (12kHz – 20MHz): 1.01ps (typical)
- $I^2C$ support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI) reduction
- 3.3V operating supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram




## Pin Assignment




**843S304I-100**
**32-Lead VFQFN**
**5.0mm x 5.0mm x 0.925mm**
**package body**
**K Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 9, 17, 21, 25, 28, 29 | $V_{CC}$ | Power | | Core supply pins. |
| 2 | REF_SEL | Input | Pullup | Select input for XTAL (LOW) or PCLK (HIGH). LVCMOS/LVTTL interface levels. |
| 3, 6,10, 20, 24, 32 | $V_{EE}$ | Power | | Negative supply pins. |
| 4 | PCLK | Input | Pulldown | External 25MHz non-inverted differential reference input. LVPECL input levels. |
| 5 | nPCLK | Input | Pullup/ Pulldown | External 25MHz inverted differential reference input. $V_{CC}/2$ bias voltage when left floating. LVPECL input levels. |
| 7 | $V_{CCA}$ | Power | | Analog supply for PLL. |
| 8 | nCLK_EN | Input | Pulldown | Places clock outputs in active state when Low. Places clock outputs in high-impedance state when High. |
| 11 | $V_{CC\_XOSC}$ | Power | | Power supply for crystal oscillator. recommended to use RC filter as on $V_{CCA}$. |
| 12, 13 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 14 | ADR | Input | Pulldown | $I^2C$ Address select pin. LVCMOS/LVTTL interface levels. |
| 15 | SCLK | Input | Pullup | $I^2C$ compatible SCLK. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels. |
| 16 | SDATA | I/O | Pullup | $I^2C$ compatible SDATA. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels. |
| 18,19 | Q4, nQ4 | Output | | Differential output pair. LVPECL interface levels. |
| 22, 23 | Q3, nQ3 | Output | | Differential output pair. LVPECL interface levels. |
| 26, 27 | Q2, nQ2 | Output | | Differential output pair. LVPECL interface levels. |
| 30, 31 | Q1, nQ1 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 2 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

## I²C Interface - Protocol

The 843S304I-100 uses an I²C slave interface for writing configuration values and reading PLL status bits to and from the on-chip configuration and status registers. This device uses the standard I²C write format for a write transaction, and a standard I²C combined format for a read transaction. *Figure 1* defines the I²C elements of the standard I²C transaction. These elements consist of a Start bit, Data bytes, an Acknowledge or Not-Acknowledge bit and the Stop bit. These elements are arranged to make up the complete I²C transactions as shown in *Figures 2A and 2B.* Figure 2A is a write transaction while Figure 2B is the combined transaction as used for the read. Please refer to the *I²C Bus Specification* for a detailed explanation on I²C operation.

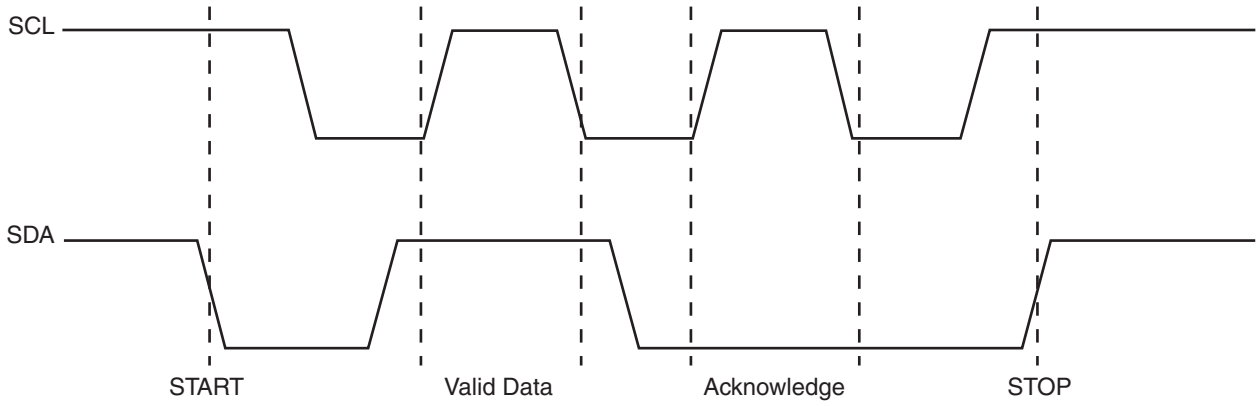



**Figure 1. Standard I²C Transaction**

START (ST) - defined as high-to-low transition on SDA while holding SCL HIGH.

DATA - Between START and STOP cycles, SDA is synchronous with SCL. Data may change only when SCL is LOW and must be stable when SCL is HIGH.

ACKNOWLEDGE (AK) - SDA is driven LOW before the SCL rising edge and held LOW until the SCL falling edge.

STOP (SP) - defined as low-to-high transition on SDA while holding SCL HIGH.

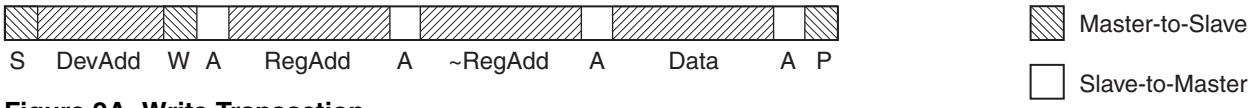



**Figure 2A. Write Transaction**

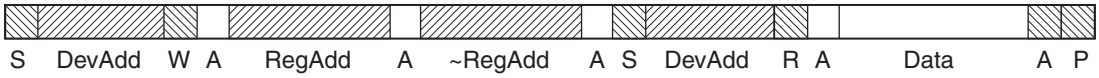



**Figure 2B. Combined Transaction (Read)**

S – Start or Repeated Start

DevAdd – 7 bit Slave Address

The 843S304I-100 also uses an additional register address byte to ensure valid I²C transactions to the device registers. The byte contains the 1's complement of the slave address. This additional address byte is referred to as the Secure I²C interface. This Secure I²C interface can be accessed by most software driver routines that handle standard I²C transactions.

## SECURE I²C Interface Communication

### I²C Write Transaction

An I²C communication write transaction to the 843S304I-100 is initiated by the I²C master sending a start bit. A start bit is a high-to-low transition on the serial data (SDA) input/output line while the serial clock (SCL) input is high. After the start condition, the 7 bit I²C slave-address is sent, MSB first, followed by the read/~write bit. The read/~write bit is set low to indicate a write operation. After receiving the valid I²C slave-address, the slave device, 843S304I-100 responds with an acknowledge (ACK). Next, the master sends the 8 bit register address that is to be accessed by this transaction. Again the 843S304I-100 responds with an acknowledge bit. The master then sends the one's complement of the 8 bit register address. This device again acknowledges. Next the master sends the 8 bit data value to be stored in the previously addressed register. The843S304I-100 will acknowledge and lastly the master will issue a stop.

### I²C Read Transaction

A read operation uses the I²C Combined Transaction. The combined transaction has a direction change from a write to a read in the middle of the transaction, allowing a register address to be sent to the 843S304I-100 and data to be received from the slave device. As with a write, the combined transaction starts with the master sending a start condition and is then followed by the 7 bit slave address, and then followed by the R/~W bit being set for a write. This slave, if properly addressed, will respond with an Acknowledge (A). Next, as with the write transaction, the master sends the 8 bit register address that is to be accessed by this transaction. Once again this device would respond with an acknowledge. The master then sends the one's complement of the 8 bit register address with an acknowledgment from the slave. The master will next send a repeated start bit followed by the slave address and the R/~W bit set to a one which is for a read operation. The 843S304I-100 will acknowledge and then proceed to send the data byte associated with the previously addressed register. The master will acknowledge and then send a stop bit indicating the end of the transaction.

## SYNTHESIZER CONFIGURATION AND I²C PROGRAMMING REGISTERS

The 843S304I-100 uses the Secure I²C interface to configure the internal dividers of the PLL. The Secure I²C interface allows the change of the M dividers, and additionally, may be used to turn on, select the amount, and select the direction of spread spectrum modulation through a series of read/write 8 bit registers. *Table 3* shows the registers, their address, and description of each of the bits in the registers. Some of the bits in these registers are not defined and are ignored on writes and will read-back as zeros on an I²C read transaction. Note, the Command register, which will be described below is a write only register, and an attempted read of this register will result in a NACK or not-acknowledge being returned to the I²C master.

**Table 3. Register Table**

| Register Address | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | Command Register | 1 | nCL | nST | nCP | 0 | CL | ST | CP |
| 01 | Lower M Dividers | M4 | M3 | M2 | M1 | M0 | N/A | N/A | N/A |
| | | | | | | | | | |
| 02 | Upper M Dividers | N/A | N/A | M10 | M9 | M8 | M7 | M6 | M5 |
| | | | | | | | | | |
| 03 | Spread Spectrum Control | N/A | UP | DN | SS4 | SS3 | SS2 | SS1 | SS0 |
| 04 | Status Read Only | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

The 843S304I-100 can be set to decode on of two device I²C slave addresses to minimize the chance of address conflicts on the I²C bus. The specific address that is decoded by the 843S304I-100 is controlled by the setting of the ADR input (pin 14). This input pin determines the value of the I²C address bit A1. See *Table 4* for the slave addresses for the 843S304I-100.

**Table 4. I²C Slave Address Table**

| Bit | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|
| ADR = 0 (default) | 1 | 0 | 1 | 1 | 0 | 0 | 0 | R/W |
| ADR = 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | R/W |

## Writing to and Reading from the Secure I²C Interface

Data is communicated to and from the 843S304I-100 registers using the secure I²C interface. The data is read from or written to a command register and a staging register as shown in *Figure 3.* This diagram shows the relative location of the Command Register, the Staging Register and the Main Register. The main register directly controls the actual PLL operation whose contents is only available through the Staging and Command registers.

The 8 bit command register (address 00) consists of three command bits in the lower nibble and the 1's compliment of those three command bits in the upper nibble. The setting of one of the bits in the lower nibble and the clearing of the 1's complement bit in the upper nibble is used to command either a copy from the Main Register to the Staging register, or a Store from the Staging register to the Main Register, or a Clear of an error flag or flags. All I²C writes to the command register must contain the bitwise compliment of the three lower bits in the three upper bits or the write will be ignored and a NACK will be returned from the 843S304I-100. For example the valid command for the Copy is 1110 0001.

To read the contents of the main register, a command should be sent to copy the contents of the Main register to the Staging register. This command is sent by setting bit D0 (CP) and clearing bit D4 (nCP) with an I²C write of 1110 0001 into the command register (register 00). After this command is sent, the contents of the main register is copied from the Main register to the Staging register and then the resultant data can be read out by the secure I²C interface without affecting the operation of the synthesizer. The data is read by an I²C read transaction to register 01, register 02, register 03 or register 04. A multi-byte read may be performed by using the I²C specified register address as the starting address for a multi-byte read transaction.

In order to store data to the Main register, the data must first be written to the Staging register associated with the desired register address. Following the I²C write into the Staging register, the data can be verified, if desired, by reading back the Staging register with an I²C read transaction. The contents in the Staging register can then be stored into the Main register with a Store command. The Store command is sent by setting bit D1 (ST) and clearing bit D5 (nST) with an I²C write of 1101 0010 into register 00 or the command register. After this command is sent, the contents of the staging register is then stored into the main register, allowing a change in the operation of the synthesizer. A multibyte write to the staging registers may be done with a multibyte I²C write transaction. The register address and 1's complement of the register address used in the I²C transaction will represent the beginning address for the write. The 843S304I-100 will automatically increment the register address such that the multiple bytes are stored in successive register locations.

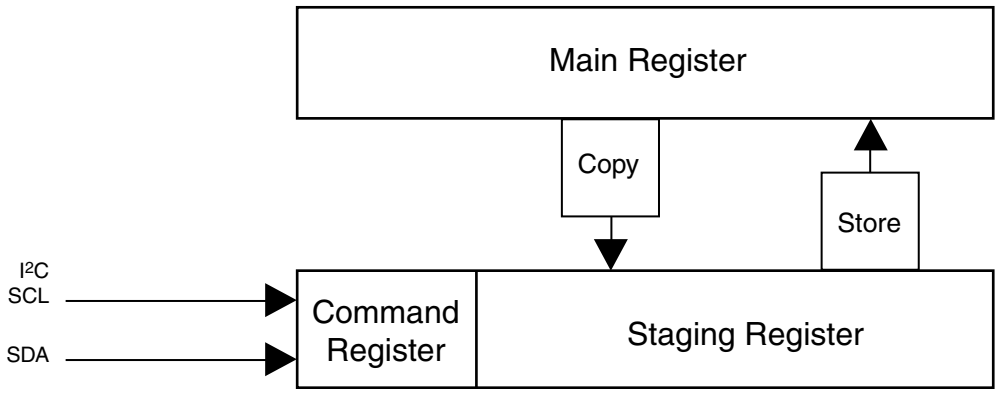



**Figure 3. Writing to and Reading from the Secure I²C Interface**

### SPREAD SPECTRUM OPERATION

Spread Spectrum operation is controlled by $I^2C$ register 03, Spread Spectrum Control Register. Bits D0 – D4 (SS) of the register are a subtrahend to the M-divider for down-spread, and they are an addend and a subtrahend to the M-divider for center-spread. When the UP bit is HIGH, then up-spread has been selected and the M-divider value will toggle between the programmed M value, and M+SS at a 32kHz rate. When the DN bit is HIGH, then down- spread has been selected and the M-divider value will toggle between the programmed M value, and M-SS at a 32kHz rate. When both the UP and DN bits are HIGH, then center-spread has been selected and the M-divider will toggle between M+SS and M-SS at a 32kHz rate. To disable Spread Spectrum operation, program both the UP and DN bits to LOW.

## Programmable Output Frequency Operation

The M value and the required values of M0 through M10 are shown in Table 5 to program the VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $91 \leq M \leq 101$. The frequency out is defined as follows:

$F_{OUT} = f_{VCO}/N = f_{XTAL} \times M/N$

For the 843S304I-100 N = 24.

**Table 5. Programmable VCO Frequency Function Table**

| VCO Frequency (MHz) | M Divide | Output Frequency (MHz) | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | M10 | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 2275 | 91 | 94.792 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 2300 | 92 | 95.833 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| • | • | • | | • | • | • | • | • | • | • | • | • | • |
| 2375 | 95 | 98.958 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 2400 | 96 (default) | 100 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 2425 | 97 | 101.042 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| • | • | • | | • | • | • | • | • | • | • | • | • | • |
| 2500 | 100 | 104.167 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 2525 | 101 | 105.208 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |

### PLL BYPASS

The device will be placed into PLL bypass mode when all the M bits are set to zeros.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 39.5°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 6A. Power Supply DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | $V_{CC}$ – 0.20 | 3.3 | $V_{CC}$ | V |
| $V_{CC\_XOSC}$ | Crystal Oscillator Supply Voltage | | $V_{CC}$ – 0.04 | 3.3 | $V_{CC}$ | V |
| $I_{EE}$ | Power Supply Current | | | | 135 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 20 | mA |
| $I_{CC\_XOSC}$ | Crystal Oscillator Power Supply Current | | | | 4 | mA |

**Table 6B. LVCMOS/LVTTL DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | SDATA, SCLK | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 10 | µA |
| | | REF_SEL, ADR, nCLK_EN | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | SDATA, SCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| | | REF_SEL, ADR, nCLK_EN | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | µA |

**Table 6C. LVPECL DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C)

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | PCLK, nPCLK | $V_{CC} = V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | µA |
| | | nPCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.3 | | 1.0 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 1.5 | | $V_{CC}$ | V |
| $V_{OH}$ | Output High Voltage; NOTE 3 | | | $V_{CC}$ – 1.3 | | $V_{CC}$ – 0.8 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 3 | | | $V_{CC}$ – 2.0 | | $V_{CC}$ – 1.6 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | | 0.6 | | 1.0 | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as $V_{IH}$.
NOTE 3: Outputs terminated with 50Ω to $V_{CC}$ – 2V.

**Table 7. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

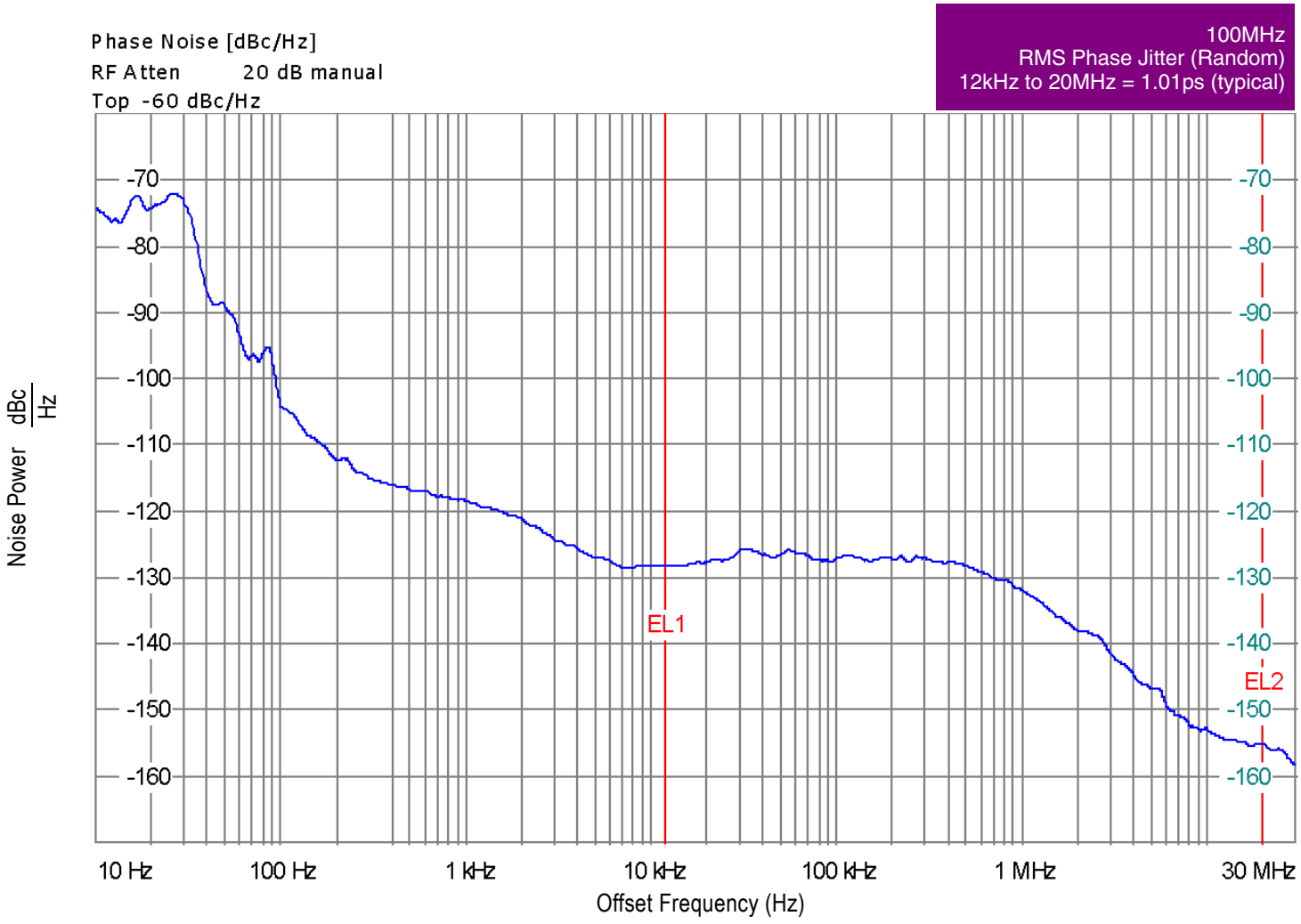
## AC Electrical Characteristics

**Table 8. AC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

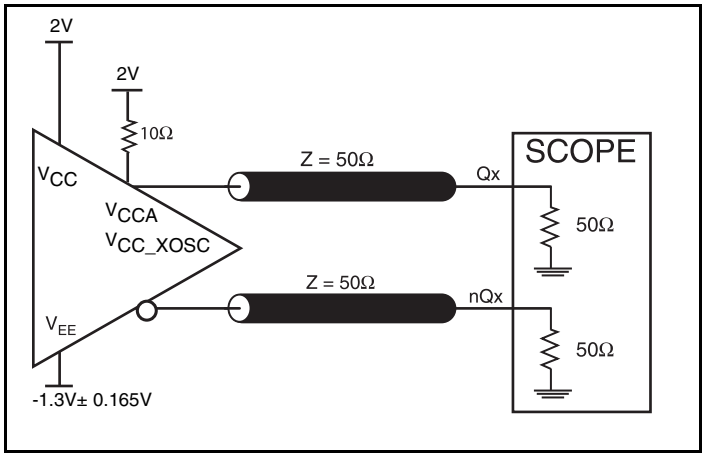
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | 95 | | 105 | MHz |
| $f_{REF}$ | Reference Frequency | | | 25 | | MHz |
| $t_{jit}(Ø)$ | Phase Jitter, RMS (Random); NOTE 1 | 100MHz, SSC Off<br>Integration Range: 12kHz – 20MHz | | 1.01 | | ps |
| $t_{REFCLK\_HF\_RMS}$ | Phase Jitter, RMS; NOTE 2 | 25MHz crystal input, SSC Off<br>High Band: 1.5MHz - Nyquist (clock frequency/2) | | 2.2 | | ps |
| $t_{REFCLK\_LF\_RMS}$ | Phase Jitter, RMS; NOTE 2 | 25MHz crystal input, SSC Off<br>Low Band: 10kHz - 1.5MHz | | 0.2 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 600 | | 900 | ps |
| odc | Output Duty Cycle | | 49 | | 51 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to phase noise plot.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps rms for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0 ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band). See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.

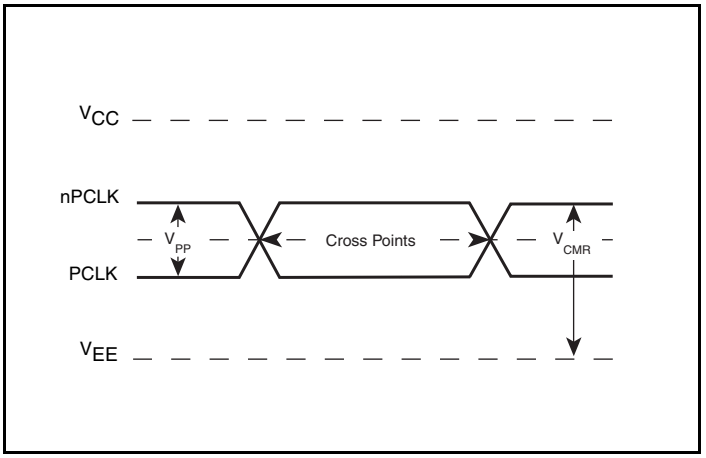
## Typical Phase Noise



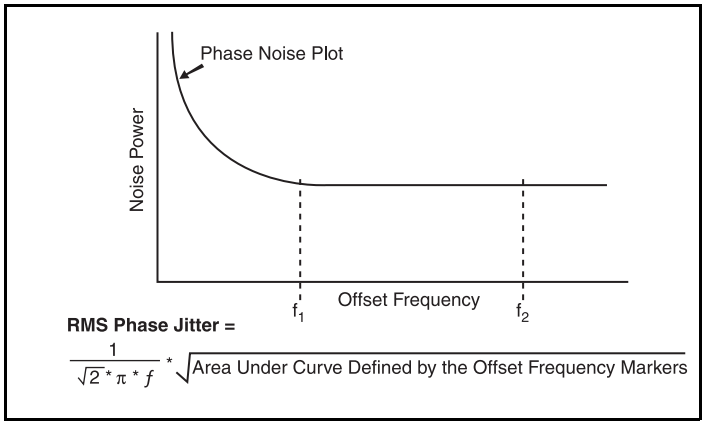
## Parameter Measurement Information



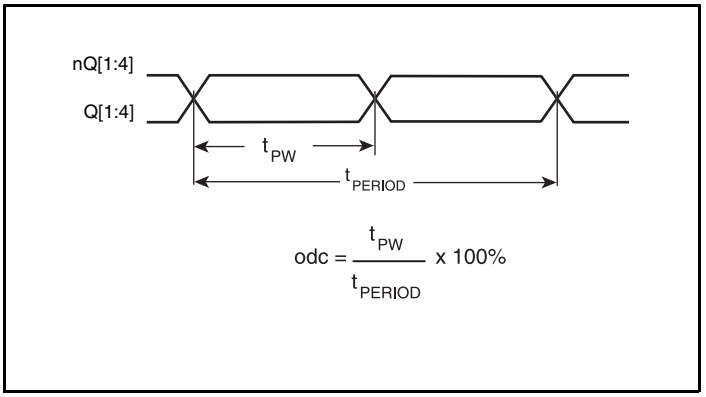

**3.3V LVPECL Output Load AC Test Circuit**



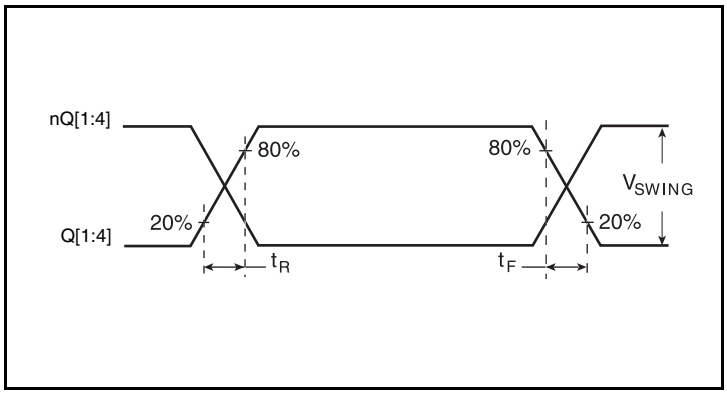

**Differential Input Level**




**RMS Phase Jitter**




**Output Duty Cycle/Pulse Width/Period**




**Output Rise/Fall Time**

# Application Information

## Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843S304I-100 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$ ,$V_{CC\_XOSC}$ and $V_{CCA}$ should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 4* illustrates this for a generic $V_{CC}$ pin and also shows that $V_{CCA}$ requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the $V_{CCA}$ pin.

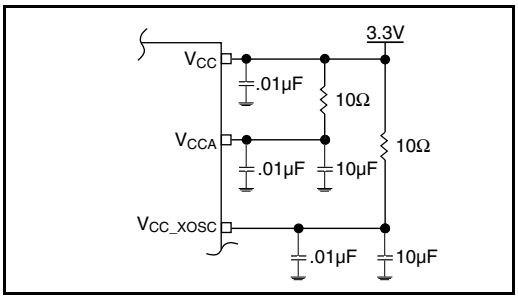



**Figure 4. Power Supply Filtering**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The 843S304I-100 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 5* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

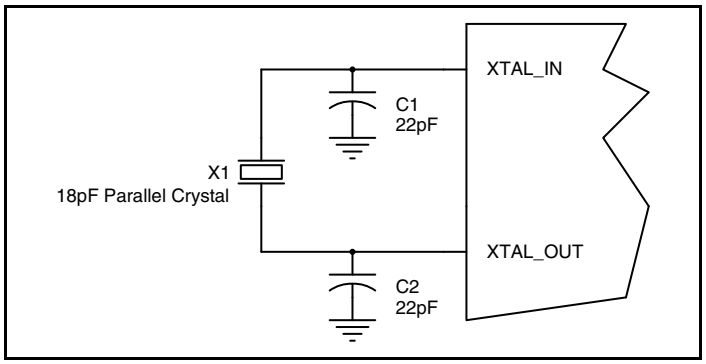



**Figure 5. Crystal Input Interface**

## LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 6.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

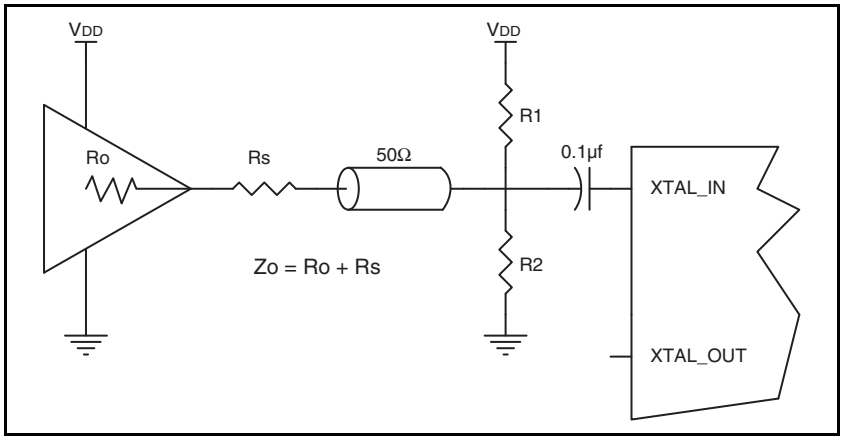



**Figure 6. General Diagram for LVCMOS Driver to XTAL Input Interface**

## LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 7A to 7E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

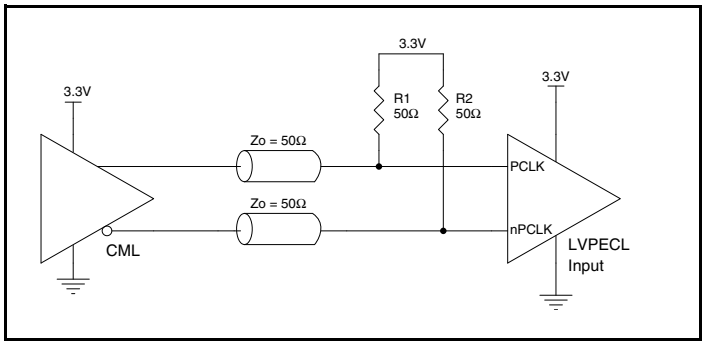



**Figure 7A. HiPerClockS PCLK/nPCLK Input Driven by a CML Driver**

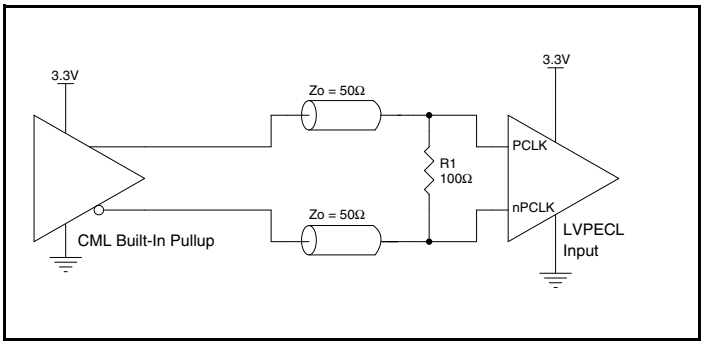



**Figure 7B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver**

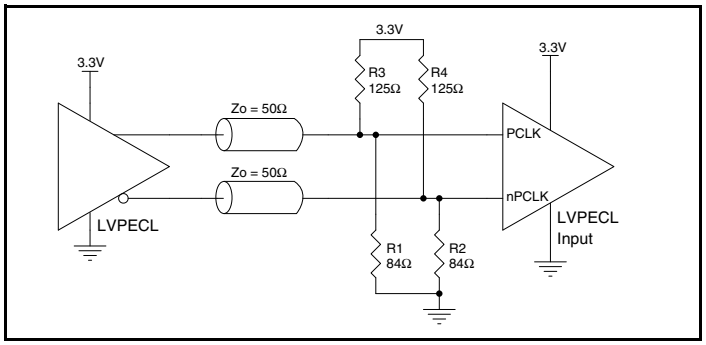



**Figure 7C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**

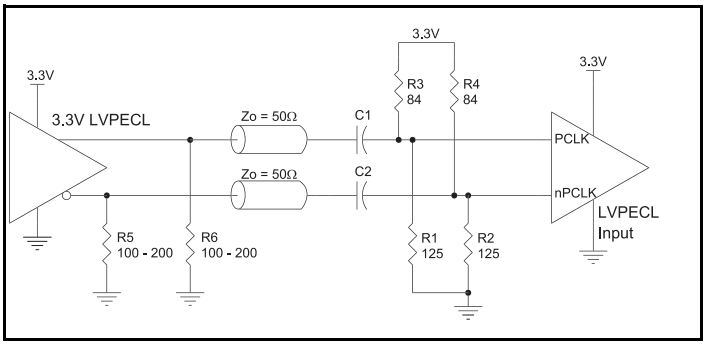



**Figure 7D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**

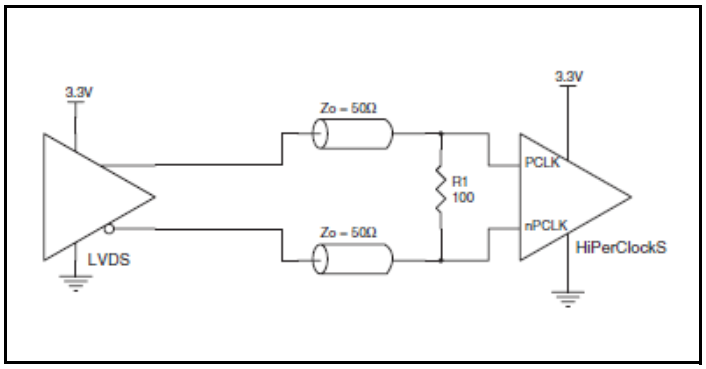



**Figure 7E. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

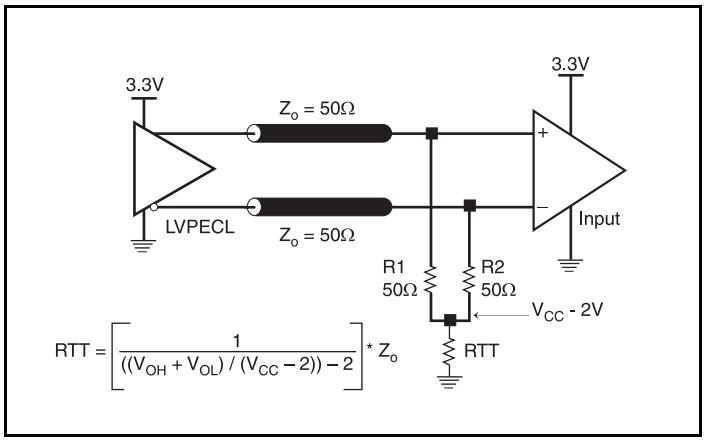



**Figure 8A. 3.3V LVPECL Output Termination**

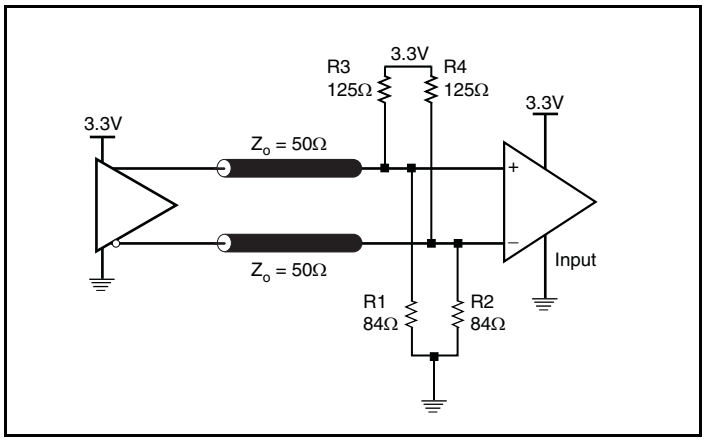



**Figure 8B. 3.3V LVPECL Output Termination**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 9.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

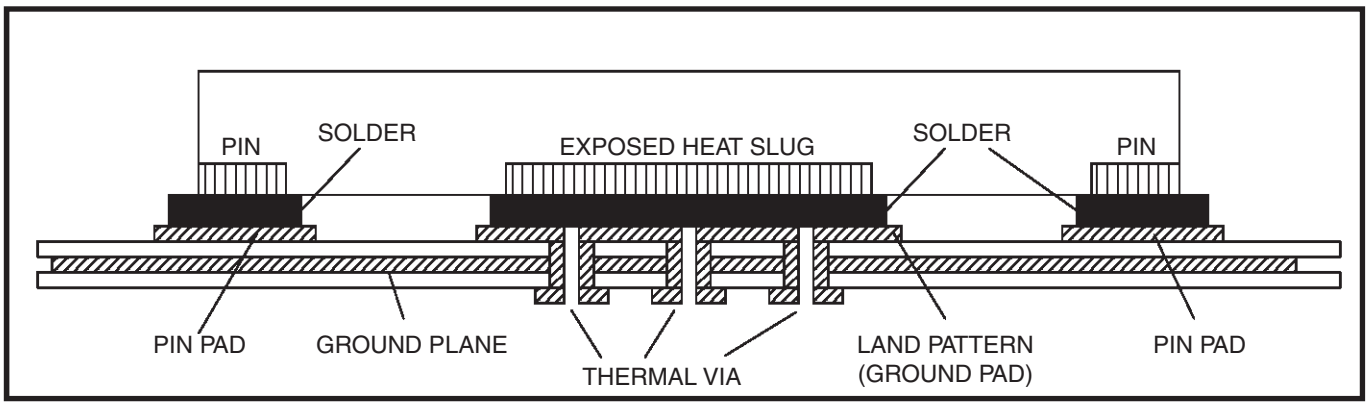
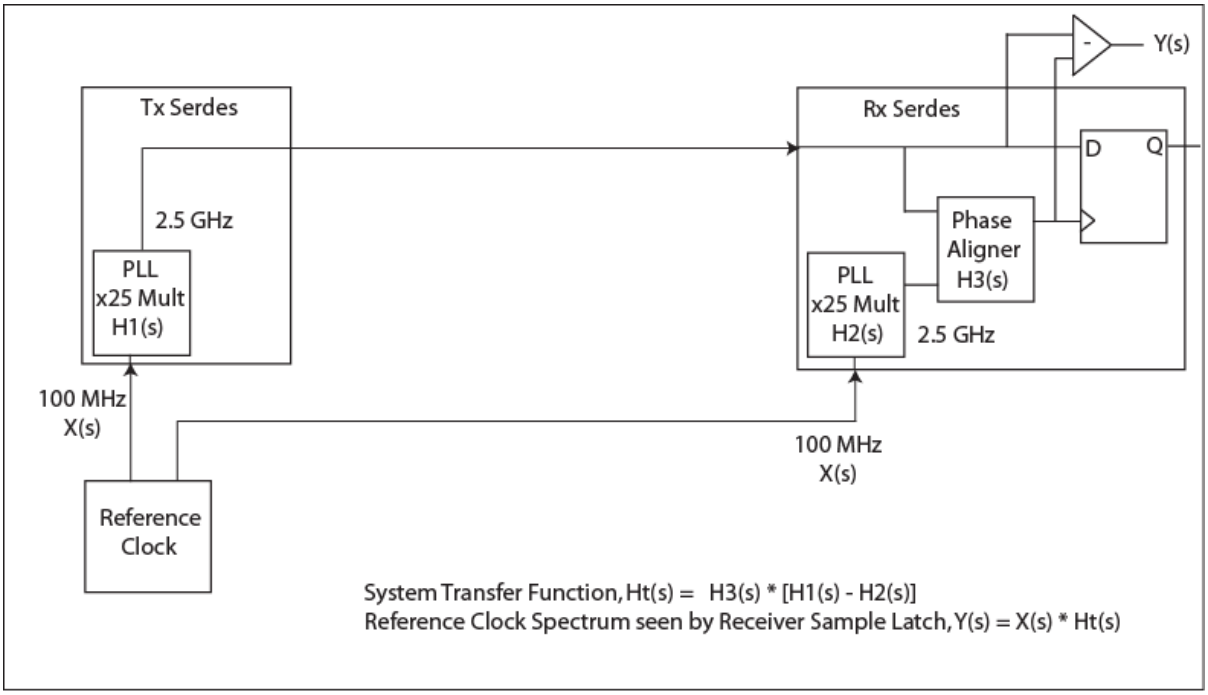



**Figure 9. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The below block diagram shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.




In the jitter analysis, the Tx and Rx serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

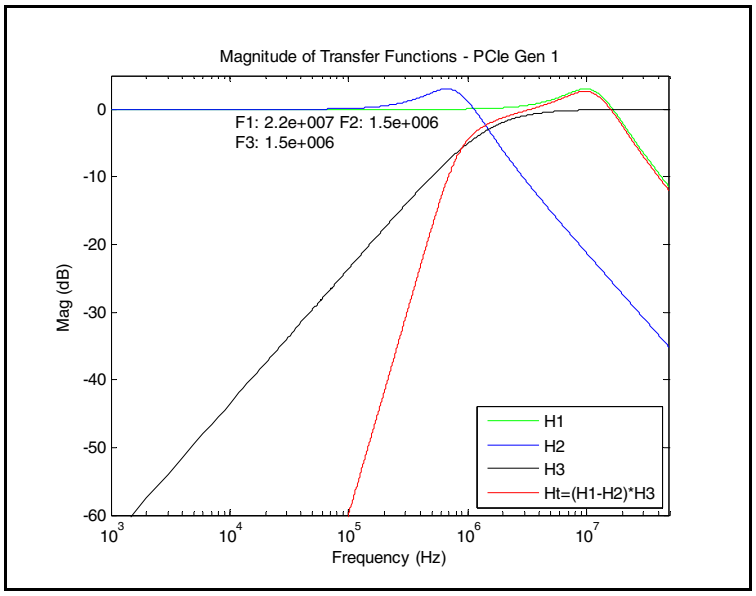
$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

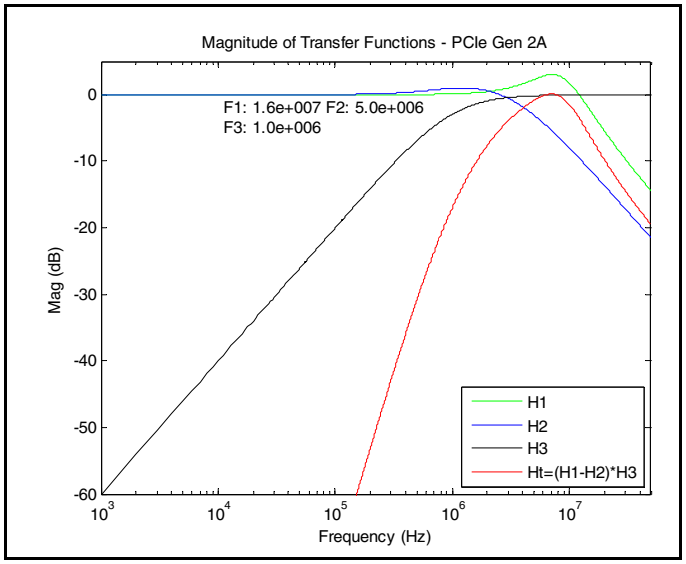
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].

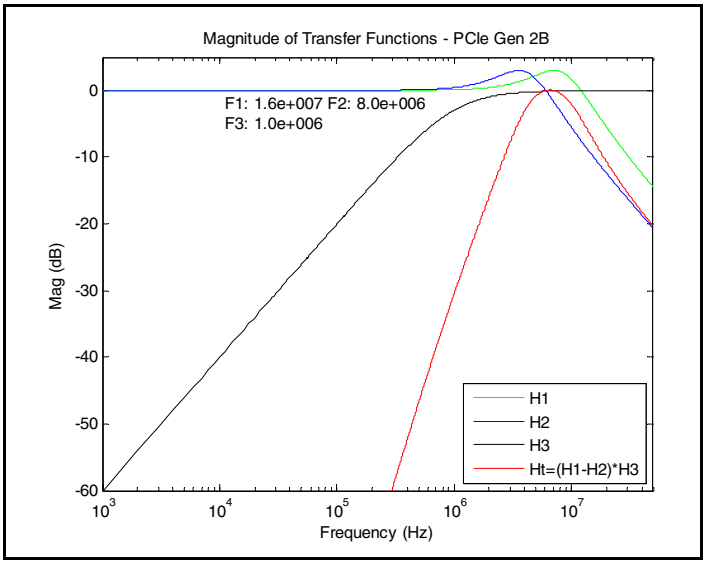
For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz to 50MHz) and the jitter result is reported in peak-peak. For PCI Express Gen 2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz - 1.5MHz (Low Band) and 1.5MHz - Nyquist (High Band). The below plots show the individual transfer functions as well as the overall transfer function Ht. The respective -3 dB pole frequencies for each transfer function are labeled as F1 for transfer function H1, F2 for H2, and F3 for H3. For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*




**PCIe Gen 1 Magnitude of Transfer Function**




**PCIe Gen 2A Magnitude of Transfer Function**




**PCIe Gen 2B Magnitude of Transfer Function**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 843S304I-100.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 843S304I-100 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 135mA = **467.775mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 32mW = **128mW**

**Total Power**$_{\_MAX}$ (3.3V, with all outputs switching) = 467.775mW + 128mW = **595.775mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.596W * 39.5°C/W = 108.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 9. Thermal Resistance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

The LVPECL output driver circuit and termination are shown in *Figure 10.*

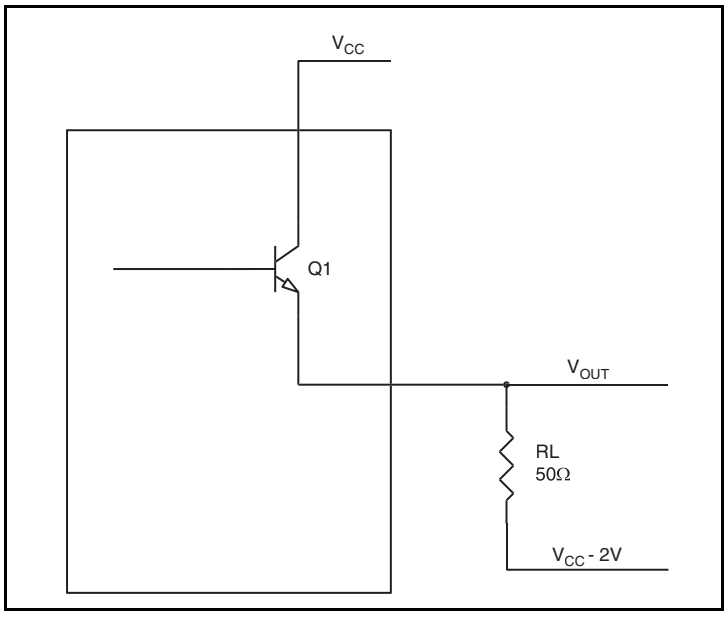



**Figure 10. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.6V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

# Reliability Information

**Table 10. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN**

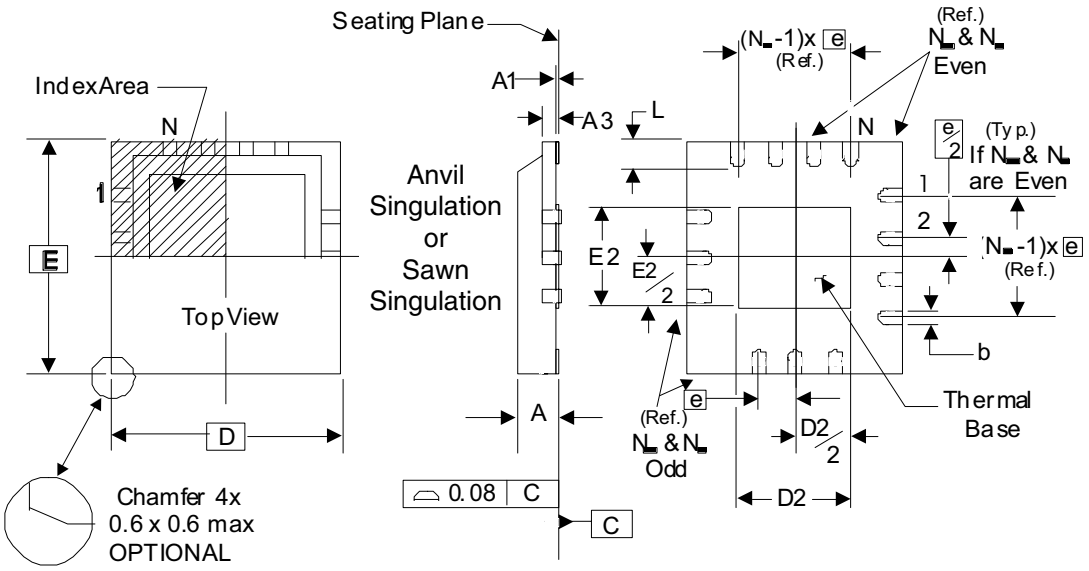
| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

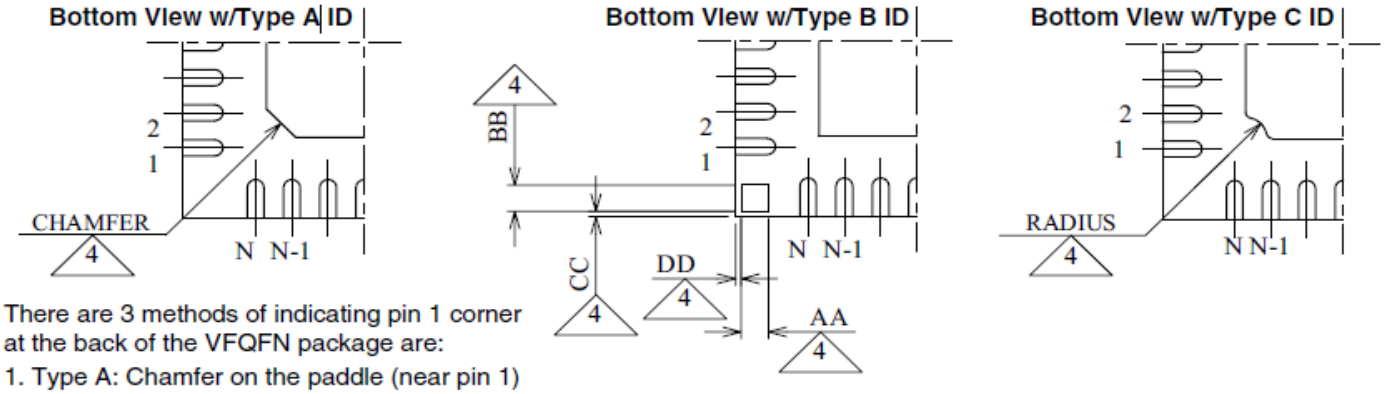
## Transistor Count

The transistor count for 843S304I-100 is: 12,787

# Package Outline and Package Dimensions

### Package Outline - K Suffix for 32 Lead VFQFN




There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

**Table 11. Package Dimensions**

| JEDEC Variation: VHHD-2/-4<br>All Dimensions in Millimeters | | | |
|---|---|---|---|
| **Symbol** | **Minimum** | **Nominal** | **Maximum** |
| **N** | | 32 | |
| **A** | 0.80 | | 1.00 |
| **A1** | 0 | | 0.05 |
| **A3** | | 0.25 Ref. | |
| **b** | 0.18 | 0.25 | 0.30 |
| **$N_D$ & $N_E$** | | | 8 |
| **D & E** | | 5.00 Basic | |
| **D2 & E2** | 3.0 | | 3.3 |
| **e** | | 0.50 Basic | |
| **L** | 0.30 | 0.40 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 11.

# Ordering Information

**Table 12. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 843S304BKI-100LF | ICS04BI100L | “Lead-Free” 32 Lead VFQFN | Tray | -40°C to 85°C |
| 843S304BKI-100LFT | ICS04BI100L | “Lead-Free” 32 Lead VFQFN | Tape & Reel | -40°C to 85°C |

## Revision History

| Revision Date | Description of Change |
|---|---|
| January 5, 2016 | ▪ General Description -Removed ICS Chip.<br>▪ Ordering Information - Removed quantity from Tape and Reel and note from below the table.<br>▪ Updated the header and footer. |

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