UFS Series N-Channel IGBT
70 A, 600 V

HGTG40N60B3

The HGTG40N60B3 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on−state conduction loss of a bipolar transistor. The much lower on−state voltage drop varies only moderately between 25°C and 150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

Formerly Developmental Type TA49052.

Features

- 70 A, 600 V, T_C = 25°C
- 600 V Switching SOA Capability
- Typical Fall Time: 100 ns at T_J = 150°C
- Short Circuit Rating
- Low Conduction Loss
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Packing

JEDEC STYLE TO-247

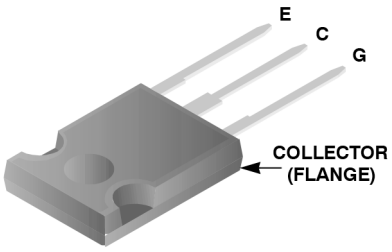

Figure 1.

ON Semiconductor®

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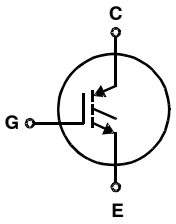
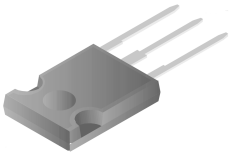
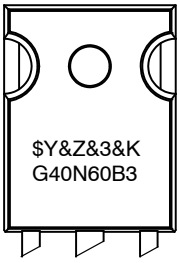




TO−247−3LD
CASE 340CK

MARKING DIAGRAMS



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
G40N60B3	= Specific Device Code

ORDERING INFORMATION

Part Number	Package	Brand
HGTG40N60B3	TO−24	G40N60B3

ABSOLUTE MAXIMUM RATINGS T_C = 25°C Unless Otherwise Specified

Description	Symbol	Ratings	Units
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous At T_C = 25°C At T_C = 110°C	 I_{C25} I_{C110}	 70 40	A
Collector Current Pulsed (Note 1)	I_{CM}	330	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at T_J = 150°C, Figure 3	SSOA	100 A at 600 V	
Power Dissipation Total at T_C = 25°C Power Dissipation Derating T_C > 25°C	P_D	290 2.33	W W/°C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	−55 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at V_{GE} = 15 V	t_{SC}	2	μs
Short Circuit Withstand Time (Note 2) at V_{GE} = 10 V	t_{SC}	10	μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)}$ = 360 V, T_J = 125°C, R_G = 3 Ω.

ELECTRICAL SPECIFICATIONS T_C = 25°C Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
BV_{CES}	Collector to Emitter Breakdown Voltage	I_C = 250 μA, V_{GE} = 0 V		600	–	–	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_C = −10 mA, V_{GE} = 0 V		20	–	–	V
I_{CES}	Collector to Emitter Leakage Current	V_{CE} = BV_{CES}	T_C = 25°C	–	–	100	μA
		V_{CE} = BV_{CES}	T_C = 150°C	–	–	6.0	mA
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = I_{C110}, V_{GE} = 15 V	T_C = 25°C	–	1.4	2.0	V
			T_C = 150°C	–	1.5	2.3	V
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_C = 250 μA, V_{CE} = V_{GE}		3.0	4.8	6.0	V
I_{GES}	Gate to Emitter Leakage Current	V_{GE} = ±20 V		–	–	±100	nA
SSOA	Switching SOA	T_J = 150°C R_G = 3 Ω V_{GE} = 15 V L = 100 μH	V_{CE} = 480 V	200	–	–	A
			V_{CE} = 600 V	100	–	–	A
V_{GEP}	Gate to Emitter Plateau Voltage	I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}		–	7.5	–	V
$Q_{G(ON)}$	On−State Gate Charge	I_C = IC110, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15 V	–	250	330	nC
			V_{GE} = 20 V	–	335	435	nC
$t_{d(ON)I}$	Current Turn−On Delay Time	IGBT and Diode Both at T_J = 25°C I_{CE} = I_{C110} V_{CE} = 0.8 BV_{CES} V_{GE} = 15 V R_G = 3 Ω L = 100 μH Test Circuit (Figure 18)		–	47	–	ns
t_{rI}	Current Rise Time			–	35	–	ns
$t_{d(OFF)I}$	Current Turn−Off Delay Time			–	170	200	ns
t_{fI}	Current Fall Time			–	50	100	ns
E_{ON}	Turn−On Energy			–	1050	1200	μJ
E_{OFF}	Turn−Off Energy (Note 3)			–	800	1400	μJ
$t_{d(ON)I}$	Current Turn−On Delay Time	IGBT and Diode Both at T_J = 150°C I_{CE} = I_{C110} V_{CE} = 0.8 BV_{CES} V_{GE} = 15 V R_G = 3 Ω L = 100 μH Test Circuit (Figure 17)		–	47	–	ns
t_{rI}	Current Rise Time			–	35	–	ns
$t_{d(OFF)I}$	Current Turn−Off Delay Time			–	285	375	ns
t_{fI}	Current Fall Time			–	100	175	ns
E_{ON}	Turn−On Energy			–	1850	–	μJ
E_{OFF}	Turn−Off Energy (Note 3)			–	2000	–	μJ
$R_{\theta JC}$	Thermal Resistance Junction To Case			–	–	0.43	°C/W

3. Turn−Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0 A). All devices were tested per JEDEC Standard No. 24−1 Method for Measurement of Power Device Turn−Off Switching Loss. This test method produces the true total Turn−Off Energy Loss. Turn−On losses include losses due to diode recovery.

TYPICAL PERFORMANCE CURVES (continued)

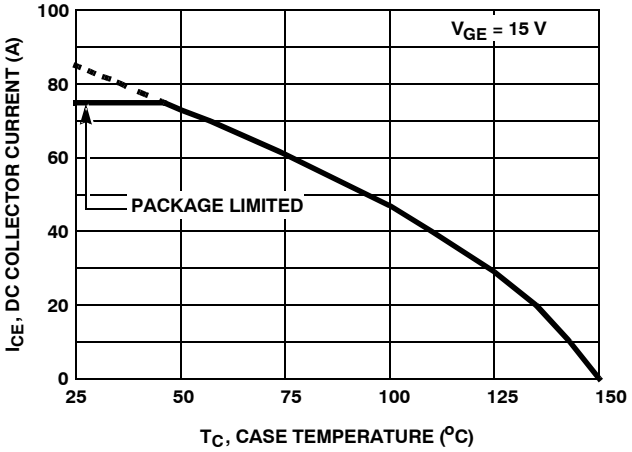


Figure 2. DC COLLECTOR CURRENT vs CASE TEMPERATURE

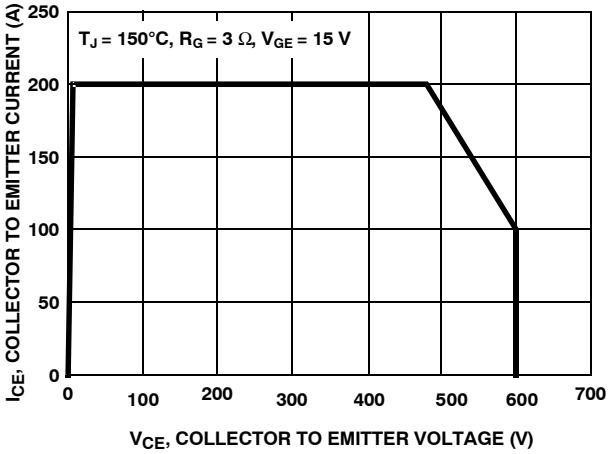


Figure 3. MINIMUM SWITCHING SAFE OPERATING AREA

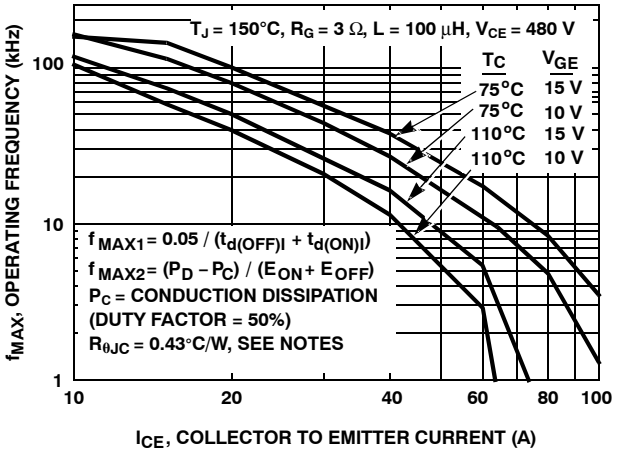


Figure 4. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

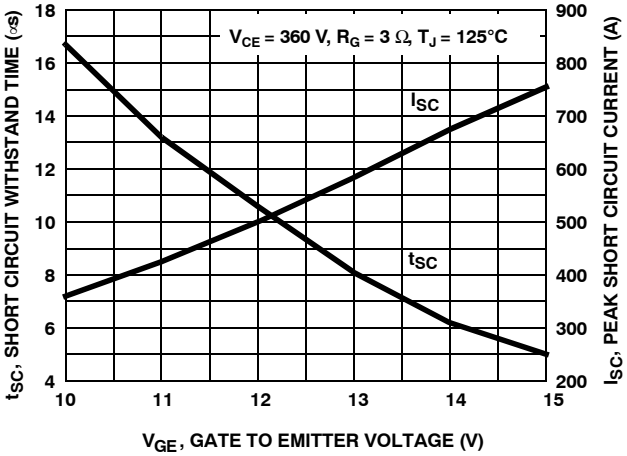


Figure 5. SHORT CIRCUIT WITHSTAND TIME

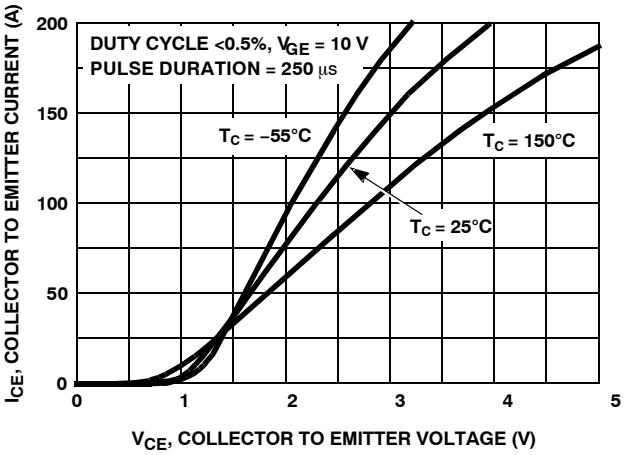


Figure 6. COLLECTOR TO EMITTER ON STATE VOLTAGE

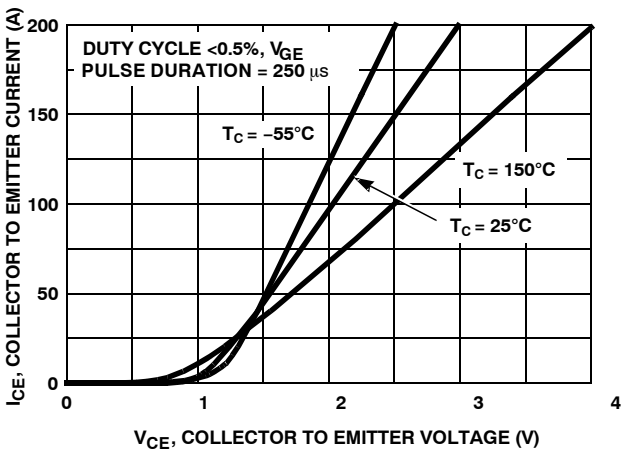


Figure 7. COLLECTOR TO EMITTER ON STATE VOLTAGE

TYPICAL PERFORMANCE CURVES (continued)

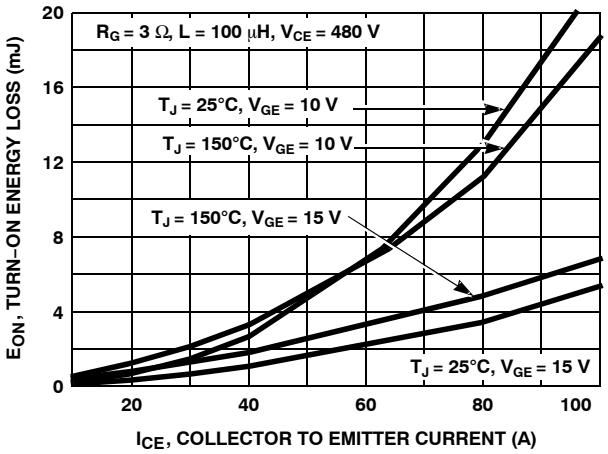


Figure 8. TURN−ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

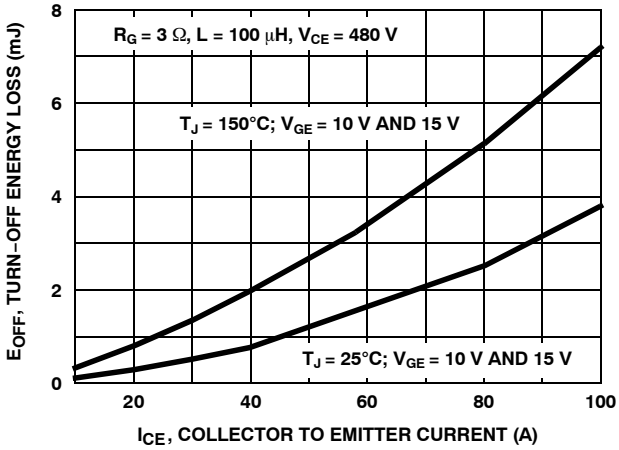


Figure 9. TURN−OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

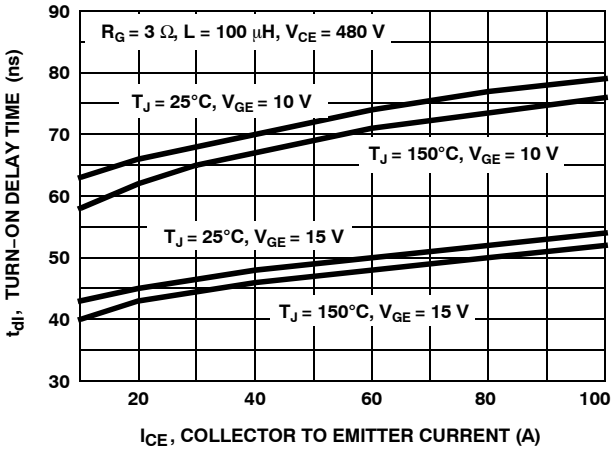


Figure 10. TURN−ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

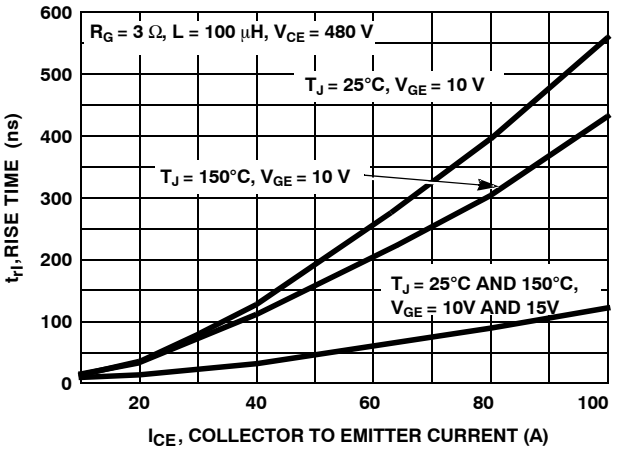


Figure 11. TURN−ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

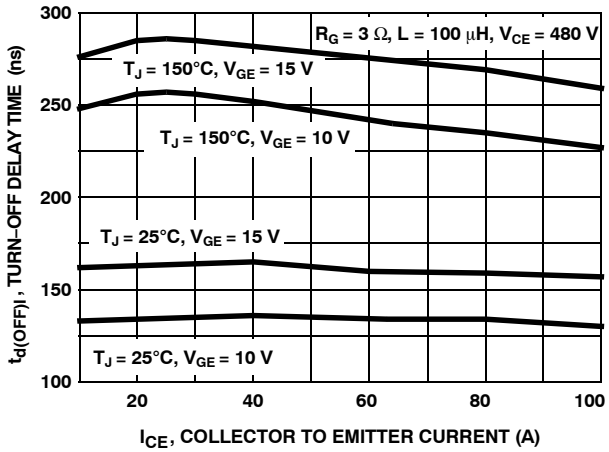


Figure 12. TURN−OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

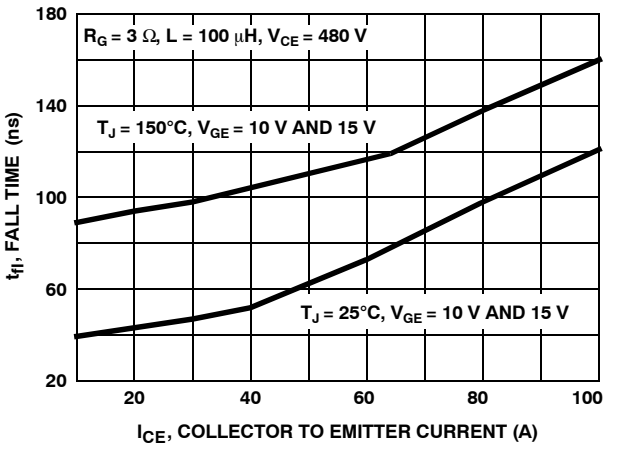


Figure 13. FALL TIME vs COLLECTOR TO EMITTER CURRENT

TYPICAL PERFORMANCE CURVES (continued)

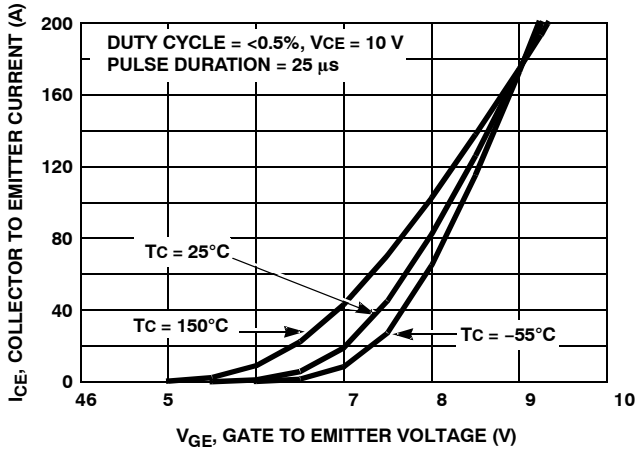


Figure 14. TRANSFER CHARACTERISTIC

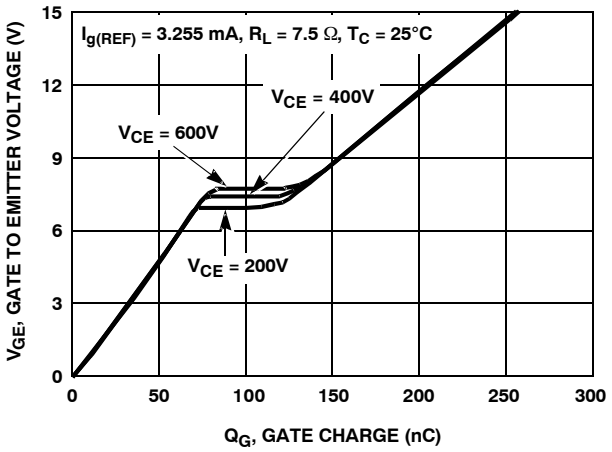


Figure 15. GATE CHARGE WAVEFORM

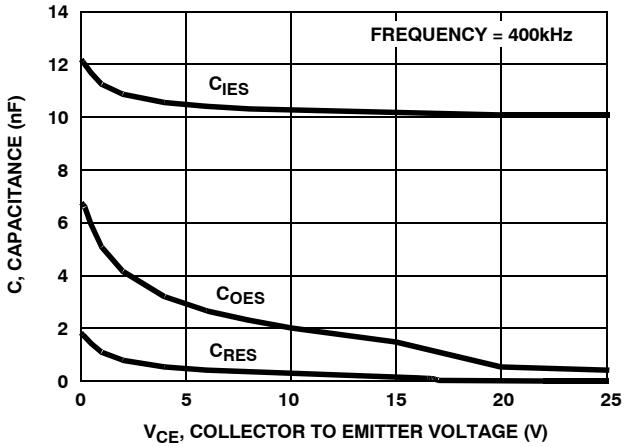


Figure 16. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

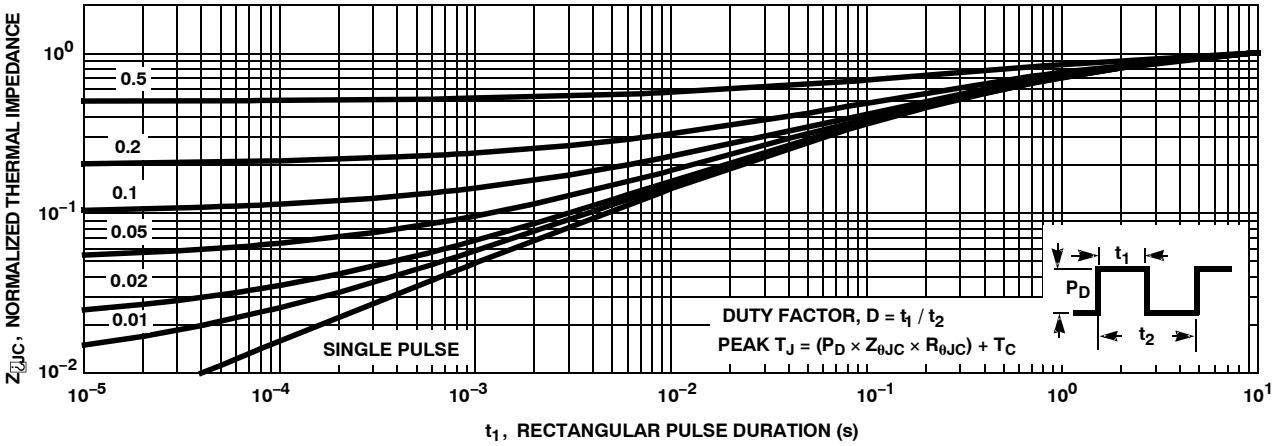


Figure 17. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

Test Circuit and Waveform

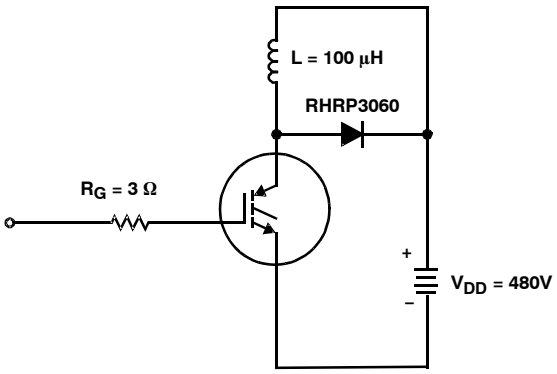


Figure 18. INDUCTIVE SWITCHING TEST CIRCUIT

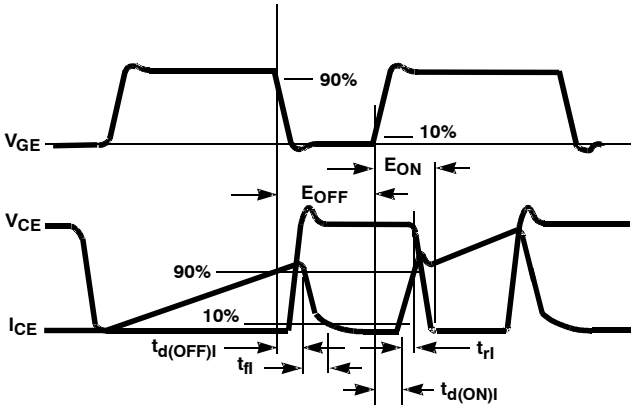


Figure 19. SWITCHING TEST WAVEFORM

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate−insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD LD26" or equivalent
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means − for example, with a metallic wristband
3. Tips of soldering irons should be grounded
4. Devices should never be inserted into or removed from circuits with power on
5. Gate Voltage Rating − Never exceed the gate−voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region
6. Gate Termination − The gates of these devices are essentially capacitors. Circuits that leave the gate open−circuited or floating should be avoided. These conditions can result in turn−on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup
7. Gate Protection − These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended

Operating Frequency Information

Operating frequency information for a typical device (Figure 4) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 6 to 11. The operating frequency plot (Figure 4) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on−state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 19. Device turn−off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 4) and the conduction losses (PC) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

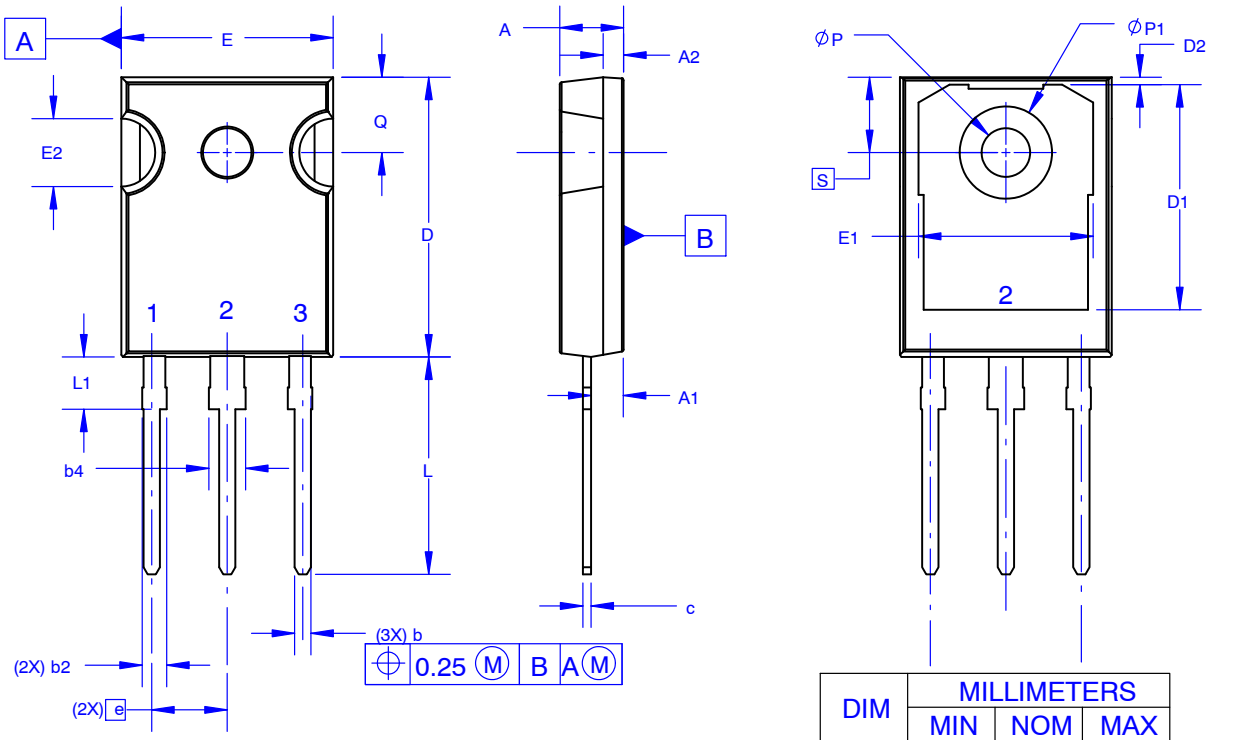
E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn−on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn−off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019

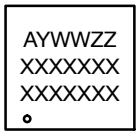


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13851G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−247−3LD SHORT LEAD**	**PAGE 1 OF 1**

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