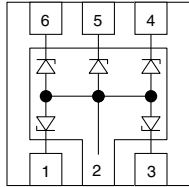
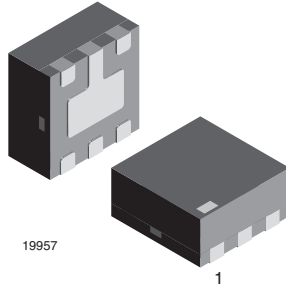


## 5-Line ESD Protection Diode Array in LLP75-6L



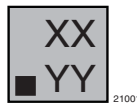
19956



19957

1

### MARKING (example only)



Dot = pin 1 marking

XX = date code

YY = type code (see table below)

### DESIGN SUPPORT TOOLS

[click logo to get started](#)

### FEATURES

- Ultra compact LLP75-6L package
- Low package profile < 0.6 mm
- 5-line ESD protection
- Low leakage current  $I_R < 0.1 \mu A$
- Low load capacitance of typ. 43 pF at  $V_R = 0 V$
- ESD immunity acc. IEC 61000-4-2  
± 30 kV contact discharge  
± 30 kV air discharge
- Working voltage range  $V_{RWM} = 5 V$
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**  
**GREEN**  
 (5-2008)

### ORDERING INFORMATION

| DEVICE NAME | ORDERING CODE    | TAPED UNITS PER REEL<br>(8 mm TAPE ON 7" REEL) | MINIMUM ORDER QUANTITY |
|-------------|------------------|--|------------------------|
| GMF05LC-HSF | GMF05LC-HSF-GS08 | 3000   | 15 000                 |

### PACKAGE DATA

| DEVICE NAME | PACKAGE NAME | TYPE CODE | WEIGHT | MOLDING COMPOUND<br>FLAMMABILITY RATING | MOISTURE<br>SENSITIVITY LEVEL        | SOLDERING CONDITIONS         |
|-------------|--------------|-----------|--------|---|--------------------------------------|------------------------------|
| GMF05LC-HSF | LLP75-6L     | 1B        | 4.2 mg | UL 94 V-0                               | MSL level 1<br>(according J-STD-020) | Peak temperature max. 260 °C |

### ABSOLUTE MAXIMUM RATINGS GMF05LC-HSF

| PARAMETER             | TEST CONDITIONS  | SYMBOL               | VALUE       | UNIT |
|-----------------------|--|----------------------|-------------|------|
| Peak pulse current    | BiAs-mode: each input (pin 1; 3 to pin 6) to ground (pin 2);<br>acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot | $I_{PPM}$            | 5           | A    |
| Peak pulse power      | BiAs-mode: each input (pin 1; 3 to pin 6) to ground (pin 2);<br>acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot | $P_{PP}$             | 70          | W    |
| ESD immunity          | BiAs-mode: each input (pin 1; 3 to pin 6) to<br>ground (pin 2);<br>acc. IEC 61000-4-2; 10 pulses                     | Contact<br>discharge | ± 30        | kV   |
|                       |  | Air<br>discharge     | ± 30        | kV   |
| Operating temperature | Junction temperature   | $T_J$                | -55 to +125 | °C   |
| Storage temperature   |  | $T_{STG}$            | -55 to +150 | °C   |

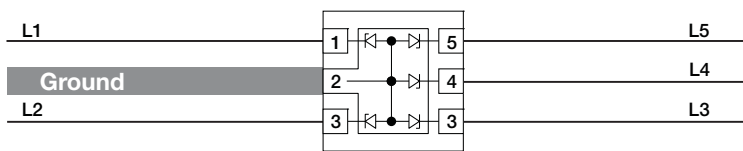
**BiAs-MODE** (5-line bidirectional asymmetrical protection mode)

With the GMF05LC-HSF up to 5 signal- or data-lines (L1 to L5) can be protected against voltage transients. With pin 2 connected to ground and pin 1; pin 3 up to pin 6 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage ( $V_{RWM}$ ) the protection diode between data-line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

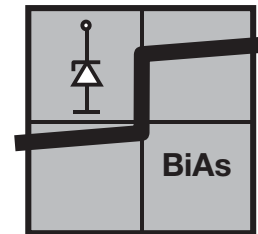
As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage ( $V_C$ ) is defined by the breakthrough voltage ( $V_{BR}$ ) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage ( $V_F$ ) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the GMF05LC-HSF clamping behavior is bidirectional and asymmetrical (BiAs).



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| ELECTRICAL CHARACTERISTICS GMF05LC-HSF |  |               |      |      |      |         |
|--|--|---------------|------|------|------|---------|
| PARAMETER                              | TEST CONDITIONS/REMARKS                        | SYMBOL        | MIN. | TYP. | MAX. | UNIT    |
| Protection paths                       | Number of lines which can be protected         | $N_{channel}$ | -    | -    | 5    | lines   |
| Reverse stand-off voltage              | at $I_R = 1 \mu A$                             | $V_{RWM}$     | -    | -    | 5    | V       |
| Reverse current                        | at $V_R = V_{RWM} = 5 V$                       | $I_R$         | -    | 0.01 | 0.1  | $\mu A$ |
| Reverse breakdown voltage              | at $I_R = 1 mA$                                | $V_{BR}$      | 6    | -    | 8    | V       |
| Reverse clamping voltage               | at $I_{PP} = 1 A$ acc. IEC 61000-4-5           | $V_C$         | -    | 8    | 9.5  | V       |
|  | at $I_{PP} = I_{PPM} = 5 A$ acc. IEC 61000-4-5 |               | -    | 11.5 | 12.5 | V       |
| Forward clamping voltage               | at $I_F = 1 A$ acc. IEC 61000-4-5              | $V_F$         | -    | 1.5  | 2    | V       |
|  | at $I_{PP} = I_{PPM} = 5 A$ acc. IEC 61000-4-5 |               | -    | 3.1  | 4    | V       |
| Capacitance                            | at $V_R = 0 V$ ; $f = 1 MHz$                   | $C_D$         | -    | 43   | 50   | pF      |
|  | at $V_R = 2.5 V$ ; $f = 1 MHz$                 |               | -    | 25   | -    | pF      |

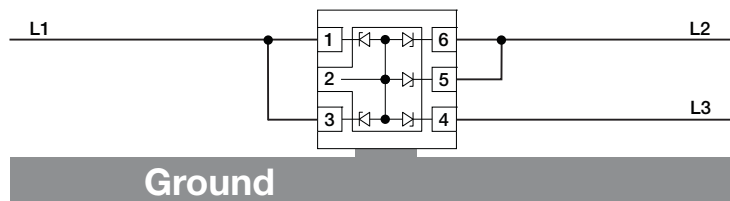
**Note**

- Ratings at 25 °C ambient temperature, unless otherwise specified. BiAs mode: each input (pin 1, 2, 3, to 6) to ground (pin 2).

If a higher surge current or peak pulse current ( $I_{PP}$ ) is needed, some protection diodes in the GMF05LC-HSF can also be used in parallel in order to "multiply" the performance.

If two diodes are switched in parallel you get

- double surge power = double peak pulse current ( $2 \times I_{PPM}$ )
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line capacitance ( $2 \times C_D$ )
- double reverse leakage current ( $2 \times I_R$ )



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**TYPICAL CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

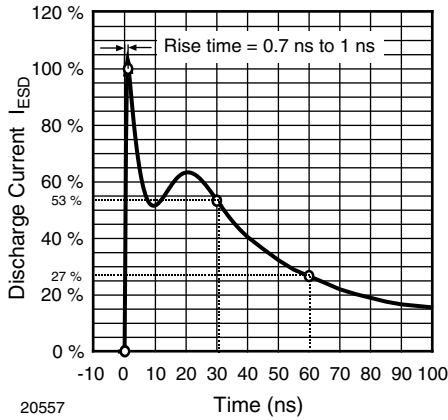


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

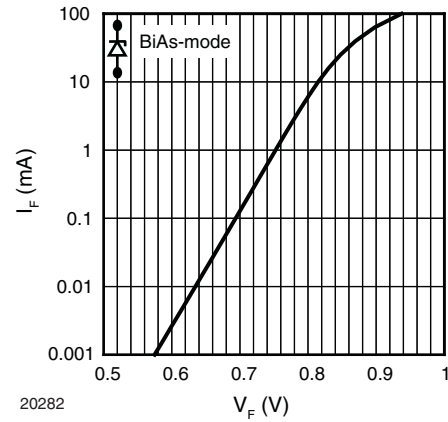


Fig. 4 - Typical Forward Current  $I_F$  vs. Forward Voltage  $V_F$

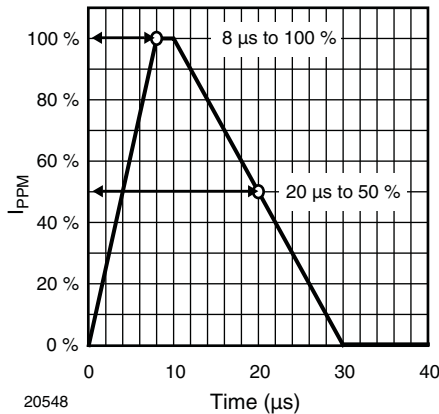


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form acc. IEC 61000-4-5

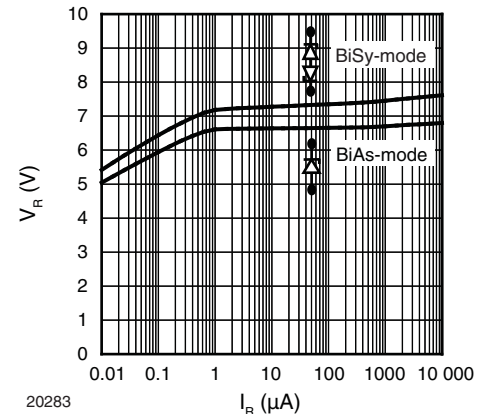


Fig. 5 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

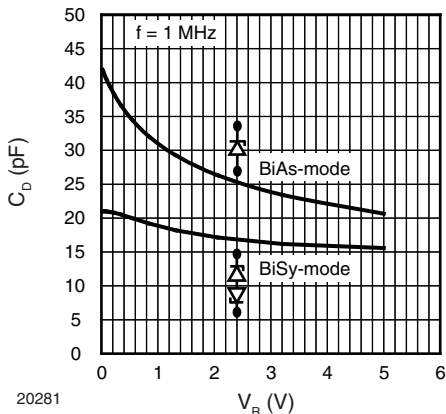


Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$

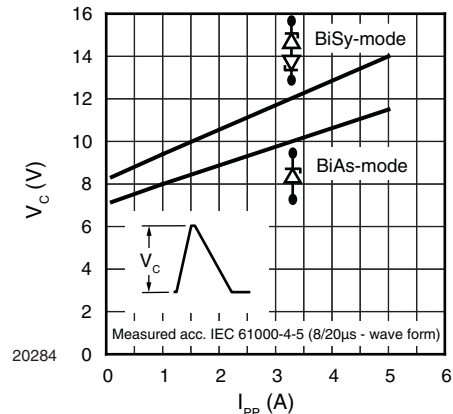


Fig. 6 - Typical Peak Clamping Voltage  $V_C$  vs. Peak Pulse Current  $I_{PP}$

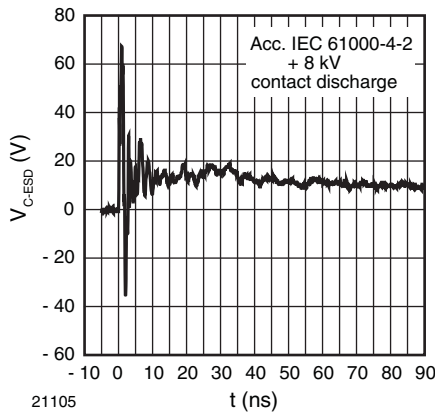


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

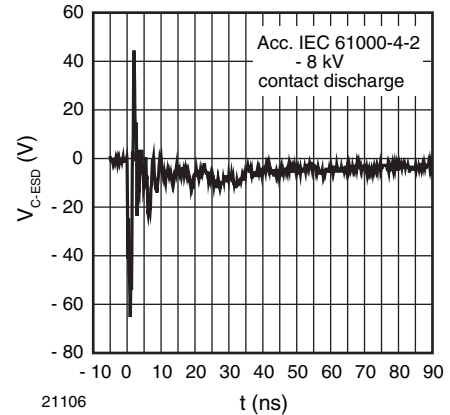


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

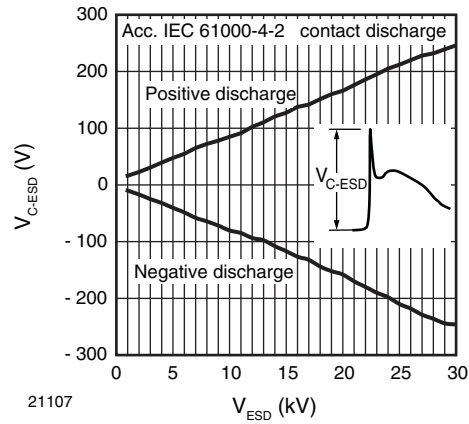
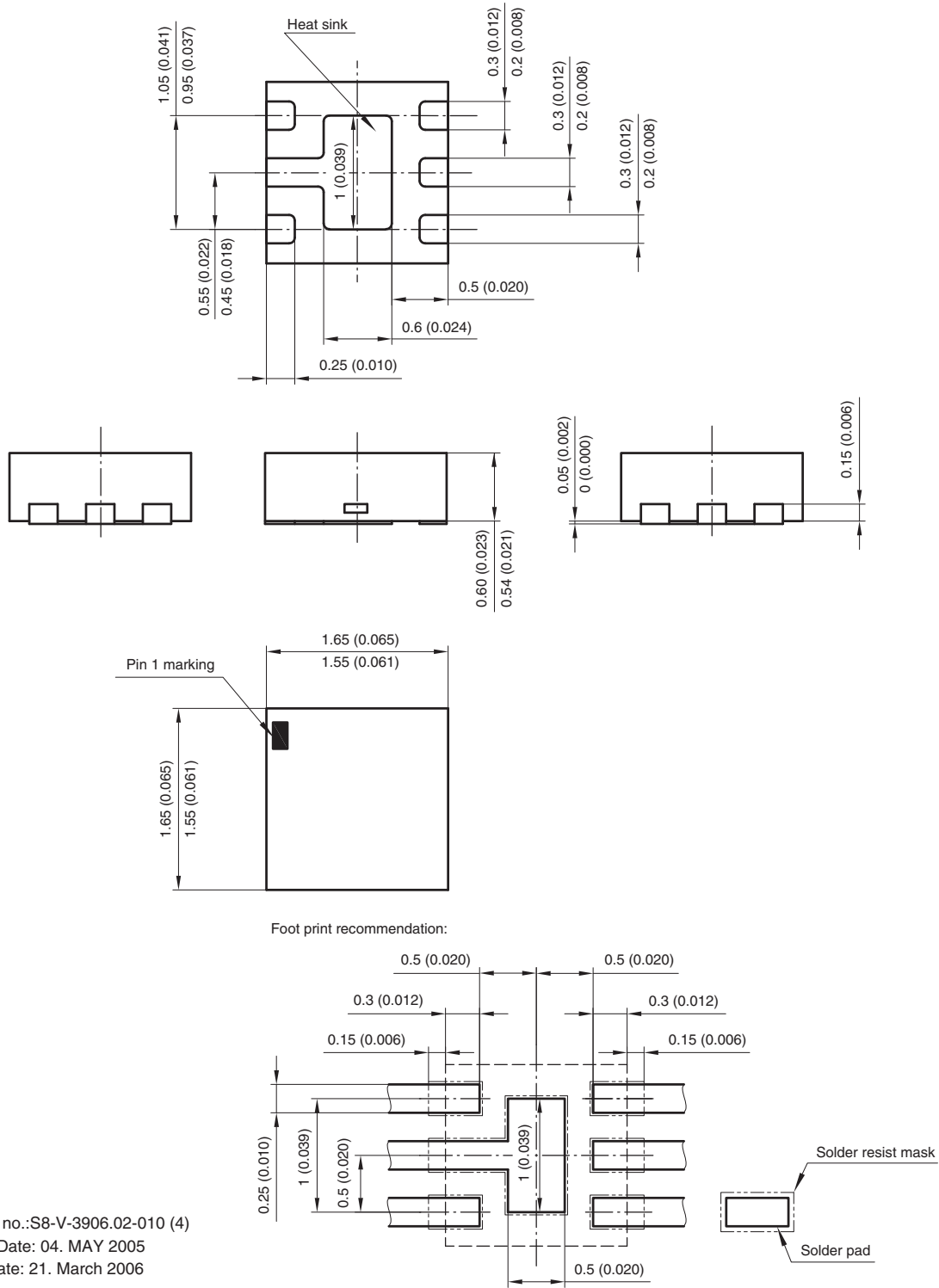


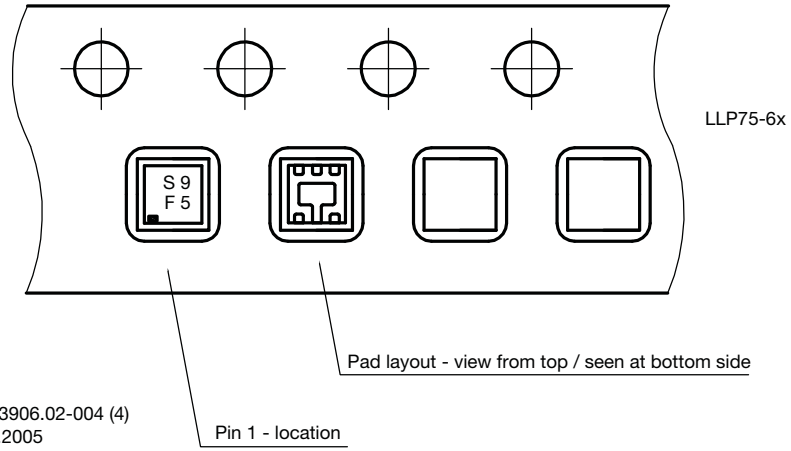
Fig. 9 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)



## PACKAGE DIMENSIONS in millimeters (inches): **LLP75-6L**



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 Created - Date: 04. MAY 2005  
 Rev. 4 - Date: 21. March 2006  
 20454





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