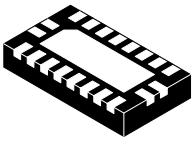
Low-Voltage Dual-Supply 8-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

FXLA108



WQFN20 4.5x2.5, 0.5P
CASE 510CD

MARKING DIAGRAM

$Y	= Logo
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code
FXLA108	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

Description

The FXLA108 is a configurable dual−voltage supply translator for both uni−directional and bi−directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi−directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

The device remains in three−state as long as either V_{CC} = 0 V, allowing either V_{CC} to be powered up first. Internal power−down control circuits place the device in 3−state if either V_{CC} is removed.

The /OE input, when HIGH, disables both the A and B ports by placing them in a 3−state condition. The /OE input is supplied by V_{CCA}.

The FXLA108 supports bi−directional translation without the need for a direction control pin. The two ports of the device have auto−direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Features

- Bi−Directional Interface Between Two Levels: from 1.1 V to 3.6 V
- Fully Configurable: Inputs and Outputs Track V_{CC}
- Non−Preferential Power−Up; Either V_{CC} May Be Powered Up First
- Outputs Switch to 3−State if Either V_{CC} is at GND
- Power−Off Protection
- Bus−Hold on Data Inputs Eliminates the Need for Pull−Up Resistors; Do Not Use Pull−Up Resistors on A or B Ports
- Control Input (/OE) Referenced to V_{CCA} Voltage
- Packaged in 20−Terminal DQFN (2.5 mm x 4.5 mm)
- Direction Control Not Necessary
- 100 Mbps Throughput when Translating Between 1.8 V and 2.5 V
- ESD Protection Exceeds:
  - 8 kV HBM (per JESD22−A114 &Mil Std 883e 3015.7)
  - 2 kV CDM (per ESD STM 5.3)
- This is a Pb−Free Device

Applications

- Laptops, Notebooks
- Routers, Switches

PIN CONFIGURATION

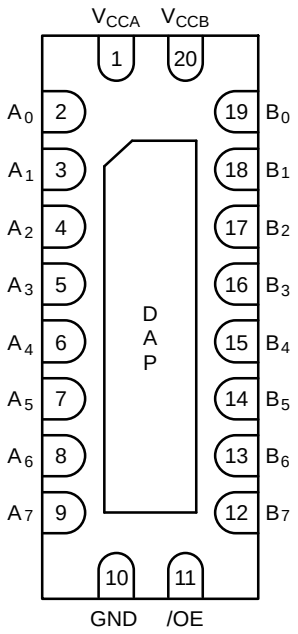


Figure 1. Pin Configuration (Top Through View)

PIN DEFINITIONS

Pin No.	Name	Description
1	V_{CCA}	A−Side Power Supply
2	A_0	A−Side Inputs or 3−State Outputs
3	A_1	A−Side Inputs or 3−State Outputs
4	A_2	A−Side Inputs or 3−State Outputs
5	A_3	A−Side Inputs or 3−State Outputs
6	A_4	A−Side Inputs or 3−State Outputs
7	A_5	A−Side Inputs or 3−State Outputs
8	A_6	A−Side Inputs or 3−State Outputs
9	A_7	A−Side Inputs or 3−State Outputs
10	GND	Ground
11	/OE	Output Enable Input
12	B_7	B−Side Inputs or 3−State Outputs
13	B_6	B−Side Inputs or 3−State Outputs
14	B_5	B−Side Inputs or 3−State Outputs
15	B_4	B−Side Inputs or 3−State Outputs
16	B_3	B−Side Inputs or 3−State Outputs
17	B_2	B−Side Inputs or 3−State Outputs
18	B_1	B−Side Inputs or 3−State Outputs
19	B_0	B−Side Inputs or 3−State Outputs
20	V_{CCB}	B−Side Power Supply
DAP	NC	No Connect

FUNCTIONAL DIAGRAM

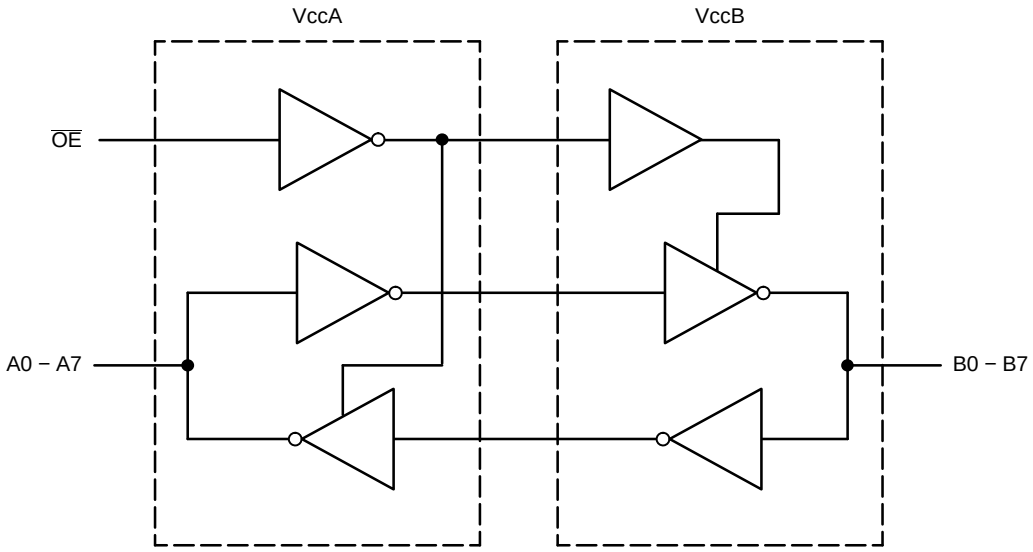


Figure 2. Functional Diagram

FUNCTION TABLE

Control	
/OE	**Outputs**
LOW Logic Level	Normal Operation
HIGH Logic Level	3−State

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	V_{CCA}	−0.5	4.6	V
		V_{CCB}	−0.5	4.6	
V_I	DC Input Voltage	I/O Ports A and B	−0.5	4.6	V
		Control Input (/OE)	−0.5	4.6	
V_O	Output Voltage (Note 2)	Output 3−State	−0.5	4.6	V
		Output Active (A_n)	−0.5	V_{CCA} + 0.5	
		Output Active (B_n)	−0.5	V_{CCB} + 0.5	
I_{IK}	DC Input Diode Current	V_I < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_O < 0 V	−	−50	mA
		V_O > V_{CC}	−	+50	
I_{OH}/I_{OL}	DC Output Source/Sink Current		−50	+50	mA
I_{CC}	DC V_{CC} or Ground Current (Per Supply Pin)		−	±100	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
P_D	Power Dissipation		−	35	mW
ESD	Human Body Model, JESD22−A114		−	8	kV
	Charged Device Model, JESD22−C101		−	2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum ratings must be observed.
2. All unused inputs and input/outputs must be held at V_{CCi} or GND.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Power Supply	Operating V_{CCA} or V_{CCB}	1.1	3.6	V
V_{IN}	Input Voltage	Ports A and B	0	3.6	V
		Control Input (/OE)	0	V_{CCA}	V
T_A	Operating Temperature, Free Air		−40	+85	°C
dt/dV	Minimum Input Edge Rate	$V_{CCA/B}$ = 1.1 to 3.6 V	−	10	ns/V
Θ_{JA}	Thermal Resistance: Junction−to−Ambient		−	50	°C/W
Θ_{JC}	Thermal Resistance: Junction−to−Case		−	23	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

POWER−UP/POWER−DOWN SEQUENCE

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 V, outputs are in a high−impedance state. The control input (/OE) is designed to track the V_{CCA} supply. A pull−up resistor tying /OE to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power−up or power−down. The size of the pull−up resistor is based upon the current−sinking capability of the device driving the /OE pin.

The recommended power−up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the /OE input LOW to enable the device.

The recommended power−down sequence is:

1. Drive /OE input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other $V_{CC.}$

Pull−Up/Pull−Down Resistors

Do not use pull−up or pull−down resistors. This device has bus−hold circuits: pull−up or pull−down resistors are not recommended because they interfere with the output state. The current through these resistors may exceed the hold drive, $I_{I(HOLD)}$ and/or $I_{I(OD)}$ bus−hold currents. The bus−hold feature eliminates the need for extra resistors.

DC CHARACTERISTICS (T_A = −40 to 85°C)

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min	Typ	Max	Unit
V_{IHA}	High−Level Input Voltage	Data Inputs A_n Control Pin /OE	2.70 to 3.60	1.10 to 3.60	2.00	−	−	V
			2.30 to 2.70		1.60	−	−	
			1.65 to 2.30		0.65 x V_{CCA}	−	−	
			1.40 to 1.65		0.65 x V_{CCA}	−	−	
			1.10 to 1.40		0.9 x V_{CCA}	−	−	
V_{IHB}		Data Inputs B_n	1.10 to 3.60	2.70 to 3.60	2.00	−	−	V
				2.30 to 2.70	1.60	−	−	
				1.65 to 2.30	0.65 x V_{CCB}	−	−	
				1.40 to 1.65	0.65 x V_{CCB}	−	−	
				1.10 to 1.40	0.9 x V_{CCB}	−	−	
V_{ILA}	Low−Level Input Voltage	Data Inputs A_n Control Pin /OE	2.70 to 3.60	1.10 to 3.60	−	−	0.8	V
			2.30 to 2.70		−	−	0.7	
			1.65 to 2.30		−	−	0.35 x V_{CCA}	
			1.40 to 1.65		−	−	0.35 x V_{CCA}	
			1.10 to 1.40		−	−	0.1 x V_{CCA}	
V_{ILB}		Data Inputs B_n	1.10 to 3.60	2.70 to 3.60	−	−	0.8	V
				2.30 to 2.70	−	−	0.7	
				1.65 to 2.30	−	−	0.35 x V_{CCB}	
				1.40 to 1.65	−	−	0.35 x V_{CCB}	
				1.10 to 1.40	−	−	0.1 x V_{CCB}	
V_{OHA}	High−Level Output Voltage (Note 3)	I_{OH} = −4 μA	1.10 to 3.60	1.10 to 3.60	V_{CCA} − 0.4	−	−	V
V_{OHB}		I_{OH} = −4 μA	1.10 to 3.60	1.10 to 3.60	V_{CCB} − 0.4	−	−	
V_{OLA}	Low−Level Output Voltage (Note 3)	I_{OL} = 4 μA	1.10 to 3.60	1.10 to 3.60	−	−	0.4	V
V_{OLB}		I_{OL} = 4 μA	1.10 to 3.60	1.10 to 3.60	−	−	0.4	
$I_{I(HOLD)}$	Bus−Hold Input Minimum Drive Current	V_{IN} = 0.80 V	3.00	3.00	75.0	−	−	μA
		V_{IN} = 2.00 V	3.00	3.00	−75.0	−	−	
		V_{IN} = 0.7 V	2.30	2.30	45.0	−	−	
		V_{IN} = 1.60 V	2.30	2.30	−45.0	−	−	
		V_{IN} = 0.57 V	1.65	1.65	25.0	−	−	
		V_{IN} = 1.07 V	1.65	1.65	−25.0	−	−	
		V_{IN} = 0.49 V	1.40	1.40	11.0	−	−	
		V_{IN} = 0.91 V	1.40	1.40	−11.0	−	−	
		V_{IN} = 0.11 V	1.10	1.10	−	4.0	−	
		V_{IN} = 0.99 V	1.10	1.10	−	−4.0	−	
$I_{I(ODH)}$	Bus−Hold Input Overdrive High Current (Note 4)	Data Inputs A_n, B_n	3.60	3.60	450.00	−	−	μA
			2.70	2.70	300.00	−	−	
			1.95	1.95	200.00	−	−	
			1.60	1.60	120.00	−	−	
			1.40	1.40	80.00	−	−	

DC CHARACTERISTICS (T_A = −40 to 85°C) (continued)

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min	Typ	Max	Unit
$I_{I(ODL)}$	Bus−Hold Input Overdrive Low Current (Note 5)	Data Inputs A_n, B_n	3.60	3.60	−450.00	−	−	μA
			2.70	2.70	−300.00	−	−	
			1.95	1.95	−200.00	−	−	
			1.60	1.60	−120.00	−	−	
			1.40	1.40	−80.00	−	−	
I_I	Input Leakage Current	Control Inputs /OE, $V_I = V_{CCA}$ or GND	1.10 to 3.60	3.60	−	−	±1.0	μA
I_{OFF}	Power−Off Leakage Current	A_n V_O = 0 V to 3.6 V	0	3.6	−	−	±2.0	μA
		B_n V_O = 0 V to 3.6 V	3.60	0	−	−	±2.0	
I_{OZ}	3−State Output Leakage	A_n, B_n V_O = 0 V or 3.6 V, /OE = V_{IH}	3.6	3.60	−	−	±5.0	μA
		A_n V_O = 0 V or 3.6 V, /OE = GND	3.60	0	−	−	±5.0	
		B_n V_O = 0 V or 3.6 V, /OE = GND	0	3.60	−	−	±5.0	
$I_{CCA/B}$	Quiescent Supply Current (Note 6, 7)	$V_I = V_{CCI}$ or GND; I_O = 0, /OE = GND	1.10 to 3.60	1.10 to 3.60	−	−	10.0	μA
I_{CCZ}		$V_I = V_{CCI}$ or GND; I_O = 0, /OE = V_{IH}	1.10 to 3.60	1.10 to 3.60	−	−	10.0	μA
I_{CCA}	Quiescent Supply Current	$V_I = V_{CCB}$ or GND; I_O = 0 B−to−A Direction, /OE = GND	0	1.10 to 3.60	−	−	−10.0	μA
		$V_I = V_{CCA}$ or GND; I_O = 0 A−to−B Direction	1.10 to 3.60	0	−	−	10.0	
I_{CCB}		$V_I = V_{CCA}$ or GND; I_O = 0, A−to−B Direction, /OE = GND	1.10 to 3.60	0	−	−	−10.0	μA
		$V_I = V_{CCB}$ or GND; I_O = 0 B−to−A Direction	0	1.10 to 3.60	−	−	10.0	

3. This is the output voltage for static conditions. Dynamic drive specifications are given in the Dynamic Output Electrical Characteristics table.
4. An external drive must source at least the specified current to switch LOW−to−HIGH.
5. An external drive must source at least the specified current to switch HIGH−to−LOW.
6. V_{CCI} is the V_{CC} associated with the input side.
7. Reflects current per supply, V_{CCA} or V_{CCB}.

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CCA} = 3.0 V to 3.6 V		V_{CCA} = 2.3 V to 2.7 V		V_{CCA} = 1.65 V to 1.95 V		V_{CCA} = 1.4 V to 1.6 V		V_{CCA} = 1.1 V to 1.3 V	Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	
A PORT (A_n) **OUTPUT LOAD: C_L = 15 pF, $R_L \geq$ 1 MΩ ($C_{I/O}$ = 4 pF), T_A = −40 to 85°C**											
t_{rise}	Output Rise Time A Port (Note 9)	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
t_{fall}	Output Fall Time A Port (Note 10)	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
I_{OHD}	Dynamic Output Current High (Note 9)	−11.4	−	−7.5	−	−4.7	−	−3.2	−	−1.7	mA
I_{OLD}	Dynamic Output Current Low (Note 10)	+11.4	−	+7.5	−	+4.7	−	+3.2	−	+1.7	mA
B PORT (B_n) **OUTPUT LOAD: C_L = 15 pF, $R_L \geq$ 1 MΩ ($C_{I/O}$ = 5 pF), T_A = −40 to 85°C**											
t_{rise}	Output Rise Time B Port (Note 9)	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
t_{fall}	Output Fall Time B Port (Note 10)	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
I_{OHD}	Dynamic Output Current High (Note 9)	−12.0	−	−7.9	−	−5.0	−	−3.4	−	−1.8	mA
I_{OLD}	Dynamic Output Current Low (Note 10)	+12.0	−	+7.9	−	+5.0	−	+3.4	−	+1.8	mA

8. Dynamic output characteristics are guaranteed, but not tested.
9. *See Figure 7.*
10. *See Figure 8.*

AC CHARACTERISTICS

Symbol	Parameter	V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V	Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	
V_{CCA} = 3.0 V to 3.6 V, T_A = −40 to 85°C											
t_{PLH}, t_{PHL}	A to B	0.2	4.0	0.3	4.2	0.5	5.4	0.6	6.8	6.9	ns
	B to A	0.2	4.0	0.2	4.1	0.3	5.0	0.5	6.0	4.5	ns
t_{PZL}, t_{PZH}	/OE to A, /OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{SKEW}	A Port, B Port (Note 11)	−	0.5	−	0.5	−	0.5	−	1.0	1.0	ns
V_{CCA} = 2.3 V to 2.7 V, T_A = −40 to 85°C											
t_{PLH}, t_{PHL}	A to B	0.2	4.1	0.4	4.5	0.5	5.6	0.8	6.9	7.0	ns
	B to A	0.3	4.2	0.4	4.5	0.5	5.5	0.5	6.5	4.8	ns
t_{PZL}, t_{PZH}	/OE to A, /OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{SKEW}	A Port, B Port (Note 11)	−	0.5	−	0.5	−	0.5	−	1.0	1.0	ns
V_{CCA} = 1.65 V to 1.95 V, T_A = −40 to 85°C											
t_{PLH}, t_{PHL}	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	7.5	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	5.4	ns
t_{PZL}, t_{PZH}	/OE to A, /OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{SKEW}	A Port, B Port (Note 11)	−	0.5	−	0.5	−	0.5	−	1.0	1.0	ns
V_{CCA} = 1.4 V to 1.6 V, T_A = −40 to 85°C											
t_{PLH}, t_{PHL}	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	7.9	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	6.1	ns
t_{PZL}, t_{PZH}	/OE to A, /OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{SKEW}	A Port, B Port (Note 12)	−	1.0	−	1.0	−	1.0	−	1.0	1.0	ns
V_{CCA} = 1.1 V to 1.3 V, T_A = −40 to 85°C											
		Typ		Typ		Typ		Typ		Typ	
t_{PLH}, t_{PHL}	A to B	4.6		4.8		5.4		6.2		9.2	ns
	B to A	6.8		7.0		7.4		7.8		9.1	ns
t_{PZL}, t_{PZH}	/OE to A, /OE to B	1.7		1.7		1.7		1.7		1.7	μs
t_{SKEW}	A Port, B Port (Note 12)	1.0		1.0		1.0		1.0		1.0	ns

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW) *(see Figure 10).*
Skew is guaranteed, but not tested.
12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW) *(see Figure 10).*
Skew is guaranteed, but not tested.

MAXIMUM DATA RATE (T_A = −40 to 85°C)

V_{CCA}	V_{CCB} = 3.0 V to 3.6 V	V_{CCB} = 2.3 V to 2.7 V	V_{CCB} = 1.65 V to 1.95 V	V_{CCB} = 1.4 V to 1.6 V	V_{CCB} = 1.1 V to 1.3 V	Unit
	Min	Min	Min	Min	Typ	
V_{CCA} = 3.00 V to 3.60 V	140	120	100	80	40	Mbps
V_{CCA} = 2.30 V to 2.70 V	120	120	100	80	40	Mbps
V_{CCA} = 1.65 V to 1.95 V	100	100	80	60	40	Mbps
V_{CCA} = 1.40 V to 1.60 V	80	80	60	60	40	Mbps
	Typ	Typ	Typ	Typ	Typ	
V_{CCA} = 1.10 V to 1.30 V	40	40	40	40	40	Mbps

13. Maximum data rate is guaranteed, but not tested.
14. Maximum data rate is specified in megabits per second *(see Figure 9)*. It is equivalent to two times the F−toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

CAPACITANCE

Symbol	Parameter		Conditions	T_A = +25°C Typical	Unit
C_{IN}	Input Capacitance Control Pin (/OE)		V_{CCA} = V_{CCB} = GND	3	pF
$C_{I/O}$	Input/Output Capacitance	A_n	V_{CCA} = V_{CCB} = 3.3 V, /OE = V_{CCA}	4	pF
		B_n		5	
C_{pd}	Power Dissipation Capacitance		V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25	pF

I/O ARCHITECTURE BENEFIT

The FXLA108 I/O architecture benefits the end user, beyond level translation, in the following three ways:

Auto Direction without an external direction pin.

Drive Capacitive Loads. Automatically shifts to a higher current drive mode only during “Dynamic Mode” or HL / LH transitions.

Lower Power Consumption. Automatically shifts to low−power mode during “Static Mode” (no transitions), lowering power consumption.

The FXLA108 does not require a direction pin. Instead, the I/O architecture detects input transitions on both side and automatically transfers the data to the corresponding output. For example, for a given channel, if both A and B side are at a static LOW, the direction has been established as A $\rightarrow$ B, and a LH transition occurs on the B port; the FXLA108 internal I/O architecture automatically changes direction from A $\rightarrow$ B to B $\rightarrow$ A.

During HL / LH transitions, or “Dynamic Mode,” a strong output driver drives the output channel in parallel with a weak output driver. After a typical delay of approximately 10 ns – 50 ns, the strong driver is turned off, leaving the weak driver enabled for holding the logic state of the channel. This weak driver is called the “bus hold.” “Static Mode” is when only the bus hold drives the channel. The bus hold can be over ridden in the event of a direction change. The strong driver allows the FXLA108 to quickly charge and discharge capacitive transmission lines during dynamic mode. Static mode conserves power, where I_{CC} is typically < 5 μA.

Bus Hold Minimum Drive Current

Specifies the minimum amount of current the bus hold driver can source/sink. The bus hold minimum drive current (II_{HOLD}) is V_{CC} dependent and guaranteed in the DC Electrical tables. The intent is to maintain a valid output state in a static mode, but that can be overridden when an input data transition occurs.

Bus Hold Input Overdrive Drive Current

Specifies the minimum amount of current required (by an external device) to overdrive the bus hold in the event of a direction change. The bus hold overdrive (II_{ODH}, II_{ODL}) is V_{CC} dependent and guaranteed in the DC Electrical tables.

Dynamic Output Current

The strength of the output driver during LH / HL transitions is *referenced on page 8, Dynamic Output Electrical Characteristics, I_{OHD}, and I_{OLD}*.

TEST DIAGRAMS

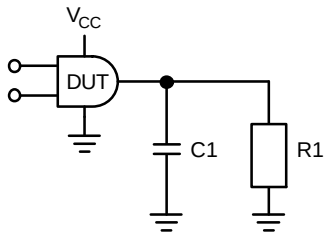


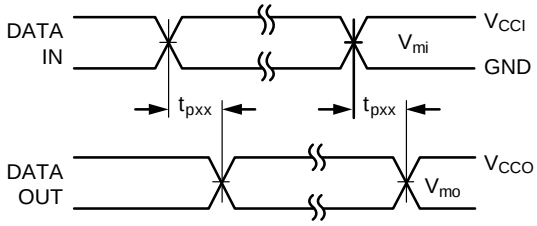
Figure 3. Test Circuit

Table 1. AC TEST CONDITIONS

Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	0 V
t_{PZL}	0 V	HIGH to LOW Switch
t_{PZH}	V_{CCI}	HIGH to LOW Switch

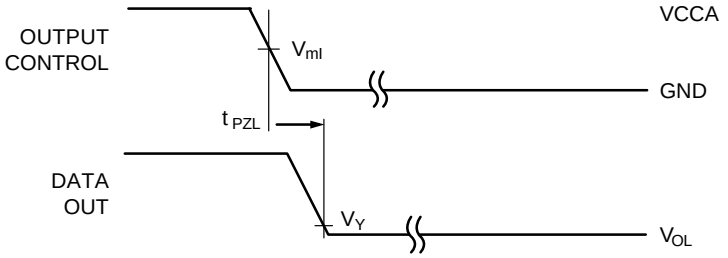
Table 2. AC LOAD

V_{CCo}	C1	R1
1.2 V ±0.1 V	15 pF	1 MΩ
1.5 V ±0.1 V	15 pF	1 MΩ
1.8 V ±0.15 V	15 pF	1 MΩ
2.5 V ±0.2 V	15 pF	1 MΩ
3.3 V ±0.3 V	15 pF	1 MΩ



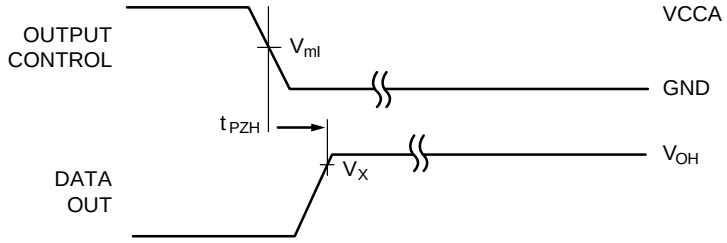
NOTES:
15. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
16. Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_I = 3.0 V to 3.6 V only.

Figure 4. Waveform for Inverting and Non−Inverting Functions



NOTES:
17. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
18. Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_I = 3.0 V to 3.6 V only.

Figure 5. 3−State Output Low Enable Time for Low Voltage Logic



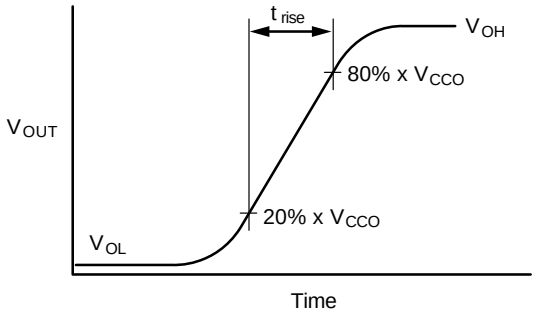
NOTES:
19. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
20. Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_I = 3.0 V to 3.6 V only.

Figure 6. 3−State Output High Enable Time for Low Voltage Logic

Table 3. TEST MEASURE POINTS

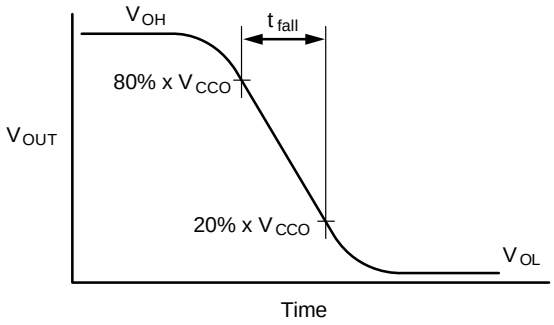
Symbol	V_{DD}
V_{MI} (Note 21)	V_{CCI} / 2
V_{MO}	V_{CCO} / 2
V_X	0.9 x V_{CCO}
V_Y	0.1 x V_{CCO}

21. $V_{CCI} = V_{CCA}$ for control pin /OE or $V_{MI} = (V_{CCA} / 2)$.



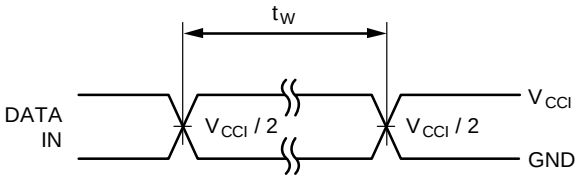
$$I_{OHD} \approx \left(C_L + C_{I/O}\right) \times \frac{\Delta V_{OUT}}{\Delta t} = \left(C_L + C_{I/O}\right) \times \frac{(20\% - 80\%) \cdot V_{CCO}}{t_{RISE}}$$

Figure 7. Active Output Rise Time and Dynamic Output Current High



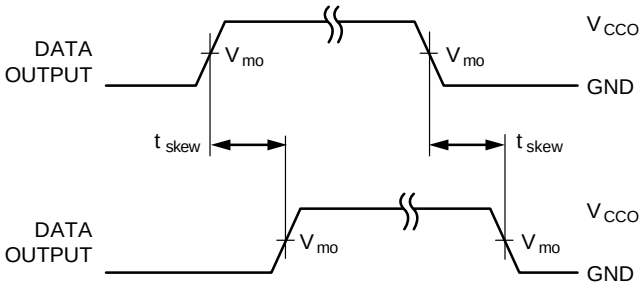
$$I_{OLD} \approx \left(C_L + C_{I/O}\right) \times \frac{\Delta V_{OUT}}{\Delta t} = \left(C_L + C_{I/O}\right) \times \frac{(80\% - 20\%) \cdot V_{CCO}}{t_{FALL}}$$

Figure 8. Active Output Fall Time and Dynamic Output Current Low



Maximum Data Rate, f = 1 / t_W

Figure 9. Maximum Data Rate



NOTE:
22. $t_{SKEW} = (t_{pHLmax} - t_{pHLmin})$ or $(t_{pLHmax} - t_{pLHmin})$

Figure 10. Output Skew Time

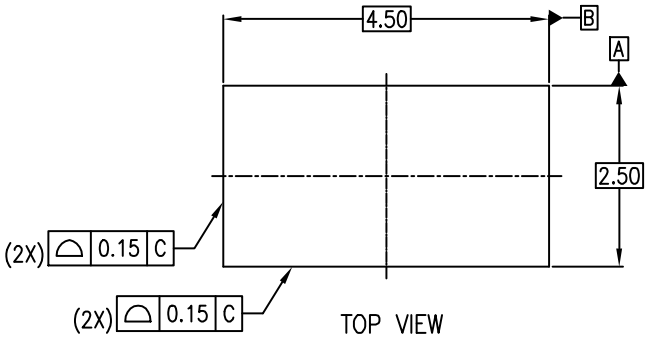
ORDERING INFORMATION

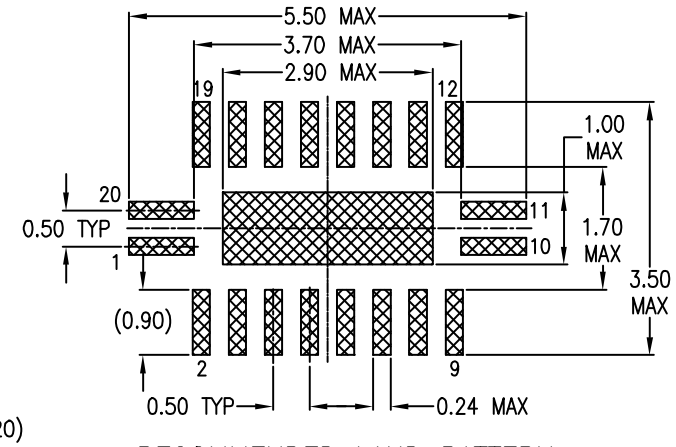
Part Number	Operating Temperature Range	Package	Shipping†
FXLA108BQX	−40 to 85°C	WQFN20 4.5x2.5, 0.5P 20−Terminal DQFN 2.5mm x 4.5mm Package (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

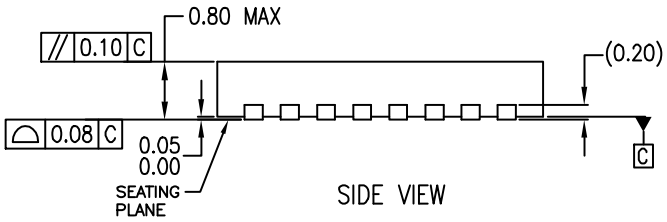
WQFN20 4.5x2.5, 0.5P
CASE 510CD
ISSUE O

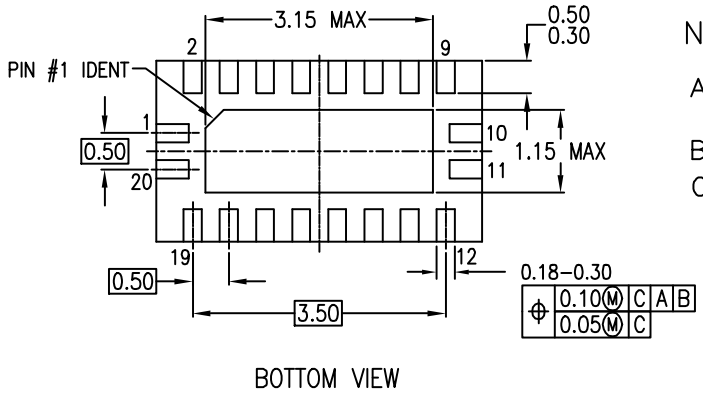
DATE 31 AUG 2016





RECOMMENDED LAND PATTERN





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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