

# Motion SPM<sup>®</sup> 5 Series

## FSB50550BB

### General Description

The FSB50550BB is an advanced Motion SPM 5 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in MOSFETs (FRFET<sup>®</sup> technology) to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts and thermal monitoring. The built-in high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.

### Features

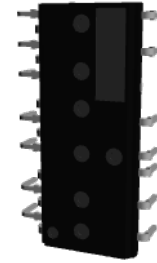
- Gate Driver Resistance  $R_{ON} = 4.5 \text{ k}\Omega$ ,  $R_{OFF} = 1.2 \text{ k}\Omega$
- Optimized for over 10 kHz Switching Frequency
- 500 V FRFET MOSFET 3-Phase Inverter with Gate Drivers and Protection
- Built-In Bootstrap Diodes Simplify PCB Layout
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3/5 V Logic, Schmitt-Trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- HVIC for Gate Driving and Under-Voltage Protection
- Isolation Rating: 1500  $V_{rms}/min$ .
- This Device is Pb-Free and is RoHS Compliant

### Applications

- 3-Phase Inverter Driver for Small Power AC Motor Drives

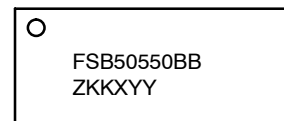
### Related Source

- RD-FSB50450AS – Reference Design for Motion SPM 5 Series Ver.2
- [AN-9082 – Motion SPM5 Series Thermal Performance by Contact Pressure](#)



SPM5T-021/21LD  
CASE M0DET

### MARKING DIAGRAM



FSB50550BB = Specific Device Code  
Z = Assembly Code  
KK = Lot Run Traceability Code  
XXYY = Date Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FSB50550BB

## ORDERING INFORMATION

Device	Device Marking	Package	Packing Type	Quantity
FSB50550BB	FSB50550BB	SPM5T-021 (Pb-Free)	Rail	15

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Rating	Unit
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### INVERTER PART (Each MOSFET Unless Otherwise Specified)

$V_{DSS}$	Drain-Source Voltage of Each MOSFET		500	V
* $I_{D25}$	Each MOSFET Drain Current, Continuous	$T_C = 25^\circ\text{C}$	3.0	A
* $I_{D80}$	Each MOSFET Drain Current, Continuous	$T_C = 80^\circ\text{C}$	1.9	A
* $I_{DP}$	Each MOSFET Drain Current, Peak	$T_C = 25^\circ\text{C}$ , $PW < 100 \mu\text{s}$	7.0	A
* $I_{DRMS}$	Each MOSFET Drain Current, Rms	$T_C = 80^\circ\text{C}$ , $F_{PWM} < 20 \text{ kHz}$	1.3	$A_{rms}$

### CONTROL PART (Each HVIC Unless Otherwise Specified)

$V_{DD}$	Control Supply Voltage	Applied Between $V_{DD}$ and COM	20	V
$V_{BS}$	High-side Bias Voltage	Applied Between $V_B$ and $V_S$	20	V
$V_{IN}$	Input Signal Voltage	Applied Between IN and COM	$-0.3 \sim V_{DD} + 0.3$	V

### BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified.)

$V_{RRMB}$	Maximum Repetitive Reverse Voltage		500	V
* $I_{FB}$	Forward Current	$T_C = 25^\circ\text{C}$	0.5	A
* $I_{FPB}$	Forward Current (Peak)	$T_C = 25^\circ\text{C}$ , Under 1 ms Pulse Width	2.0	A

### THERMAL RESISTANCE

$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 1)	Each FET under inverter operating condition (Note 1)	8.9	$^\circ\text{C}/\text{W}$
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### TOTAL SYSTEM

$T_J$	Operating Junction Temperature		-40~150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature		-40~125	$^\circ\text{C}$
$V_{ISO}$	Isolation Voltage	60 Hz, Sinusoidal, 1 minute, Connect Pins to Heat Sink Plate	1500	$V_{rms}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

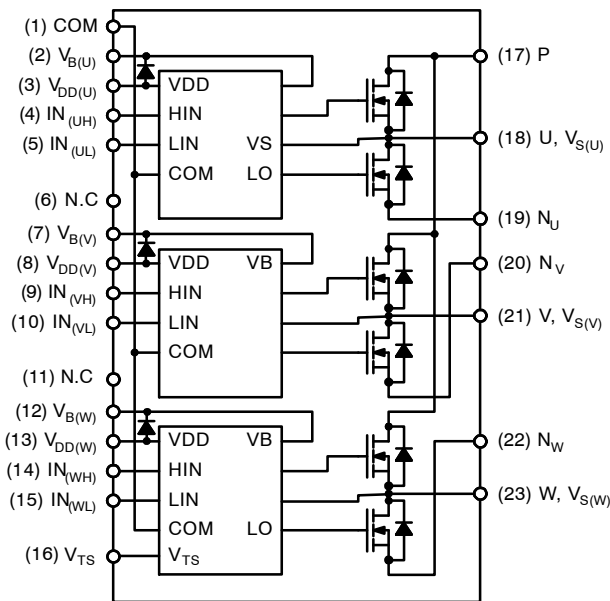
#### NOTES:

- For the measurement point of case temperature  $T_C$ , Please refer to Figure 4.
- Marking "\*" is calculation value or design factor.

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## PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	V <sub>B(U)</sub>	Bias Voltage for U-Phase High-Side MOSFET Driving
3	V <sub>DD(U)</sub>	Bias Voltage for U-Phase IC and Low-Side MOSFET Driving
4	IN <sub>(UH)</sub>	Signal Input for U-Phase High-Side
5	IN <sub>(UL)</sub>	Signal Input for U-Phase Low-Side
6	N.C	No Connection
7	V <sub>B(V)</sub>	Bias Voltage for V-Phase High Side MOSFET Driving
8	V <sub>DD(V)</sub>	Bias Voltage for V-Phase IC and Low Side MOSFET Driving
9	IN <sub>(VH)</sub>	Signal Input for V-Phase High-Side
10	IN <sub>(VL)</sub>	Signal Input for V-Phase Low-Side
11	N.C	No Connection
12	V <sub>B(W)</sub>	Bias Voltage for W-Phase High-Side MOSFET Driving
13	V <sub>DD(W)</sub>	Bias Voltage for W-Phase IC and Low-Side MOSFET Driving
14	IN <sub>(WH)</sub>	Signal Input for W-Phase High-Side
15	IN <sub>(WL)</sub>	Signal Input for W-Phase Low-Side
16	V <sub>TS</sub>	Output for HVIC Temperature Sensing
17	P	Positive DC-Link Input
18	U, V <sub>S(U)</sub>	Output for U-Phase & Bias Voltage Ground for High-Side MOSFET Driving
19	N <sub>U</sub>	Negative DC-Link Input for U-Phase
20	N <sub>V</sub>	Negative DC-Link Input for V-Phase
21	V, V <sub>S(V)</sub>	Output for V-Phase & Bias Voltage Ground for High-Side MOSFET Driving
22	N <sub>W</sub>	Negative DC-Link Input for W-Phase
23	W, V <sub>S(W)</sub>	Output for W Phase & Bias Voltage Ground for High-Side MOSFET Driving



**Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)**

**NOTE:**

- Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside Motion SPM 5 product. External connections should be made as indicated in Figure 3.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C, V<sub>DD</sub> = V<sub>BS</sub> = 15 V Unless Otherwise Specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### INVERTER PART (Each MOSFET Unless Otherwise Specified)

BV <sub>DSS</sub>	Drain – Source Breakdown Voltage	V <sub>IN</sub> = 0 V, I <sub>D</sub> = 1 mA (Note 4)	500	–	–	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>IN</sub> = 0 V, V <sub>DS</sub> = 500 V	–	–	1	mA
R <sub>DS(on)</sub>	Static Drain – Source Turn-On Resistance	V <sub>DD</sub> = V <sub>BS</sub> = 15 V, V <sub>IN</sub> = 5 V, I <sub>D</sub> = 1.2 A	–	2.3	3.0	Ω
V <sub>SD</sub>	Drain – Source Diode Forward Voltage	V <sub>DD</sub> = V <sub>BS</sub> = 15 V, V <sub>IN</sub> = 0 V, I <sub>D</sub> = –1.2 A	–	–	1.3	V
t <sub>ON</sub>	Switching Times	V <sub>PN</sub> = 300 V, V <sub>DD</sub> = V <sub>BS</sub> = 15 V, I <sub>D</sub> = 1.2 A V <sub>IN</sub> = 0 V ↔ 5 V, Inductive Load L = 3 mH High- and Low-Side MOSFET Switching (Note 5)	460	780	1100	ns
t <sub>OFF</sub>			1001	1660	2300	ns
t <sub>rr</sub>			–	230	–	ns
E <sub>ON</sub>			–	69	–	μJ
E <sub>OFF</sub>			–	17	–	μJ
RBSOA	Reverse Bias Safe Operating Area	V <sub>PN</sub> = 400 V, V <sub>DD</sub> = V <sub>BS</sub> = 15 V, I <sub>D</sub> = I <sub>DP</sub> , V <sub>DS</sub> = BV <sub>DSS</sub> , T <sub>J</sub> = 150°C High- and Low-Side MOSFET Switching (Note 6)	Full Square			

### CONTROL PART (Each HVIC Unless Otherwise Specified)

I <sub>QDD</sub>	Quiescent V <sub>DD</sub> Current	V <sub>DD</sub> = 15 V, V <sub>IN</sub> = 0 V	Applied between V <sub>DD</sub> and COM	–	–	200	μA
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Current	V <sub>BS</sub> = 15 V, V <sub>IN</sub> = 0 V	Applied between V <sub>B(U)</sub> – U, V <sub>B(V)</sub> – V, V <sub>B(W)</sub> – W	–	–	100	μA
I <sub>PDD</sub>	Operating V <sub>DD</sub> Supply Current	V <sub>DD</sub> – COM	V <sub>DD</sub> = 15 V, f <sub>PWM</sub> = 20 kHz, duty = 50%, Applied to One PWM Signal Input for Low-Side	–	–	900	μA
I <sub>PBS</sub>	Operating V <sub>BS</sub> Supply Current	V <sub>B(U)</sub> – V <sub>S(U)</sub> , V <sub>B(V)</sub> – V <sub>S(V)</sub> , V <sub>B(W)</sub> – V <sub>S(W)</sub>	V <sub>DD</sub> = V <sub>BS</sub> = 15 V, f <sub>PWM</sub> = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High-Side	–	–	800	μA
UV <sub>DDD</sub>	Low-Side Under-Voltage Protection (Figure 8)	V <sub>DD</sub> Under-Voltage Protection Detection Level		7.4	8.0	9.4	V
UV <sub>DDR</sub>		V <sub>DD</sub> Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
UV <sub>BSD</sub>	High-Side Under-Voltage Protection (Figure 9)	V <sub>BS</sub> Under-Voltage Protection Detection Level		7.4	8.0	9.4	V
UV <sub>BSR</sub>		V <sub>BS</sub> Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
V <sub>TS</sub>	HVIC Temperature Sensing Voltage Output	V <sub>DD</sub> = 15 V, T <sub>HVIC</sub> = 25°C (Note 7)		600	790	980	mV
V <sub>IH</sub>	ON Threshold Voltage	Logic HIGH Level	Applied between V <sub>IN</sub> and COM	–	–	2.9	V
V <sub>IL</sub>	OFF Threshold Voltage	Logic LOW Level		0.8	–	–	V
R <sub>ON</sub>	Gate Driver ON Output Resistance			3.6	4.5	5.4	kΩ
R <sub>OFF</sub>	Gate Driver OFF Output Resistance			0.96	1.2	1.44	kΩ

### BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified)

V <sub>FB</sub>	Forward Voltage	I <sub>F</sub> = 0.1 A, T <sub>C</sub> = 25°C (Note 8)	–	2.5	–	V
t <sub>rrB</sub>	Reverse Recovery Time	I <sub>F</sub> = 0.1 A, T <sub>C</sub> = 25°C	–	80	–	ns

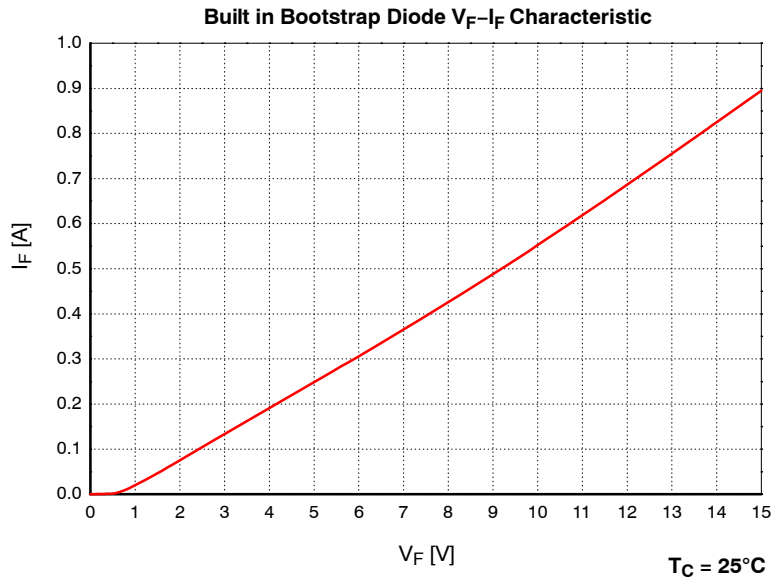
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply Voltage	Applied between P and N	–	300	400	V
$V_{DD}$	Control Supply Voltage	Applied between $V_{DD}$ and COM	13.5	15.0	18.5	V
$V_{BS}$	High-Side Bias Voltage	Applied between $V_B$ and $V_S$	13.5	15.0	18.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between $V_{IN}$ and COM	3.0	–	$V_{DD}$	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	–	0.6	V
$t_{dead}$	Blanking Time for Preventing Arm-Short	$V_{DD} = V_{BS} = 13.5\sim 16.5$ V, $T_J \leq 150^\circ\text{C}$	2	–	–	$\mu\text{s}$
		$V_{DD} = V_{BS} = 12.3\sim 14.4$ V, $T_J \leq 150^\circ\text{C}$	1	–	–	$\mu\text{s}$
$f_{PWM}$	PWM Switching Frequency	$T_J \leq 150^\circ\text{C}$	–	15	–	kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

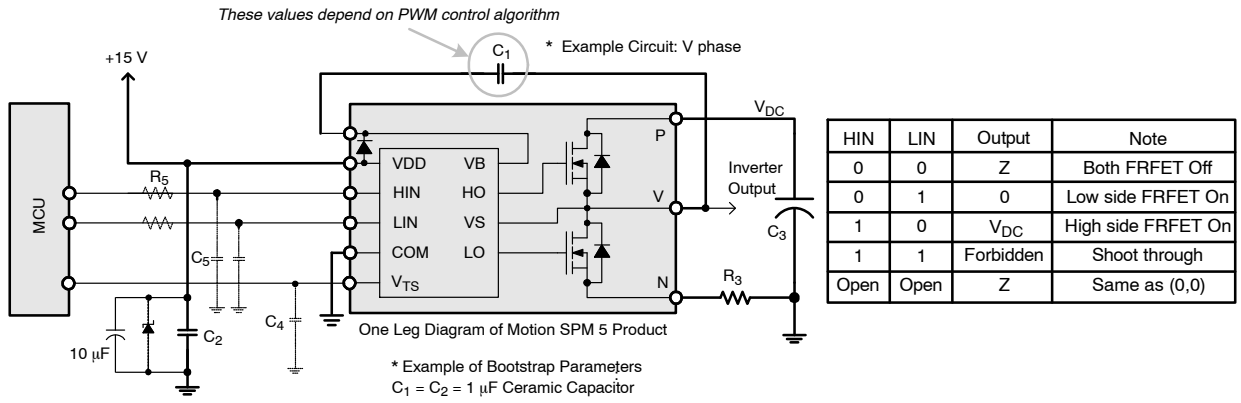


**Figure 2. Built in Bootstrap Diode Characteristics (Typical)**

### NOTES:

- $BV_{DSS}$  is the absolute maximum voltage rating between drain and source terminal of each MOSFET inside Motion SPM 5 product.  $V_{PN}$  should be sufficiently less than this value considering the effect of the stray inductance so that  $V_{PN}$  should not exceed  $BV_{DSS}$  in any case.
- $t_{ON}$  and  $t_{OFF}$  include the propagation delay of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 6 for the switching time definition with the switching test circuit of Figure 7.
- The peak current and voltage of each MOSFET during the switching operation should be included in the Safe Operating Area (SOA). Please see Figure 7 for the RBSOA test circuit that is same as the switching test circuit.
- $V_{IS}$  is only for sensing-temperature of module and cannot shutdown MOSFETs automatically.
- Built in bootstrap diode includes around  $15\ \Omega$  resistance characteristic. Please refer to Figure 2.

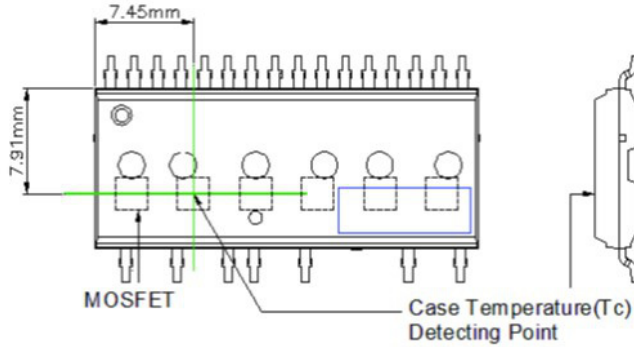
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**Figure 3. Recommended MCU Interface and Bootstrap Circuit with Parameters**

**NOTES:**

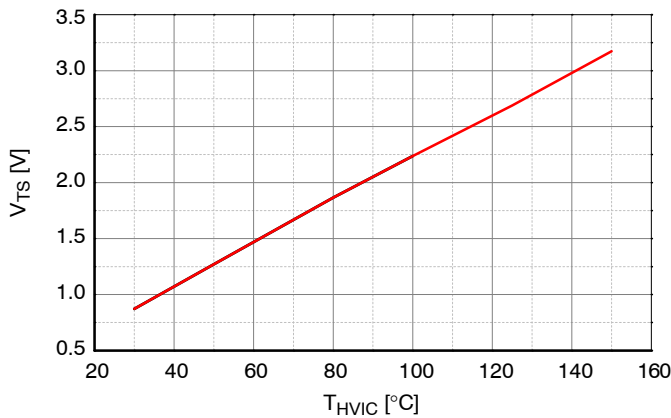
9. Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
10. RC-coupling (R<sub>5</sub> and C<sub>5</sub>) and C<sub>4</sub> at each input of Motion SPM and MCU (Indicated as Dotted Lines) may be used to prevent improper signal due to surge-noise.
11. Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge-voltage. Bypass capacitors such as C<sub>1</sub>, C<sub>2</sub> and C<sub>3</sub> should have good high-frequency characteristics to absorb high-frequency ripple-current.



**Figure 4. Case Temperature Measurement**

**NOTE:**

12. Attach the thermocouple on top of the heat-sink of SPM 5 package (between SPM 5 package and heatsink if applied) to get the correct temperature measurement.



**Figure 5. Temperature Profile of V<sub>TS</sub> (Typical)**

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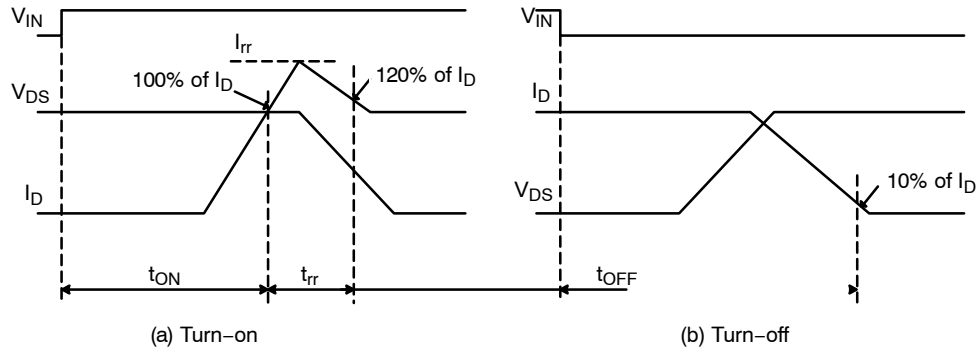


Figure 6. Switching Time Definitions

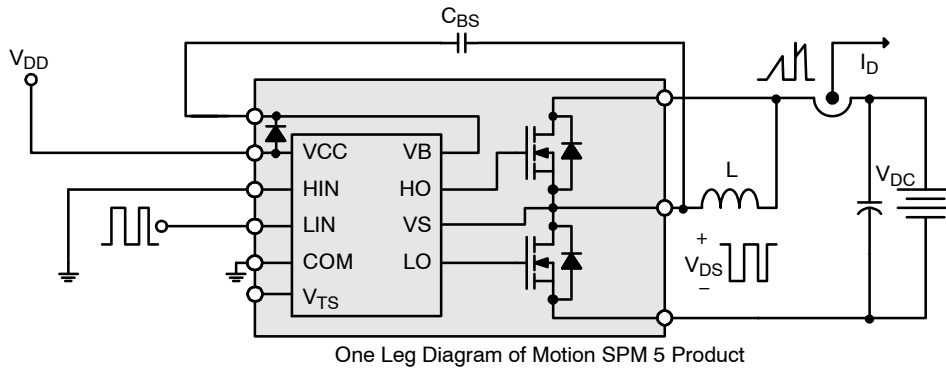


Figure 7. Switching and RBSOA (Single-Pulse) Test Circuit (Low-side)

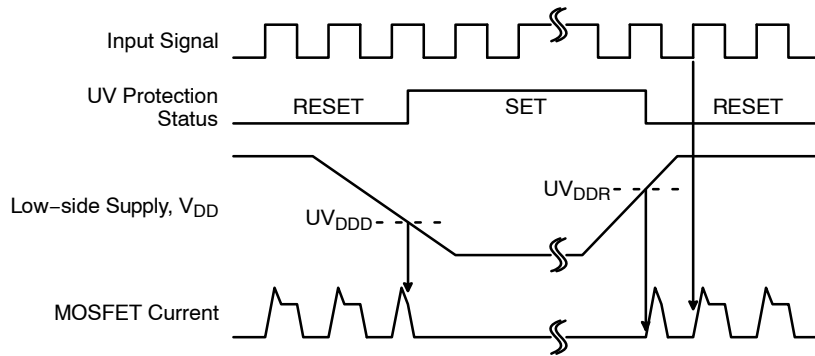


Figure 8. Under-Voltage Protection (Low-Side)

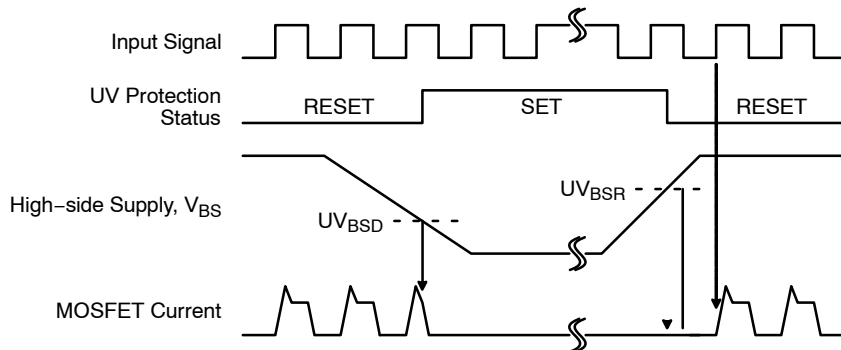
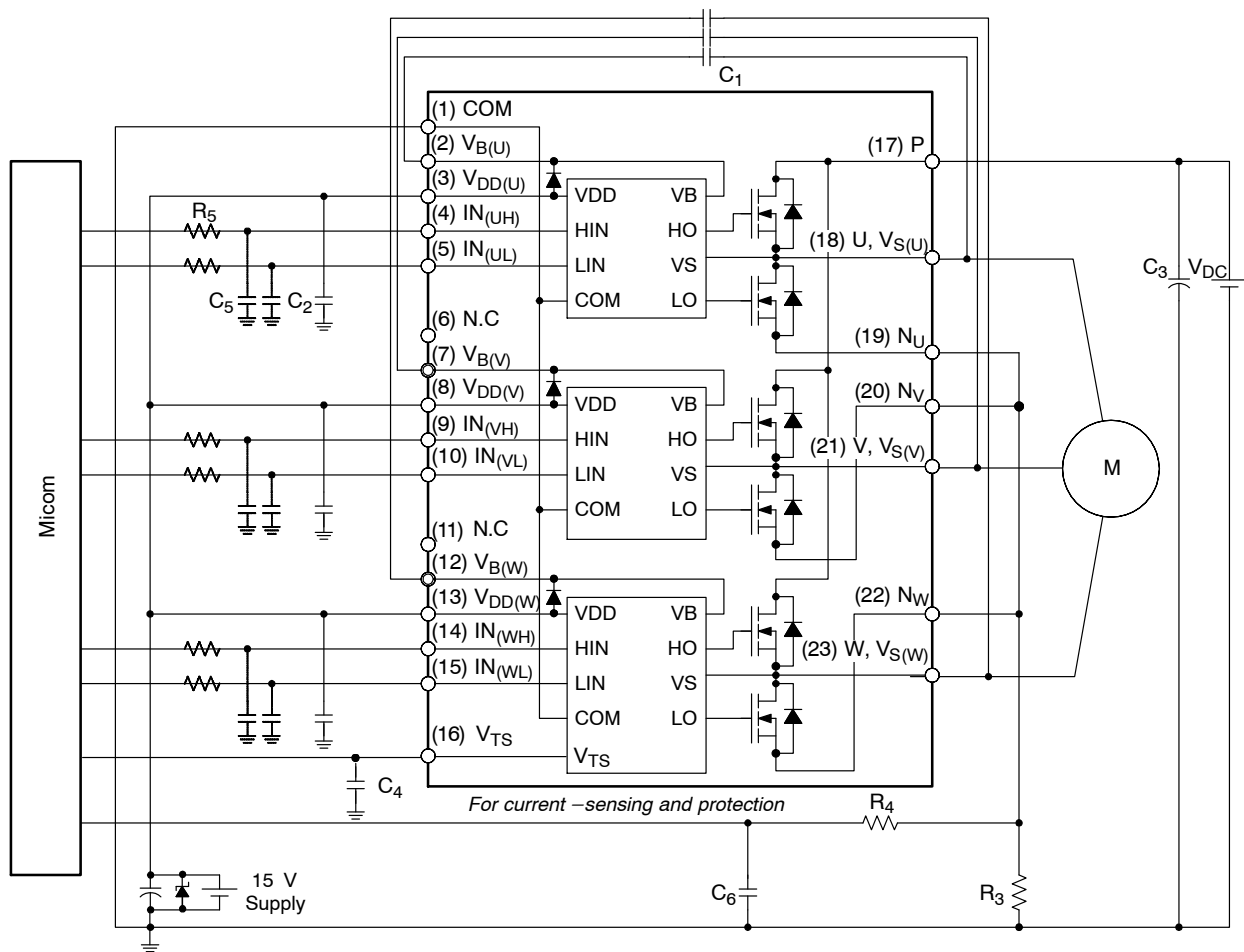


Figure 9. Under-Voltage Protection (High-Side)

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**Figure 10. Example of Application Circuit**

**NOTES:**

- 13. About pin position, refer to Figure 1.
- 14. RC-coupling ( $R_5$  and  $C_5$ ,  $R_4$  and  $C_6$ ) and  $C_4$  at each input of Motion SPM 5 product and MCU are useful to prevent improper input signal caused by surge-noise.
- 15. The voltage-drop across  $R_3$  affects the low-side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low-side MOSFET. For this reason, the voltage drop across  $R_3$  should be less than 1 V in the steady-state.
- 16. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
- 17. All the filter capacitors should be connected close to Motion SPM 5 product, and they should have good characteristics for rejecting high-frequency ripple current.



# MECHANICAL CASE OUTLINE

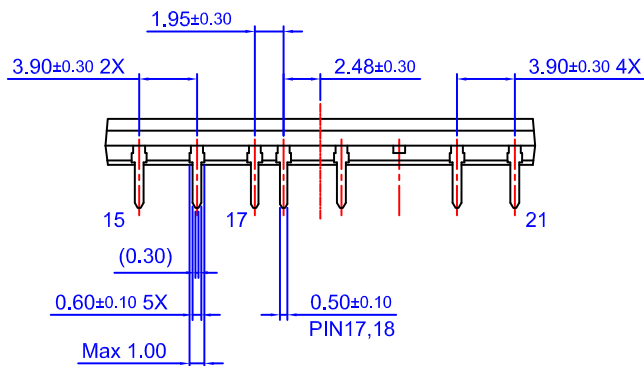
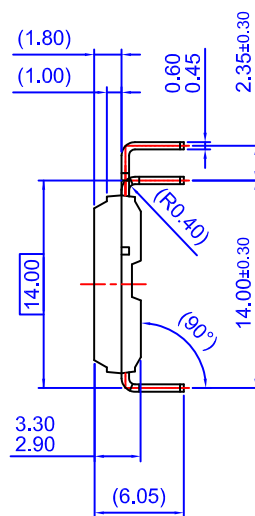
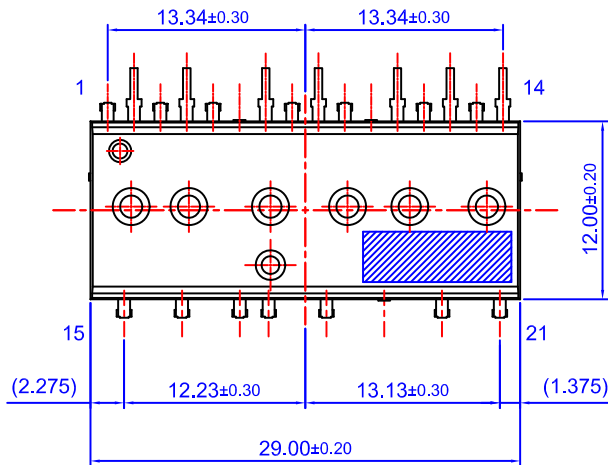
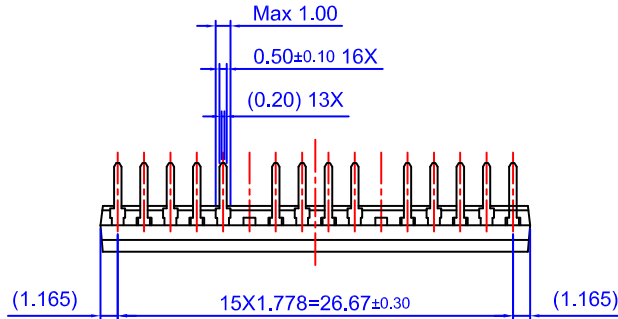
## PACKAGE DIMENSIONS

ON Semiconductor®



### SPM5T-021 / 21LD, PDD STD, FULL PACK, DOUBLE DIP TYPE CASE MODET ISSUE O

DATE 31 JAN 2017



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