USB Type-C Analog Audio Switch with Protection Function

FSA4476

WLCSP25, 2.03x2.03x0.586
CASE 567UP

MARKING DIAGRAM

GR = Device Code
&K = 2−Digits Lo Run Traceability Code
&2 = 2−Digit Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

Description

FSA4476 is a high performance USB Type−C port multimedia switch which supports analog audio headsets. FSA4476 allows the sharing of a common USB Type−C port to pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal. FSA4476 also supports high voltage on CC port, SBU port and USB port on USB Type−C receptacle side. In addition, FSA4476 supports USB Type−C dead battery application and dual power supply with VBAT rail and VBUS rail.

Features

- Power Management
  - Primary Power Supply: VBAT, 2.7 V to 5.5 V
  - Second Power Supply VBUS, 4.0 V to 20 V
- USB High Speed (480 Mbps) Switch:
  - −3 dB Bandwidth: 1 GHz
  - 3 Ω R_{ON} Typical
- Audio Switch
  - Negative Rail Capability: −3 V to +3 V
  - THD+N = −110 dB; 1 V_{RMS}, f = 20 Hz~20 kHz, 32 Ω Load
  - 0.6 Ω R_{ON} Typical
- High Voltage Protection
  - 20 V DC Protection on CC Port and SBU Port
  - 16 V DC Protection on DP/R and DN/L Port
- Over Voltage Protection:
  - 5.8 V (Typ) on CC Port
  - 4.5 V (Typ) on SBU Port
  - 4.5 V (Typ) on DP/R and DN/L Port
- OMTP and CTIA Pinout Support
- Support Audio Sense Path
- Support Dead Battery
- 25−ball WLCSP Package (2.03 mm x 2.03 mm)
- This is a Pb−Free Device

Applications

- Mobile Phone, Tablet, Notebook PC, Media Player

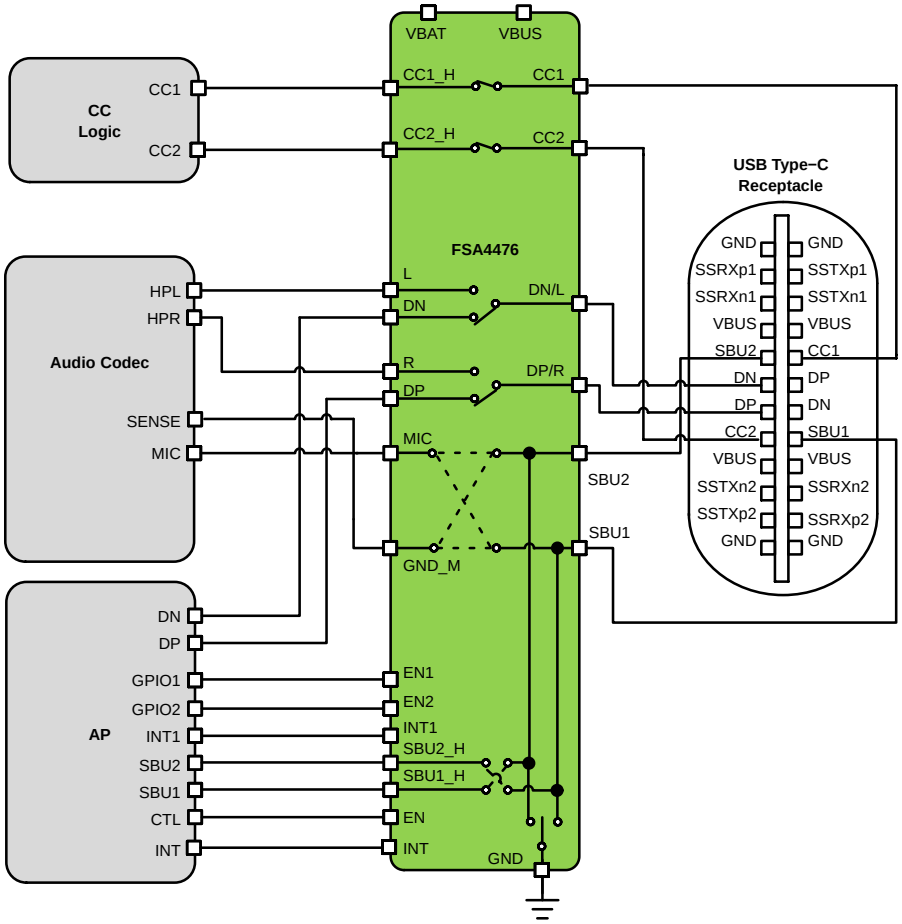


Figure 1. Application Block Diagram

PIN CONFIGURATION

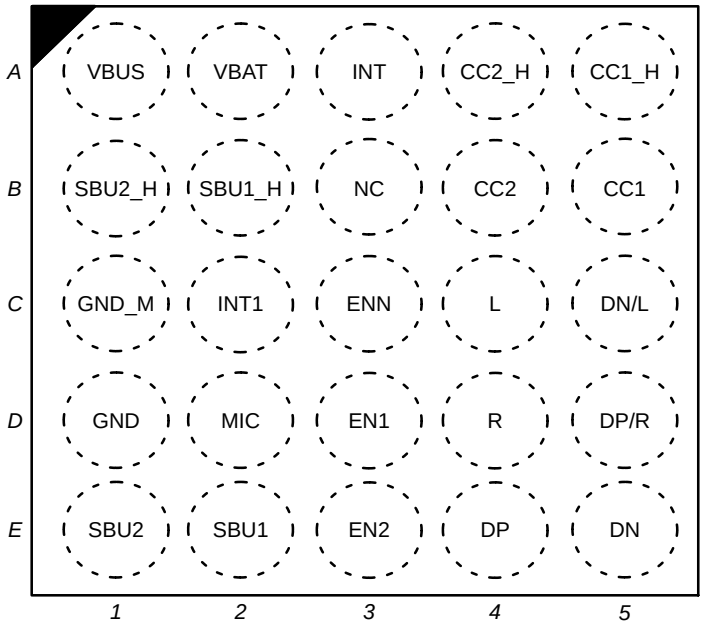


Figure 2. Pin Assignment (Top Through View)

PIN DESCRIPTIONS

Name	Ball	Description
VBUS	A1	Power Supply
VBAT	A2	Power Supply
GND	D1	Ground
DP/R	D5	USB Positive Data/Right Audio Common Line
DN/L	C5	USB Negative Data/Left Audio Common Line
DP	E4	Positive DataLine for USB signals
DN	E5	Negative DataLine for USB signals
L	C4	Left Line for Audio Signals
R	D4	Right Line for Audio Signals
SBU1	E2	Sideband Use Wire 1 Common Line
SBU2	E1	Sideband Use Wire 2 Common Line
MIC	D2	Microphone, connects to microphone pre−amplifier
GND_M	C1	Sense Pin to Detect GND offset
SBU1_H	B2	Host Side Sideband Use Wire 1
SBU2_H	B1	Host Side Sideband Use Wire 2
CC1	B5	Configuration Channel 1
CC2	B4	Configuration Channel 2
CC1_H	A5	Host Side Configuration Channel 1
CC2_H	A4	Host Side Configuration Channel 2
INT	A3	OVP Interrupt Output, active low (open drain)
INT1	C2	Interrupt Output Signal; During EN1=1, INT1 is low active (open drain output) when CC1_H < 1.2 V and CC2_H < 1.2 V.
ENN	C3	Chip Enable, active low, internal pull−down by 1Mohm.
EN1	D3	Logic Configuration Input 1
EN2	E3	Logic Configuration Input 2
NC	B3	No Connect

TRUTH TABLE

Power	ENN	EN1,EN2	CC Switch	Headset Detection	USB Switch	Audio Switch	MIC SW / GND_M SW	SBU Bypass Switch
OFF	X	XX	Dead battery	OFF	OFF	OFF	OFF	OFF
ON	H	XX	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	00	ON	OFF	ON: DP/R to DP DN/L to DN	OFF	OFF	ON: SBU1 to SBU1_H SBU2 to SBU2_H
ON	L	01	ON	OFF	ON: DP/R to DP DN/L to DN	OFF	OFF	ON: SBU1 to SBU2_H SBU2 to SBU1_H
ON	L	10	ON	ON	OFF	ON: DP/R to R DN/L to L	ON: SBU1 to MIC SBU2 to GND_M SBU2 to GND	OFF
ON	L	11	ON	ON	OFF	ON: DP/R to R DN/L to L	ON: SBU2 to MIC SBU1 to GND_M SBU1 to GND	OFF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{BAT}	Supply Voltage from VBAT		−0.5	6.5	V
VBUS	Supply Voltage from VBUS		−0.5	28	V
V_{VICC}	V_{CCx}, to GND		−0.5	20	V
V_{VCC_H}	V_{CCx_H}, to GND		−0.5	6.5	V
$V_{SW\_USB/Audio}$	V_{DP_R} to GND, V_{DN_L} to GND		−3.5	16	V
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND		−0.5	6.5	V
V_{SW_Audio}	V_L to GND, V_R to GND		−3.5	+3.5	V
V_{VSBU}	V_{SBU1} to GND, V_{SBU2} to GND		−0.5	20	V
V_{VSBU_H}	V_{SBU1_H} to GND, V_{SBU2_H} to GND		−0.5	6.5	V
$V_{I/O}$	MIC,GND_M, INT,INT1to GND		−0.5	6.5	V
V_{CNTRL}	Control Input Voltage	ENN, ENx	−0.5	6.5	V
I_{CCSW}	CC Switch Current		−	1.25	A
I_{SW_Audio}	Switch I/O Current, Audio Path		−250	250	mA
I_{SW_USB}	Switch I/O Current, USB Path		−	100	mA
I_{SW_MIC}	Switch I/O Current, MIC to SBU1 or SBU2		−	50	mA
$I_{SW\_GND\_M}$	Switch I/O Current, GND_M to SBU1 or SBU2		−	100	mA
I_{SW_GND}	Switch I/O Current, GND to SBU1 or SBU2		−	500	mA
I_{IK}	DC Input Diode Current		−50	−	mA
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	Connector Side and Power Pins: VBUS, V_{BAT}, CC1, CC2, SBU1, SBU2, DP/R, DN/L	4	−	kV
		Host Side Pins: The Rest Pins	2	−	
	Charged Device Model, JEDEC: JESD22−C101		1	−	
T_A	Absolute Maximum Operating Temperature		−40	+85	°C
T_{STG}	Storage Temperature		−65	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Max	Unit
POWER					
VBAT	Supply Voltage	2.7	−	5.5	V
VBUS	Supply Voltage	4.0	−	20	V
USB SWITCH					
VSW_USB	V_{DP} to GND, V_{DN} to GND, $V_{DP/Rto}$ GND, $V_{DN/L}$ to GND	0	−	4.0	V
AUDIO SWITCH					
VSW_Audio	$V_{DP/Rto}$ GND, $V_{DN/L}$ to GND, V_L to GND, V_R to GND	−3	−	+3	V
VSW_MIC	MIC to GND	0	−	3.6	V
SBU SWITCH					
VVSBU	V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND	0	−	4.0	V
CC SWITCH					
VVICC	V_{CCx}, to GND	0	−	5.5	V
VVCC_H	V_{CCx_H}, to GND	0	−	5.5	V
ICCSW	CC Switch Current		−	1.25	A
CONTROL VOLTAGE (ENN, ENX)					
VIH	Input Voltage High	1.3	−	−	V
VIL	Input Voltage Low	−	−	0.5	V
OPERATING TEMPERATURE					
TA	Ambient Operating Temperature	−40	25	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (VBAT = 2.7 V to 5.5 V or VBUS = 4.0 V to 20 V, VBAT (Typ.) = 4.3 V or VBUS (Typ.) = 5 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (Note 1)

Symbol	Parameter	Condition	Power	T_A=−40°C to +85°C			Unit
				Min	Typ	Max	
I_{CC}	VBAT Supply Current		VBAT = 4.3 V	−	25	−	μA
I_{CCZ}	Quiescent Current		VBAT = 4.3 V	−	5	−	μA
USB/AUDIO COMMON PINS							
I_{OZ}	Off Leakage Current of Port DP/R and DN/L	DN/L, DP/ R = −3 V to 4.0 V	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−3.0	−	3.0	μA
I_{OFF}	Power−Off Leakage Current of Port DP/R and DN/L	DN/L, DP/R = 0 V to 4.0 V	Power off	−3.0	−	3.0	μA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	4.2	4.5	4.8	V
V_{OV_HYS}	Input OVP Hysteresis			−	0.3	−	V
AUDIO SWITCH							
I_{ON}	On Leakage Current of Audio Switch	DN/L, DP/R = −3 V to 3.0 V, DP, DN, R, L = Float	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−2.0	0.1	2.0	μA
I_{OFF}	Power−Off Leakage Current on L and R	L, R = 0 V to 3 V	Power off	−1.0	−	1.0	μA
R_{ON}	Switch On Resistance	I_{SW} = 100 mA, V_{SW} = −3 V to 3 V	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−	0.6	−	Ω
R_{SHUNT}	Pull Down Resistor on R/L Pin when Audio Switch is Off	L = R = 3 V		6	10	14	kΩ
USB SWITCH							
I_{ON}	On Leakage Current of USB Switch	DN/L, DP/R = 0 V to 4.0 V, DP, DN, R, L = Float	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−3.0	1.0	3.0	μA
I_{OZ}	Off Leakage Current of Port DP and DN	DN, DP = 0 V to 4.0 V		−3.0	−	3.0	μA
I_{OFF}	Power−Off Leakage Current on DP and DN	DN, DP = 0 V to 4.0 V	Power off	−3.0	−	3.0	μA
R_{ON_USB}	USB Switch On Resistance	I_{SW} = 8 mA, V_{SW} = 0.4 V	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−	3	−	Ω
CC SWITCH							
I_{ON}	On Leakage Current of CC Switch	Vsw from 0 V to 3.6 V	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−1.5	−	2.0	μA
R_{ON}	CC Path On Resistance	I_{OUT} = 200 mA, V_{SW} = 5 V		−	300	−	mΩ
V_{OV_TRIP}	Input OVP Lockout	Rising edge		5.6	5.8	6.1	V
V_{OV_HYS}	Input OVP Hysteresis			−	0.3	−	V
R_d	Dead Battery Pull Down Resistance	350 μA on CCx pin	VBAT < 2.4 V and VBUS < 3.5 V	4.08	5.1	6.12	kΩ
V_{THR_H}	CCx_H High Threshold under Headset Detection	EN1 = H	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−	1.5	−	V
V_{THR_L}	CCx_Hlow Threshold under Headset Detection	EN1 = H		−	1.2	−	V
SBU COMMON PINS							
I_{OZ}	Off Leakage Current of Port SBUx	SBUx = 0 V to 4 V	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−3.0	−	3.0	μA
I_{OFF}	Power−Off Leakage Current of Port SBUx	SBUx= 0 V to 4 V	Power off	−3.0	−	3.0	μA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	4.2	4.5	4.8	V
V_{OV_HYS}	Input OVP Hysteresis			−	0.3	−	V

DC CHARACTERISTICS (VBAT = 2.7 V to 5.5 V or VBUS = 4.0 V to 20 V, VBAT (Typ.) = 4.3 V or VBUS (Typ.) = 5 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (Note 1) (continued)

Symbol	Parameter	Condition	Power	T_A=−40°C to +85°C			Unit
				Min	Typ	Max	
MIC SWITCH							
I_{ON}	On Leakage Current of MIC Switch	SBUx = 0 V to 3.6 V, MIC is floating	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−3.0	−	3.0	μA
I_{OZ}	Off Leakage Current on MIC	MIC = 0 V to 3.6 V		−1.0	−	1.0	μA
I_{OFF}	Power Off Leakage Current on MIC	MIC = 0 V to 3.6 V	Power off	−1.0	−	1.0	μA
R_{ON}	MIC Switch On Resistance	MIC = 0 V to 3.6 V, Isw = 30 mA	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−	2	−	Ω
GND_M SWITCH							
I_{OZ}	Off Leakage on GND_M	GND_M = 0 V to 3.6 V	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−2.0	−	2.0	μA
I_{OFF}	Power Off Leakage Current on GND_M	GND_M = 0 V to 3.6 V	Power off	−1.0	−	1.0	μA
R_{ON}	GND_M Switch On Resistance	Isw = 30 mA	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−	0.5	−	Ω
SBU BYPASS SWITCH							
I_{ON}	On Leakage Current of SBU Bypass Switch	SBUx= 0 V to 4 V, SBUx_H is floating	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−1.0	−	2.0	μA
I_{OZ}	Off Leakage Current on SBUx_H	SBUx_H = 0 V to 4 V		−1.0	−	1.0	μA
R_{ON}	SBU Bypass Switch On Resistance	SBUx = 0 V to 3.6 V, Isw = 50 mA		−	3	−	Ω
INTERNAL GND SWITCH							
R_{ON}	Internal GND Switch On Resistance	Isw = 200 mA	VBAT: 2.7 V to 5.5 V or VBUS: 4 V to 20 V	−	75	110 (Note 2)	mΩ

1. Limits over the recommended temperature operating range (T_A = −40°C to +85°C) are correlated by statistical quality.
2. Guaranteed by characterization, not production tested.

AC CHARACTERISTICS (VBAT = 2.7 V to 5.5 V or VBUS = 4.0 V to 20 V, VBAT (Typ.) = 4.3 V or VBUS (Typ.) = 5 V, T_A = −40°C to 85°C. T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	T_A=−40°C to +85°C			Unit
				Min	Typ	Max	
AUDIO SWITCH							
t_{ON}	Turn On Time (Note 3)	DP/R = DN/L = 1.5 V, R_L = 50 Ω	VBAT: 4.3 V or VBUS: 5 V	−	55	−	μs
t_{OFF}	Turn OFF Time (Note 3)	DP/R = DN/L = 1.5 V, R_L = 50 Ω		−	2	−	μs
X_{TALK}	Cross Talk (Adjacent) (Note 3)	f = 1 kHz, R_L = 50 Ω, V_{SW} = 1 V_{RMS}		−	−110	−	dB
BW	−3 dB Bandwidth (Note 3)	R_L = 50 Ω		−	950	−	MHz
O_{IRR}	Off Isolation (Note 3)	f= 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}		−	−100	−	dB
THD+N	Total Harmonic Distortion + Noise Performance with A− Weighting Filter (Note 3)	R_L = 600 Ω, f = 20 Hz~20 kHz, V_{SW} = 2 V_{RMS}		−	−110	−	dB
		R_L = 32 Ω, f = 20 Hz~20 kHz, V_{SW} = 1 V_{RMS}		−	−110	−	dB
		R_L = 16, , f = 20 Hz~20 kHz, V_{SW} = 0.5 V_{RMS}		−	−108	−	dB
USB SWITCH							
t_{ON}	Turn−on Time (Note 3)	DP/R = DN/L = 1.5 V, R_L = 50 Ω	VBAT: 4.3 V or VBUS: 5 V	−	40	−	μs
t_{OFF}	Turn−off Time (Note 3)	DP/R = DN/L = 1.5 V, R_L = 50 Ω		−	1	−	μs
BW	−3 dB Bandwidth (Note 3)	R_L = 50 Ω		−	1	−	GHz
O_{IRR}	Off Isolation (Note 3) between DP, DN and Common Node Pins	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}		−	−100	−	dB
t_{OVP}	DP/R and DN/L Pins OVP Response Time (Note 3)	R_L = 50 Ω, Vsw = 3.5 V to 5.5 V		−	0.5	1.5	μs
CC SWITCH							
t_{ON}	Turn−On Time (Note 3)	V_{ICCx} = 5 V, R_L = 5 kΩ	VBAT: 4.3 V or VBUS: 5 V	−	0.5	−	ms
t_{OFF}	Turn−Off Time (Note 3)	V_{ICCx} = 5 V, R_L = 5 kΩ		−	3	−	μs
BW	PD Traffic Bandwidth (Note 3)	R_L = 50 Ω		−	25	−	MHz
t_{OVP}	CCx Pins OVP Response Time (Note 3)	R_L= 25 Ω, C_L = 200 pF, V_{SW}: 4 V to 7 V		−	0.6	1	μs
SBUX BYPASS SWITCH							
t_{OVP}	SBUx Pins OVP Response Time (Note 3)	R_L = 50 Ω, Vsw = 3.5 V to 5.5 V	VBAT: 4.3 V or VBUS: 5 V	−	0.6	1	μs
t_{ON}	Turn−On Time (Note 3)	Isw on SBUx = 1 mA and clamp to 2 V, $R_L$on MIC and SBUx_H = 1 kΩ, GND_M = 100 mV, series 50 Ω on GND_M pin	VBAT: 4.3 V or VBUS: 5 V	−	12	−	μs
t_{OFF}	Turn−OFF Time (Note 3)			−	1	−	
BW	Bandwidth (Note 3)	R_L = 50 Ω		−	25	−	MHz

AC CHARACTERISTICS (VBAT = 2.7 V to 5.5 V or VBUS = 4.0 V to 20 V, VBAT (Typ.) = 4.3 V or VBUS (Typ.) = 5 V, T_A = −40°C to 85°C. T_A (Typ.) = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Power	T_A=−40°C to +85°C			Unit
				Min	Typ	Max	
MIC/GND_M/INTERNAL GND SWITCH							
t_{ON_MIC}	Turn−On Time (Note 3)	Isw on SBUx = 1 mA and clamp to 2 V, R_L on MIC and SBUx_H = 1 kΩ, GND_M = 100 mV, series 50 Ω on GND_M pin	VBAT: 4.3 V or VBUS: 5 V	−	10	−	μs
$t_{ON\_GND\_M}$				−	60	−	
t_{ON_GND}				−	950	−	
t_{OFF_MIC}	Turn−OFF Time (Note 3)				1	−	
$t_{OFF\_GND\_M}$				−	1	−	
t_{OFF_GND}				−	1	−	
BW	MIC Switch Bandwidth (Note 3)	R_L = 50 Ω		−	25	−	MHz
INTERRUPT DELAY							
T_{DELAY_INT}	INT Response Delay (Note 3)	INT pull up by 10k resistor to valid power	VBAT: 4.3 V or VBUS: 5 V	−	5	−	μs
T_{DELAY_INT1}	INT1 Response Delay (Note 3)	INT1 pull up by 10k resistor to valid power		−	5	−	

3. Guaranteed by characterization, not production tested

CAPACITANCE (Unless otherwise stated VBAT = 2.7 V to 5.5 V or VBUS = 4.0 V to 20 V, VBAT (Typ.) = 4.3 V or VBUS (Typ.) = 5 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C.)

Symbol	Parameter	Condition		Power	T_A=−40°C to +85°C			Unit
					Min	Typ	Max	
$C_{ON\_USB/Audio}$	On Capacitance (Common Port) (Note 4)	f = 1 MHz, 100 $mV_{PK−PK}$, 100 mV DC bias		VBAT: 4.3 V or VBUS: 5 V	−	7	−	pF
$C_{OFF\_USB/Audio}$	Off Capacitance (Common Port) (Note 4)	f = 1 MHz, 100 $mV_{PK−PK}$, 100 mV DC bias			−	7	−	pF
C_{OFF_USB}	Off Capacitance (Non−Common Ports) (Note 4)	f = 1 MHz, 100 $mV_{PK−PK}$, 100 mV DC bias Figure 12			−	2	−	pF
$C_{OFF\_SBUx\_H}$	Off Capacitance (Non−Common Ports) (Note 4)	f = 1 MHz, 100 $mV_{PK−PK}$, 100 mV DC bias			−	12	−	pF
C_{OFF_SBUx}	Off Capacitance (Common Ports) (Note 4)	f = 1 MHz, 100 $mV_{PK−PK}$, 100 mV DC bias			−	140	−	pF
C_{ON_SBUx}	On Capacitance (Common Port) (Note 4)	f = 1 MHz, 100 $mV_{PK−PK}$, 100 mV DC bias			−	150	−	pF
C_{CNTRL}	Control Input Pin Capacitance (ENx) (Note 4)	f = 1 MHz, 100 mV_{PP}, 100 mV DC bias	ENx, ENN		−	6	−	pF

4. Guaranteed by characterization, not production tested

APPLICATION INFORMATION

Dead Battery

FSA44776 supports dead battery application. When power is not applied to FSA4476 and it is attached to a Source device, then the Source would pull up the CC line connected through the cable. FSA4476 in response would turn on the pull−down that will bring the CC voltage to a range that the Source can detect an attach event and turn on VBUS.

Headset detection

FSA4476 integrates headset unplug detection function by detecting the CCx_H voltage. The headset detection is only active during audio switch on status(EN1 = 1). When headset is attached (both CC1_H and CC2_H are Low), the flag signal is sent low to host controller by INT1 (INT1 = low). Once either of CCx_H = High (CCx_H > 1.5 V), INT1 will be released to high by external pull up resistor.

POWER SUPPLY CONFIGURATION

VBUS	VBAT	Power Supply
Invalid	Invalid	Max (VBAT, VBUS)
Valid	Invalid	VBUS
Invalid	Valid	VBAT
Valid	Valid	VBAT

TEST DIAGRAMS

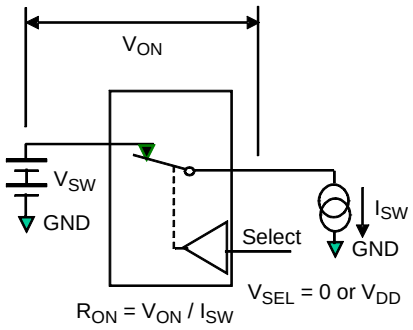
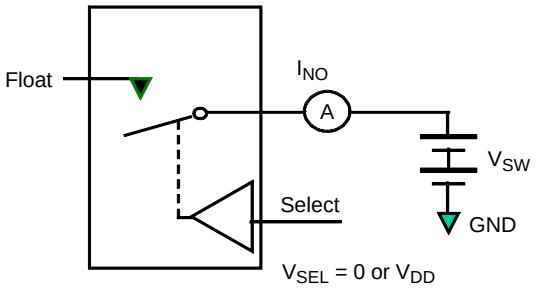


Figure 3. On Resistance



**Each switch port is tested separately

Figure 4. Off Leakage (Ioz)

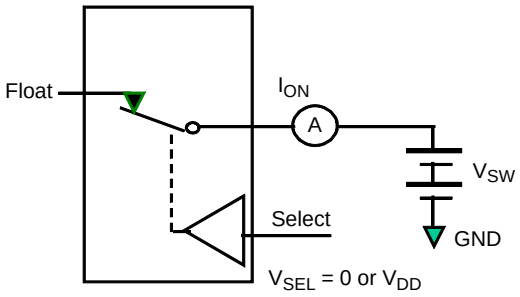
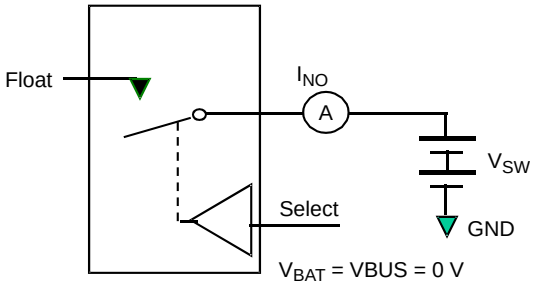


Figure 5. On Leakage



**Each switch port is tested separately

Figure 6. Power Off Leakage (Ioff)

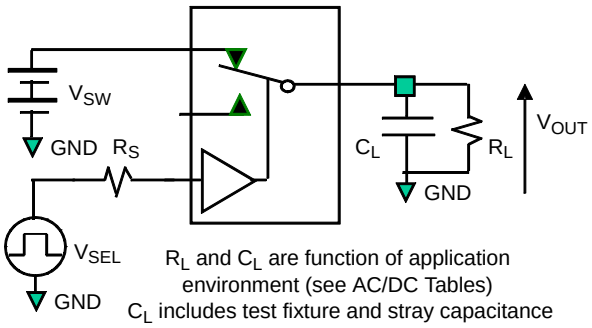


Figure 7. Test Circuit Load

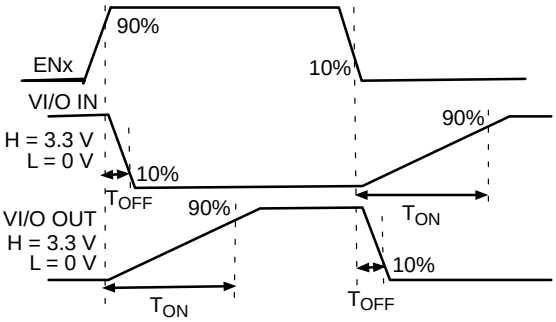


Figure 8. Turn On/Off Waveforms

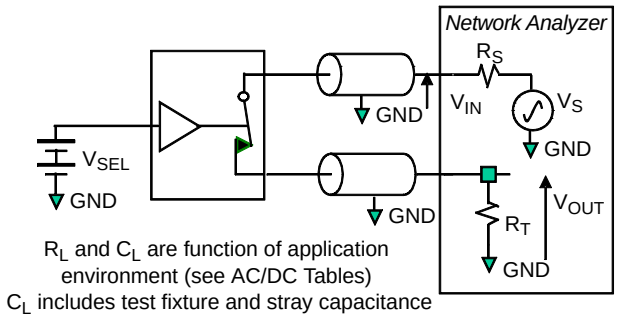


Figure 9. Bandwidth

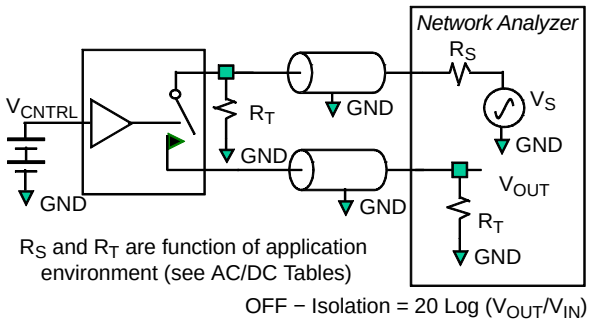
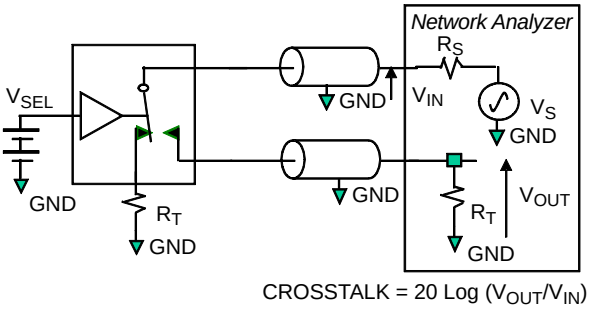


Figure 10. Channel Off Isolation



CROSSTALK = 20 Log (V_{OUT}/V_{IN})

R_S and R_T are function of application environment (see AC/DC Tables)

Figure 11. Adjacent Channel Crosstalk

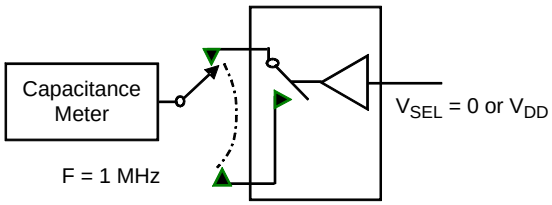


Figure 12. Channel Off Capacitance

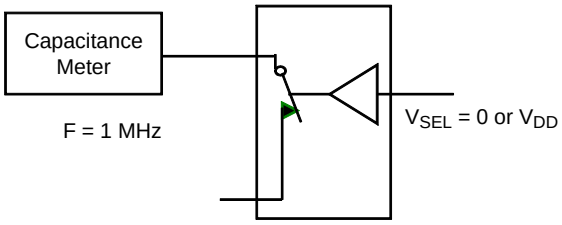
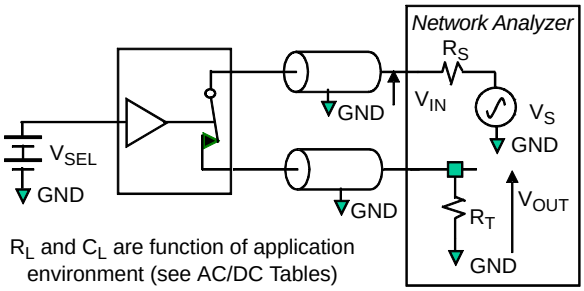


Figure 13. Channel On Capacitance



R_L and C_L are function of application environment (see AC/DC Tables)

C_L includes test fixture and stray capacitance

Figure 14. Total Harmonic Distortion (THD+N)

ORDERING INFORMATION

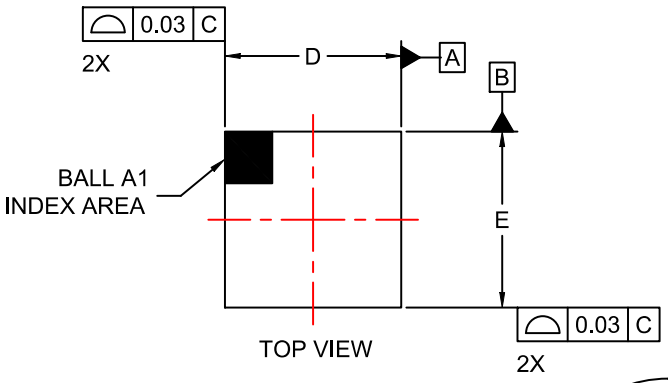
Part Number	Top Mark	Package Description	Shipping†
FSA4476UCX	GR	25 Ball WLCSP25, 2.03x2.03x0.586 (Pb−Free)	3000 / Tape & Reel

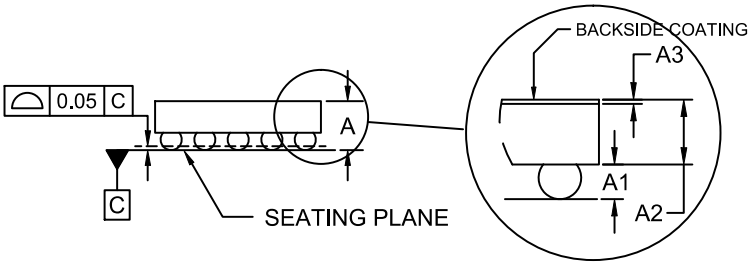
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

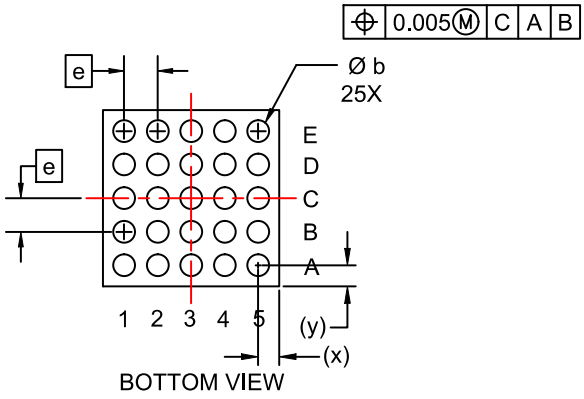
WLCSP25, 2.03x2.03x0.586
CASE 567UP
ISSUE A

DATE 21 MAY 2019

SCALE 4:1



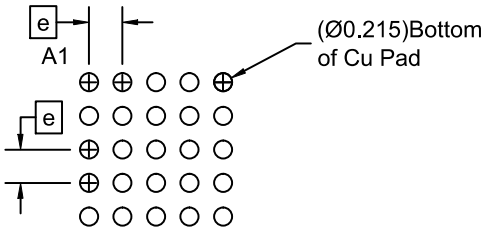




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MIN.	NOM.	MAX.
A	0.547	0.586	0.625
A1	0.188	0.208	0.228
A2	0.337	0.353	0.369
A3	0.022	0.025	0.028
b	0.24	0.26	0.28
D	2.00	2.03	2.06
E	2.00	2.03	2.06
e	0.40 BASIC		
x	0.200	0.215	0.230
y	0.200	0.215	0.230



RECOMMENDED
MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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