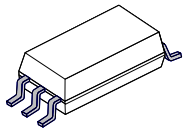
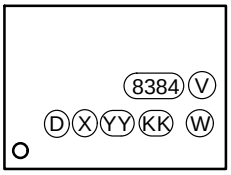
2.5 A Output Current, High-Speed, MOSFET/IGBT Gate Drive Optocoupler in OPTOPLANAR® Wide-Body SOP 5-Pin

FOD8384



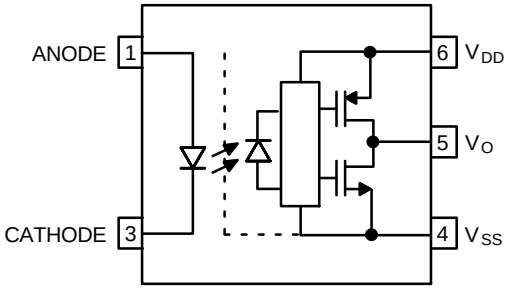
SOIC6 W LESS PIN 2
CASE 752AG

MARKING DIAGRAM



8384 = Device number, e.g., '8384' for FOD8384
V = DIN EN/IEC60747−5−5 Option (Only Appears on Component Ordered with This Option)
D = Plant Code
X = Last Digit Year Code
YY = Two−digit Work Week
KK = Lot Traceability Code
W = Package Assembly Code

FUNCTIONAL SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

Description

The FOD8384 is a 2.5 A output current gate drive optocoupler capable of driving medium−power IGBT/ MOSFETs. It is ideally suited for fast−switching driving of power IGBT and MOSFET used in motor−control inverter applications and high−performance power systems.

The FOD8384 utilizes **onsemi**'s OPTOPLANAR coplanar packaging technology and optimized IC design to achieve reliable high−insulation voltage and high−noise immunity.

It consists of an Aluminum Gallium Arsenide (AlGaAs) Light−Emitting Diode (LED) optically coupled to an integrated circuit with a high−speed driver for push−pull MOSFET output stage. The device is housed in a wide body, 5−pin, small−outline, plastic package.

Features

- Reliable and High−Voltage Insulation with Greater than 8 mm Creepage and Clearance Distance and 0.5 mm Internal Insulation Distance
- 2.5 A Output Current Driving Capability for Medium−Power IGBT/MOSFET
  - P−Channel MOSFET at Output Stage Enables Output Voltage Swing Close to Supply Rail
- 35 kV/μs Minimum Common Mode Rejection
- Wide Supply Voltage Range: 15 V to 30 V
- Fast Switching Speed Over Full Operating Temperature Range
  - 210 ns Maximum Propagation Delay
  - 65 ns Maximum Pulse−Width Distortion
- Under−Voltage Lockout (UVLO) with Hysteresis
- Extended Industrial Temperate Range: −40°C to 100°C
- Safety and Regulatory Approvals:
  - UL1577, 5,000 VACRMS for 1 Minute
  - DIN−EN/IEC60747−5−5, 1,414 V Peak Working
- Insulation Voltage
- These are Pb−Free Devices

Applications

- AC and Brushless DC Motor Drives
- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

Related Resources

- FOD3184 − 3 A Output Current, High−Speed MOSFET/IGBT Gate Drive Optocoupler Datasheet
- https://www.onsemi.com/products/interfaces/igbt−mosfet−gate−drivers−optocouplers

TRUTH TABLE

LED	V_{DD} – V_{SS} “Positive Going” (Turn−on)	V_{DD}–V_{SS} “Positive Going” (Turn−off)	V_O
Off	0 V to 30 V	0 V to 30 V	LOW
On	0 V to 11.5 V	0 V to 10 V	LOW
On	11.5 V to 14.5 V	10 V to 13 V	Transition
On	14.5 V to 30 V	13 V to 30 V	HIGH

Pin Configuration

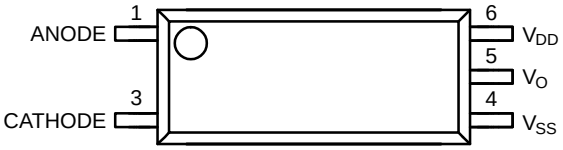


Figure 1. Pin Configuration

PIN DEFINITIONS

Pin No.	Name	Description
1	Anode	LED Anode
3	Cathode	LED Cathode
4	V_{SS}	Negative Supply Voltage
5	V_O	Output Voltage
6	V_{DD}	Positive Supply Voltage

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC60747−5−5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150 V_{RMS}	–	I–IV	–	
	For Rated Mains Voltage < 300 V_{RMS}	–	I–IV	–	
	For Rated Mains Voltage < 450 V_{RMS}	–	I–III	–	
	For Rated Mains Voltage < 600 V_{RMS}	–	I–III	–	
	Climatic Classification	–	40/100/21	–	
	Pollution Degree (DIN VDE 0110/1.89)	–	2	–	
CTI	Comparative Tracking Index	175	–	–	
V_{PR}	Input−to−Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	2651	–	–	
	Input−to−Output Test Voltage, Method a, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	2262	–	–	
V_{IORM}	Maximum Working Insulation Voltage	1414	–	–	V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	8000	–	–	V_{peak}
	External Creepage	8.0	–	–	mm
	External Clearance	8.0	–	–	mm
	Insulation Thickness	0.5	–	–	mm
	Safety Limit Values – Maximum Values Allowed in the Event of a Failure				
T_S	Case Temperature	150	–	–	°C
$I_{S,INPUT}$	Input Current	200	–	–	mA
$P_{S,OUTPUT}$	Output Power	600	–	–	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9	–	–	Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +100	°C
T_J	Junction Temperature	−40 to +125	°C
T_{SOL}	Lead Solder Temperature *Refer to Reflow Temperature Profile on page 13.*	260 for 10 s	°C
$I_{F(AVG)}$	Average Input Current	25	mA
V_R	Reverse Input Voltage	5.0	V
$I_{O(PEAK)}$	Peak Output Current (Note 1)	3.0	A
$V_{DD} – V_{SS}$	Supply Voltage	−0.5 to 35	V
$V_{O(PEAK)}$	Peak Output Voltage	0 to V_{DD}	V
PD_I	Input Power Dissipation (Note 2, 4)	45	mW
PD_O	Output Power Dissipation (Note 3, 4)	500	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%.
2. No derating required across operating temperature range.
3. Derate linearly from 25°C at a rate of 5.2 mW/°C.
4. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	−40	100	°C
$V_{DD} – V_{SS}$	Supply Voltage	15	30	V
$I_{F(ON)}$	Input Current (ON)	10	16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	0	0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ISOLATION CHARACTERISTICS (Apply over all recommended conditions; typical value is measured at T_A = 25°C.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISO}	Input−Output Isolation Voltage	T_A = 25°C, R.H. < 50%, t = 60 s, $I_{I–O} \le$ 20 μA, 50 Hz (Note 5, 6)	5,000	–	–	V_{RMS}
R_{ISO}	Isolation Resistance	$V_{I–O}$ = 500 V (Note 5)	–	10^{11}	–	Ω
C_{ISO}	Isolation Capacitance	$V_{I–O}$ = 0 V, Frequency = 1.0 MHz (Note 6)	–	1	–	pF

5. Device is considered a two−terminal device: pins 1 and 3 are shorted together and pins 4, 5 and 6 are shorted together.
6. 5,000 VAC_{RMS} for 1 minute duration is equivalent to 6,000 VAC_{RMS} for 1 second duration.

ELECTRICAL CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Figure
V_F	Input Forward Voltage	I_F = 10 mA	1.10	1.43	1.80	V	17
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage		–	−1.5	–	mV/°C	
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	5	–	–	V	
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V	–	60	–	pF	
I_{OH}	High Level Output Current (Note 1)	$V_{OH} = V_{DD}$ – 1 V	–	−0.9	−0.5	A	2, 4
		$V_{OH} = V_{DD}$ – 6 V	–	–	−2.5	A	2, 4, 20
I_{OL}	Low Level Output Current (Note 1)	$V_{OL} = V_{SS}$ + 1 V	0.5	1.0	–	A	5, 7
		$V_{OL} = V_{SS}$ + 6 V	2.5	–	–	A	5, 7, 219
V_{OH}	High Level Output Voltage (Note 7, 8)	I_F = 10 mA, I_O = −2.5 A	V_{DD} − 7.0	–	–	V	2
		I_F = 10 mA, I_O = −100 mA	V_{DD} − 0.5	–	–	V	4, 3, 21
V_{OL}	Low Level Output Voltage (Note 7, 8)	I_F = 0 mA, I_O = 2.5 A	–	–	V_{SS} + 7.0	V	5
		I_F = 0 mA, I_O = 100 mA	–	–	V_{SS} + 0.5	V	6, 22
I_{DDH}	High Level Supply Current	V_O = Open, I_F = 7 to 16 mA	–	2.9	3.5	mA	8, 9, 23
I_{DDL}	Low Level Supply Current	$V_{O\,=}$ Open, V_F = 0 to 0.8 V	–	2.8	3.5	mA	8, 9, 24
I_{FLH}	Threshold Input Current Low−to−High	I_O = 0 mA, V_O > 5 V	–	3.1	7.5	mA	10, 16, 25
V_{FHL}	Threshold Input Voltage High−to−Low	I_O = 0 mA, V_O < 5 V	0.8	–	–	V	26
V_{UVLO+}	Under−Voltage Lockout Threshold	I_F = 10 mA, V_O > 5 V	11.5	13.0	14.5	V	18, 27
$V_{UVLO−}$		I_F = 10 mA, V_O < 5 V	10.0	11.5	13.0	V	18, 27
$UVLO_{HYS}$	Under−Voltage Lockout Threshold Hysteresis		–	1.5	–	V	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. In this test, V_{OH} is measured with a dc load current of 100 mA. When driving capacitive load V_{OH} will approach V_{DD} as I_{OH} approaches 0 A.
8. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

SWITCHING CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Figure
t_{PHL}	Propagation Delay Time to Logic LOW Output (Note 9)	I_F = 7 mA to 16 mA, Rg = 10 Ω, Cg =10 nF, f = 250 kHz, Duty Cycle = 50%	50	145	210	ns	11, 12, 13, 14, 15, 28
t_{PLH}	Propagation Delay Time to Logic HIGH Output (Note 10)		50	135	210	ns	11, 12, 13, 14, 15, 28
PWD	Pulse Width Distortion (Note 11) $\lvert t_{PHL} - t_{PLH} \rvert$		–	25	65	ns	
PDD (Skew)	Propagation Delay Difference Between Any Two Parts (Note 12)		−90	–	90		
t_R	Output Rise Time (10% to 90%)		–	35	–	ns	28
t_F	Output Fall Time (90% to 10%)		–	25	–	ns	28
$t_{ULVO\ ON}$	ULVO Turn−On Delay	I_F = 10 mA, V_O > 5 V	–	1.7	–	μs	
$t_{ULVO\ OFF}$	ULVO Turn−Off Delay	I_F = 10 mA, V_O < 5 V	–	0.1	–	μs	
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output HIGH	T_A = 25°C, V_{DD} = 30 V, I_F = 10 to 16 mA, V_{CM} = 1500 V (Note 13)	35	50	–	kV/μs	29
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output LOW	T_A = 25°C, V_{DD} = 30 V, V_F = 0 V, V_{CM} = 1500 V (Note 14)	35	50	–	kV/μs	29

9. Propagation delay t_{PHL} is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal.
10. Propagation delay t_{PLH} is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
11. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
12. The difference between t_{PHL} and t_{PLH} between any two FOD8384 parts under the same operating conditions, with equal loads.
13. Common mode transient immunity at output high is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, V_{CM}, to ensure that the output remains high (i.e., V_O > 15.0 V).
14. Common mode transient immunity at output low is the maximum tolerable positive dVcm/dt on the leading edge of the common pulse signal, V_{CM}, to ensure that the output remains low (i.e., V_O < 1.0 V).

TYPICAL PERFORMANCE CHARACTERISTICS

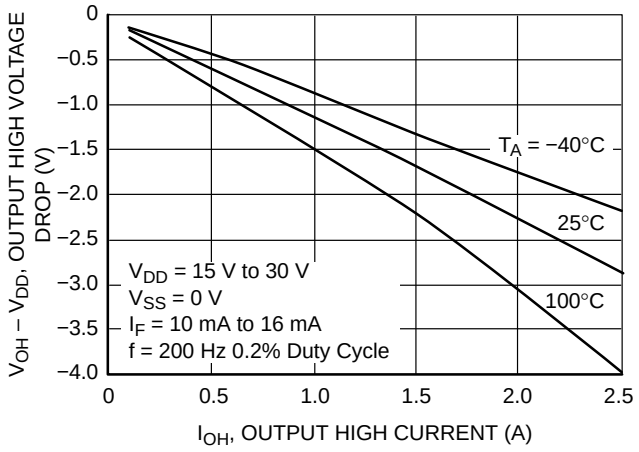


Figure 2. Output High Voltage Drop vs. Output High Current

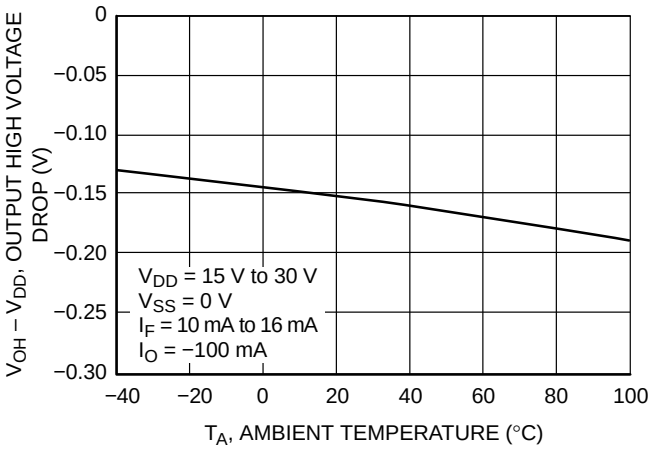


Figure 3. Output High Voltage Drop vs. Ambient Temperature

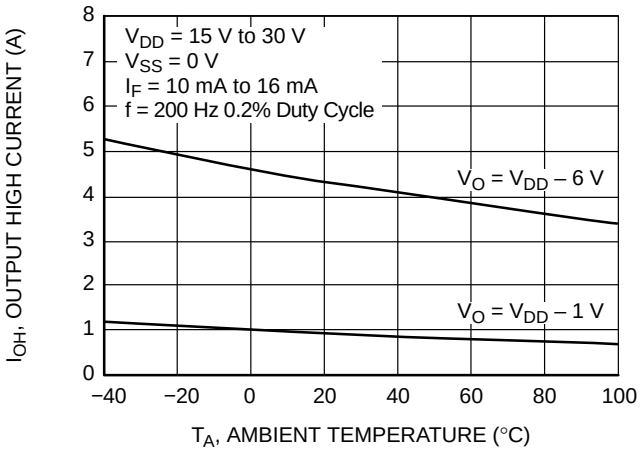


Figure 4. Output High Current vs. Ambient Temperature

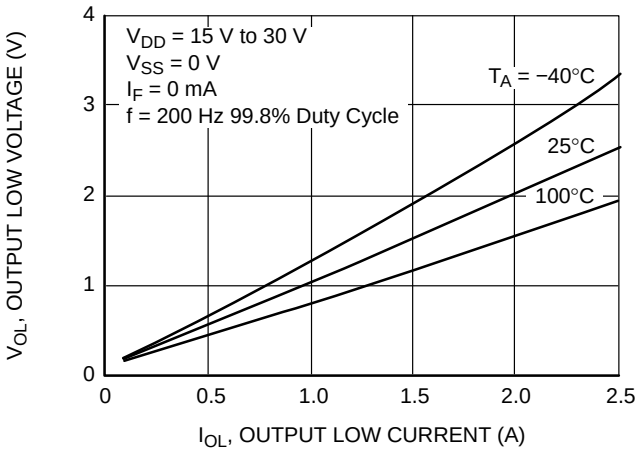


Figure 5. Output Low Voltage vs. Output Low Current

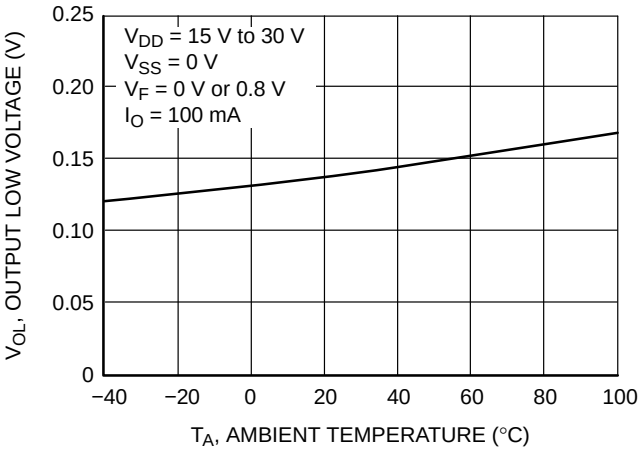


Figure 6. Output Low Voltage vs. Ambient Temperature

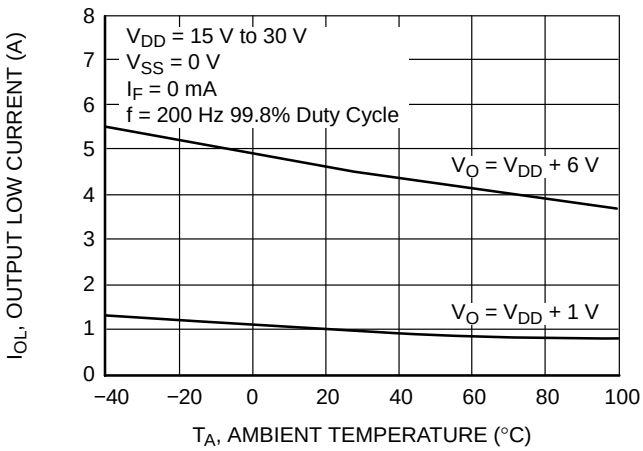


Figure 7. Output Low Current vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

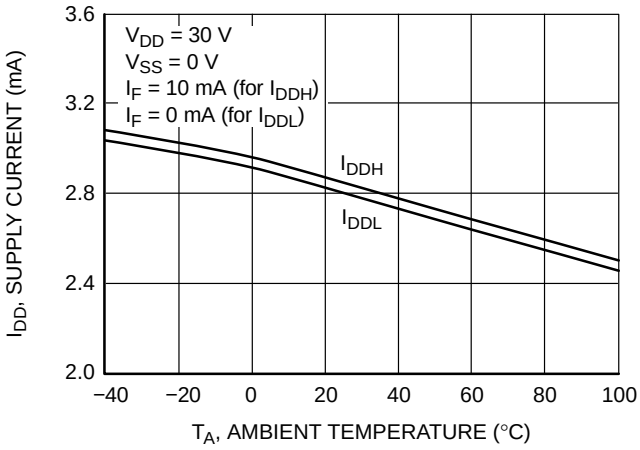


Figure 8. Supply Current vs. Ambient Temperature

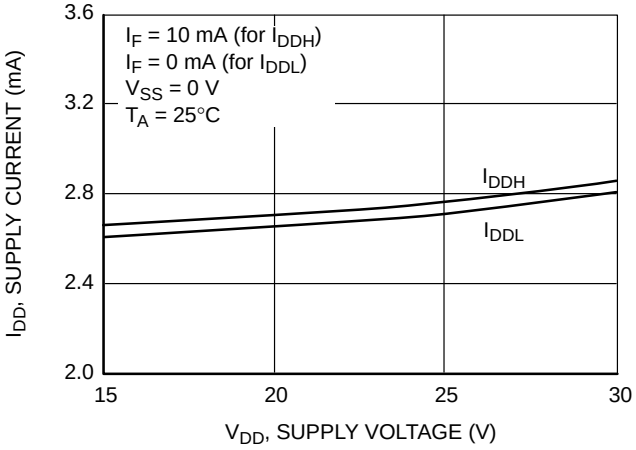


Figure 9. Supply Current vs. Supply Voltage

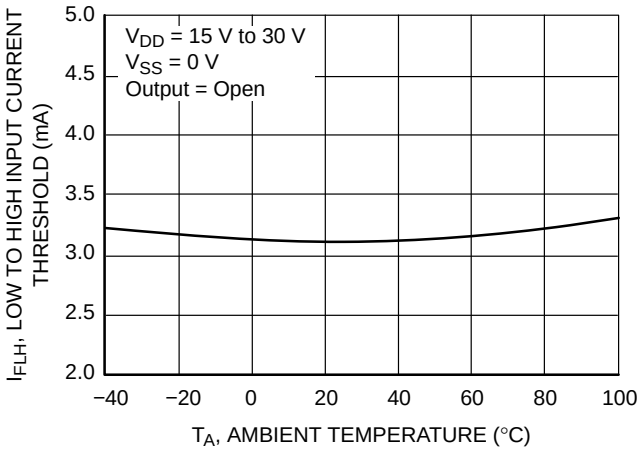


Figure 10. Low−to−High Input Current Threshold vs. Ambient Temperature

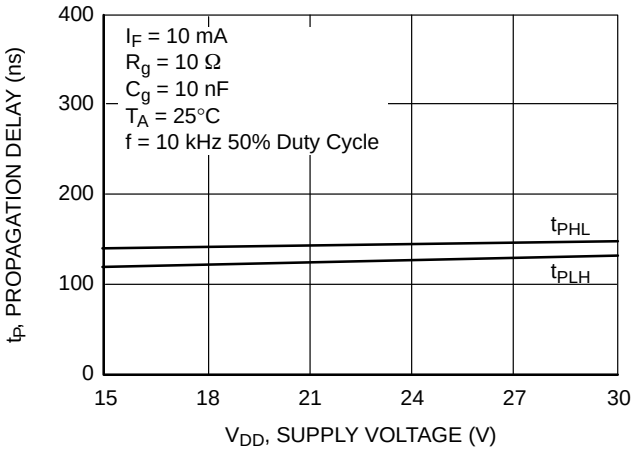


Figure 11. Propagation Delay vs. Supply Voltage

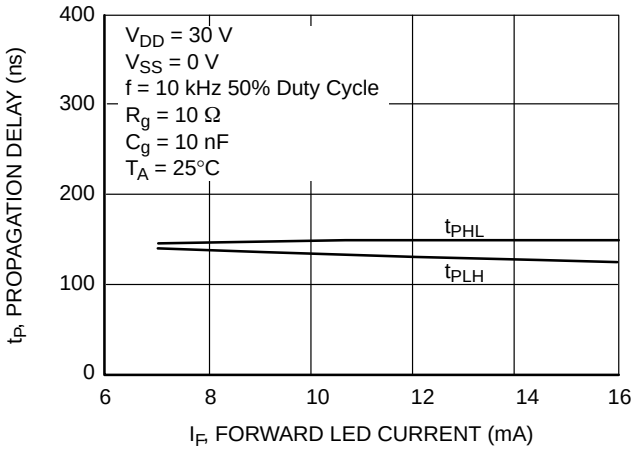


Figure 12. Propagation Delay vs. LED Forward Current

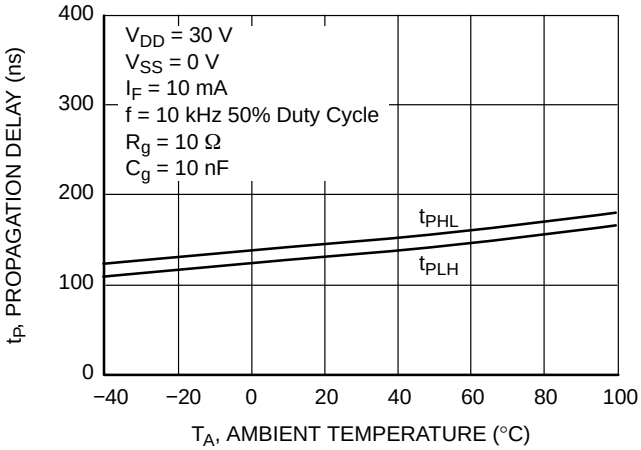


Figure 13. Propagation Delay vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

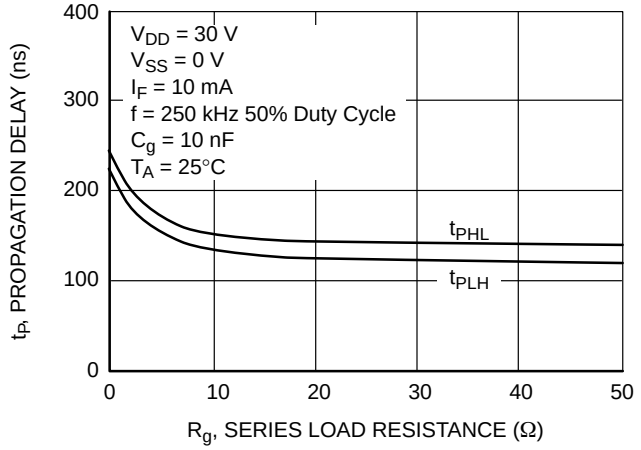


Figure 14. Propagation Delay vs. Series Load Resistance

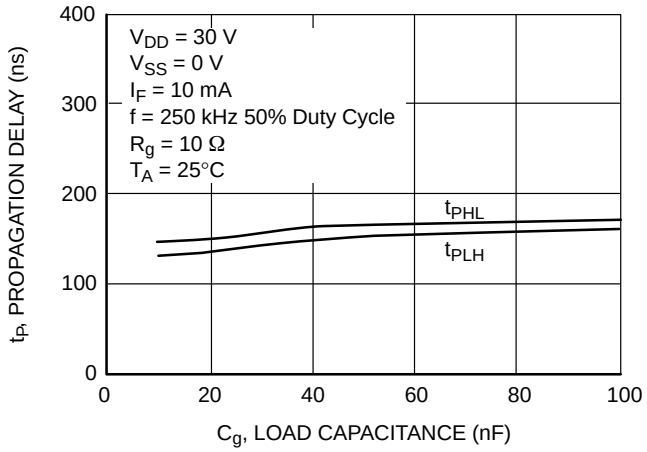


Figure 15. Propagation Delay vs. Load Capacitance

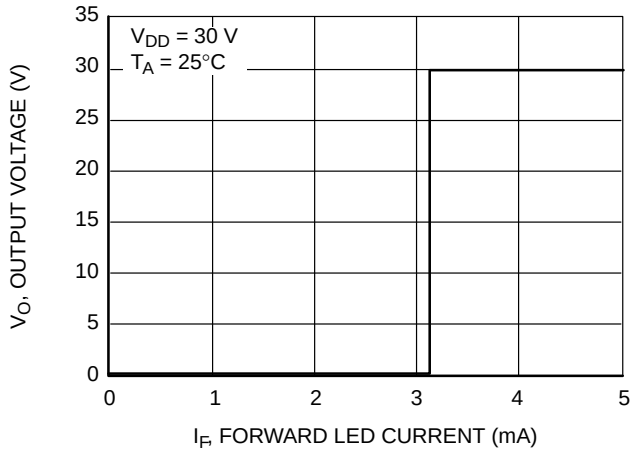


Figure 16. Transfer Characteristics

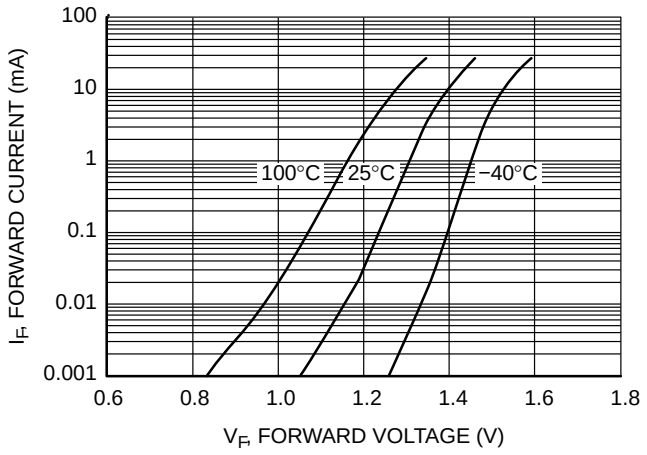


Figure 17. Input Forward Current vs. Forward Voltage

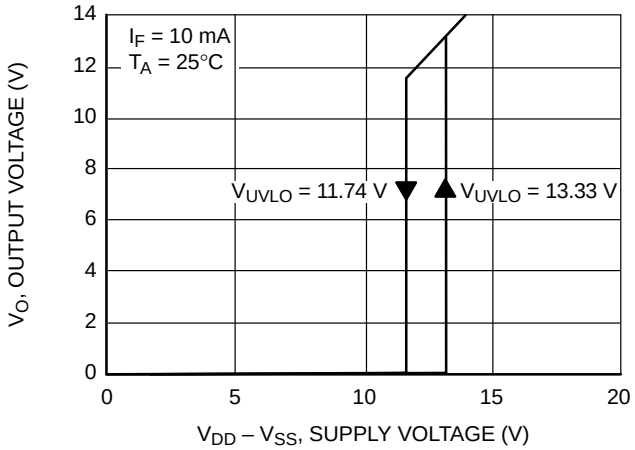
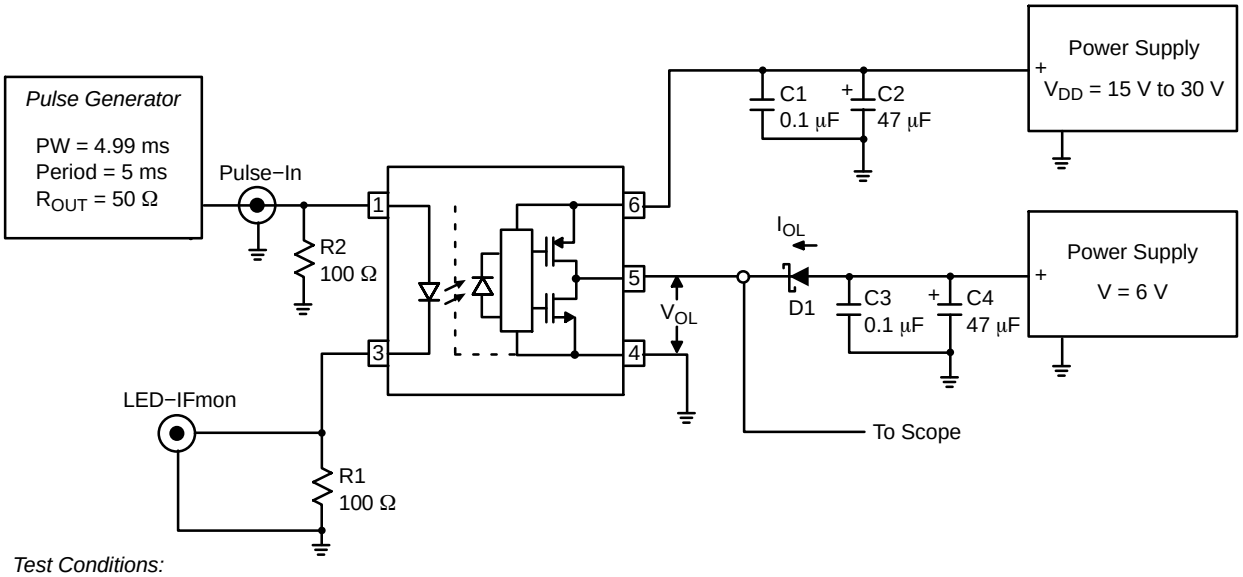


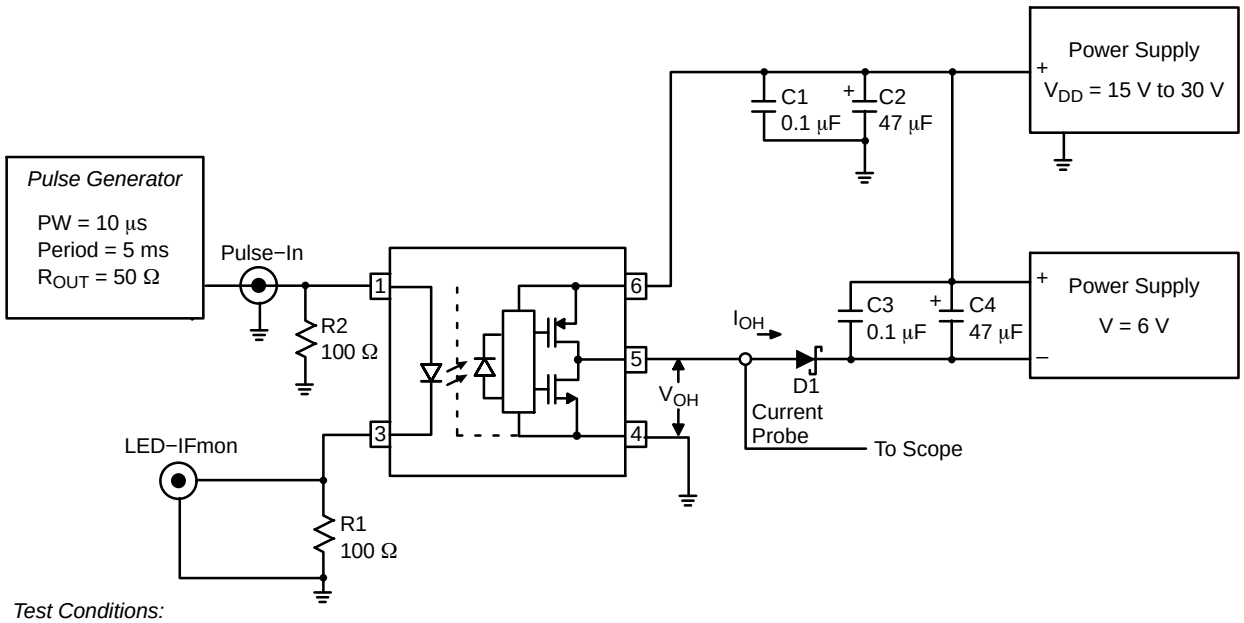
Figure 18. Under−Voltage Lockout

TEST CIRCUIT



Test Conditions:
Frequency = 200 Hz
Duty Cycle = 99.8%
V_{DD} = 15 V to 30 V
V_{SS} = 0 V
I_F = 0 mA

Figure 19. I_{OL} Test Circuit



Test Conditions:
Frequency = 200 Hz
Duty Cycle = 0.2%
V_{DD} = 15 V to 30 V
V_{SS} = 0 V
I_F = 10 mA to 16 mA

Figure 20. I_{OH} Test Circuit

TEST CIRCUIT (CONTINUED)

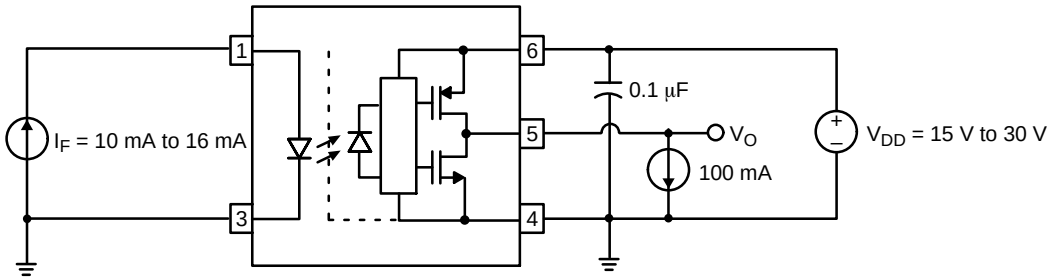


Figure 21. V_{OH} Test Circuit

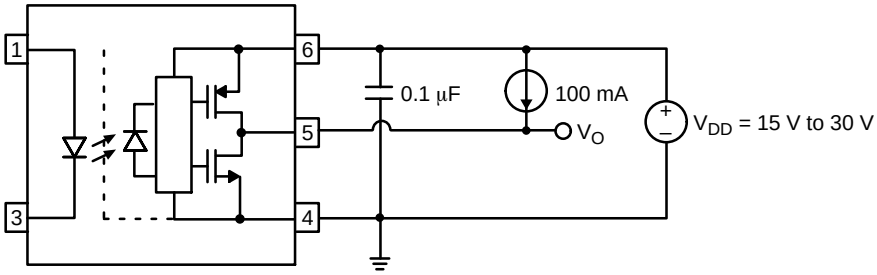


Figure 22. V_{OL} Test Circuit

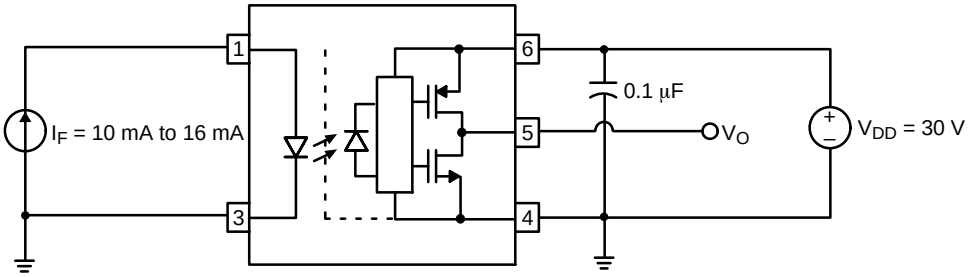


Figure 23. I_{DDH} Test Circuit

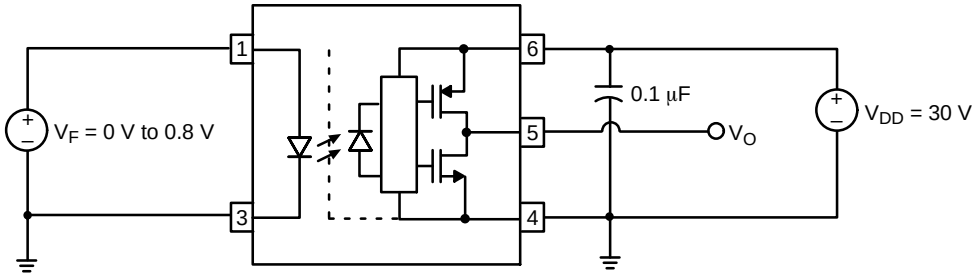


Figure 24. I_{DDL} Test Circuit

TEST CIRCUIT (CONTINUED)

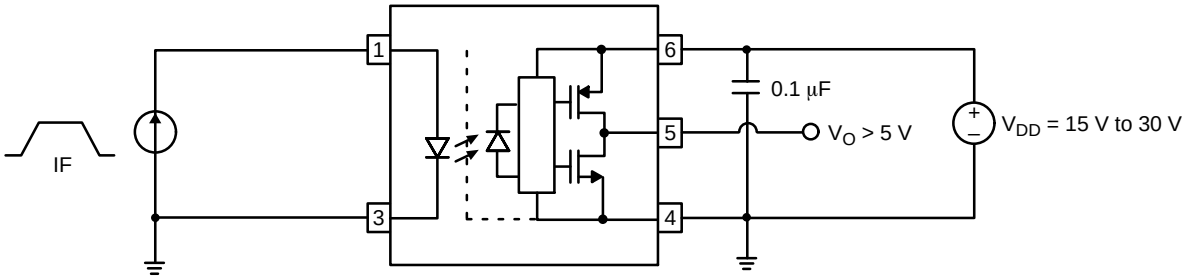


Figure 25. I_{FLH} Test Circuit

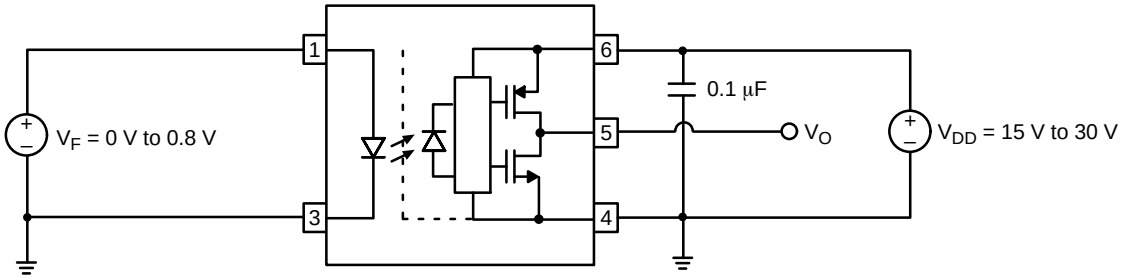


Figure 26. V_{FHL} Test Circuit

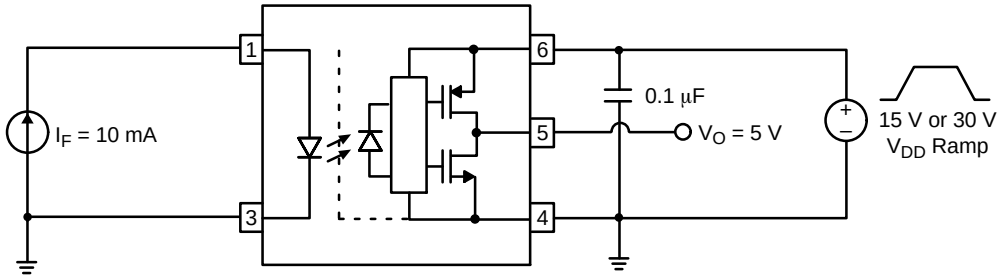


Figure 27. UVLO Test Circuit

TEST CIRCUIT (CONTINUED)

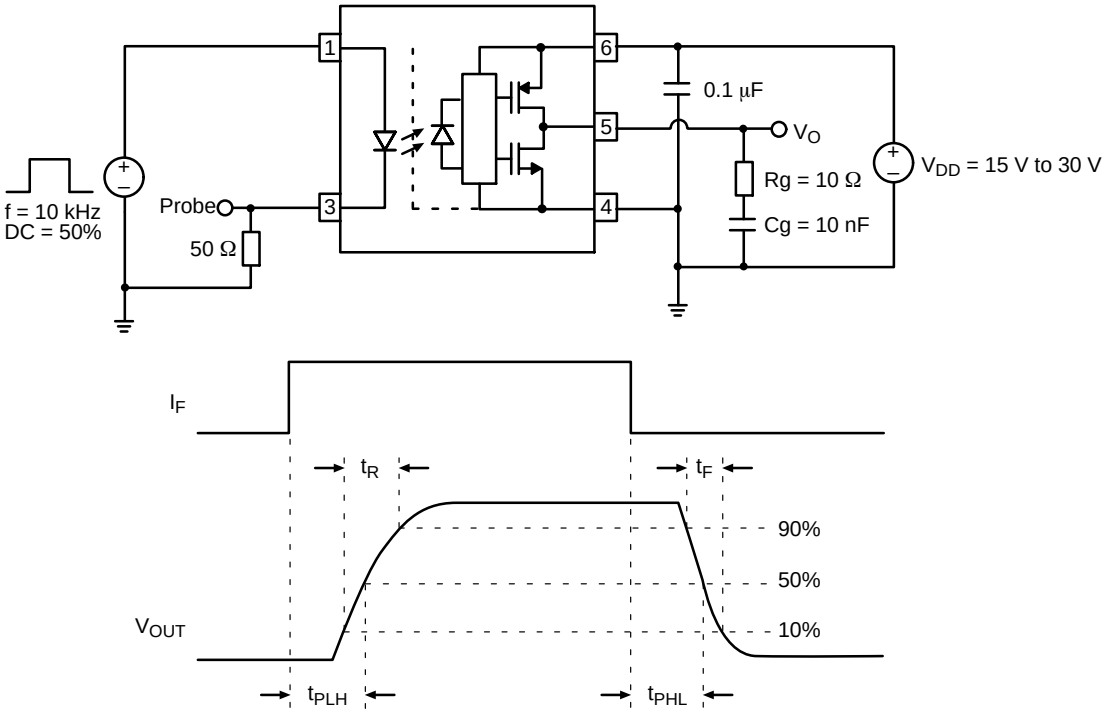


Figure 28. t_{PHL}, t_{PLH}, t_R, and t_F Test Circuit and Waveforms

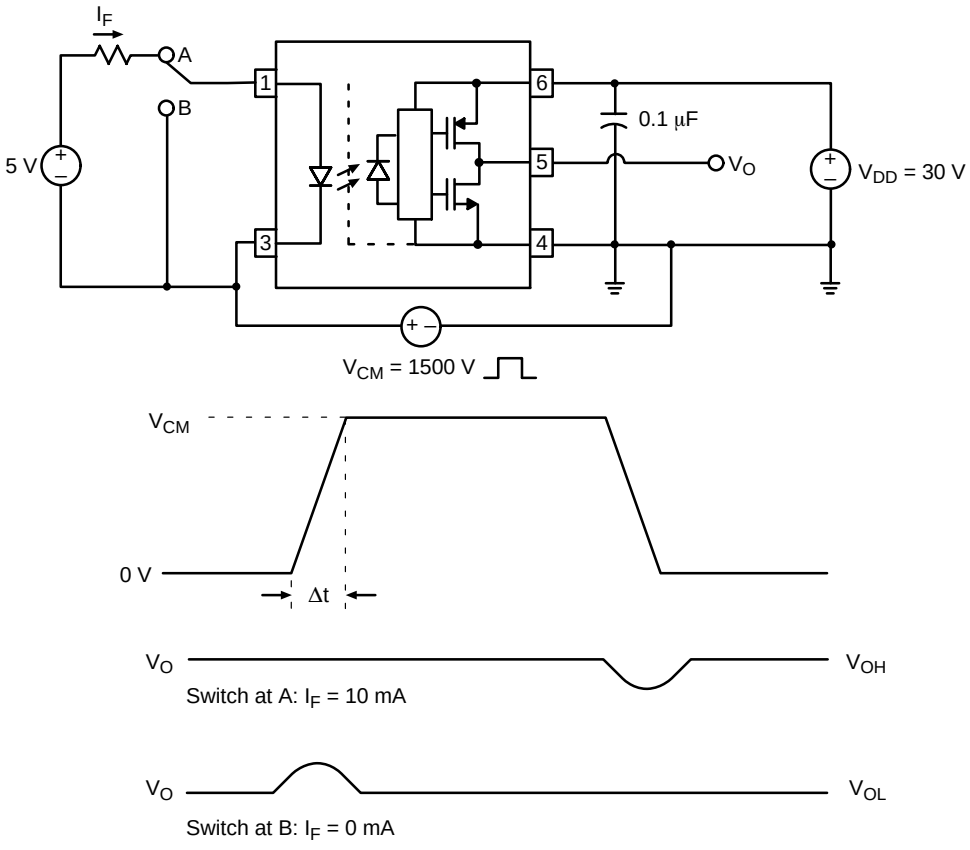


Figure 29. CMR Test Circuit and Waveforms

REFLOW PROFILE

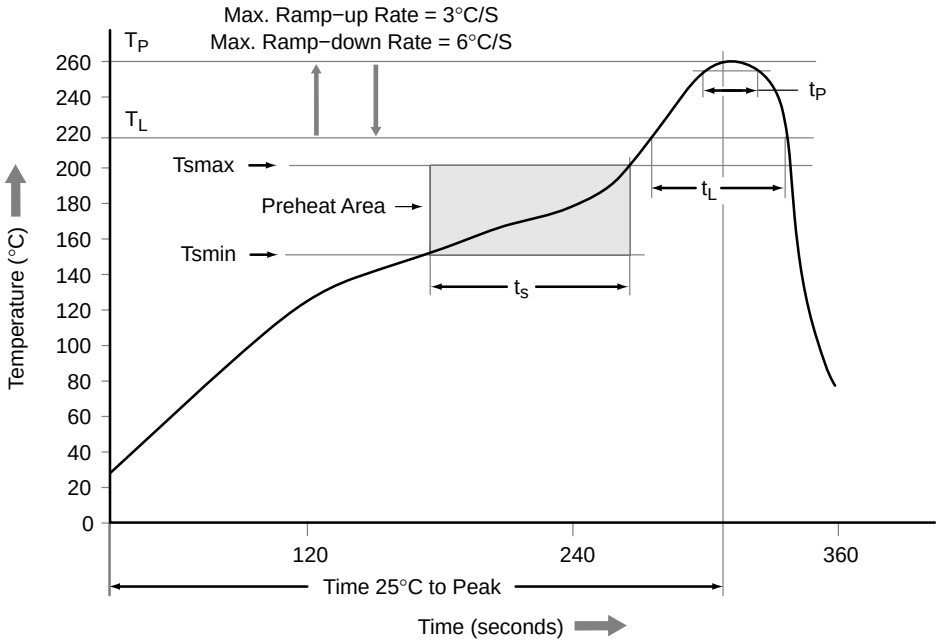


Figure 30. Reflow Profile

Profile Feature	Pb−Free Assembly Profile
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_S) from (T_{smin} to T_{smax})	60 s to 120 s
Ramp−up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 s to 150 s
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 55°C of 260°C	30 s
Ramp−Down Rate (T_P to T_L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

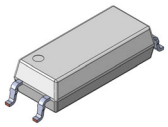
ORDERING INFORMATION

Part Number	Package	Shipping†
FOD8384	SOIC6 W LESS PIN 2, Wide Body SOP 5−Pin (Pb−Free)	100 Units / Tube
FOD8384R2	SOIC6 W LESS PIN 2, Wide Body SOP 5−Pin (Pb−Free)	1,000 Units / Tape & Reel
FOD8384V	SOIC6 W LESS PIN 2, Wide Body SOP 5−Pin, DIN EN/IEC60747−5−5 Option (Pb−Free)	100 Units / Tube
FOD8384R2V	SOIC6 W LESS PIN 2, Wide Body SOP 5−Pin, DIN EN/ IEC60747−5−5 Option (Pb−Free)	1,000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

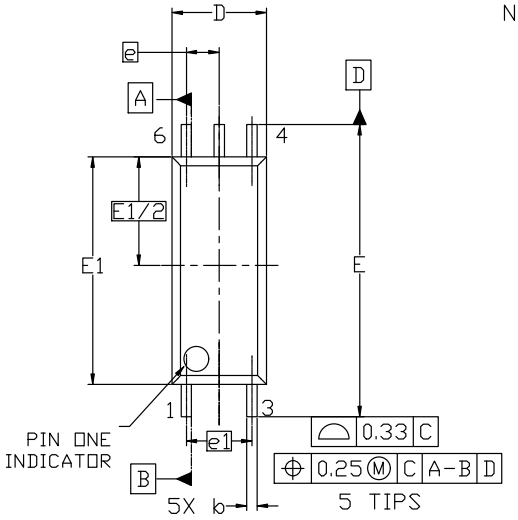
15. All packages are lead free per JEDEC: J−STD−020B standard.

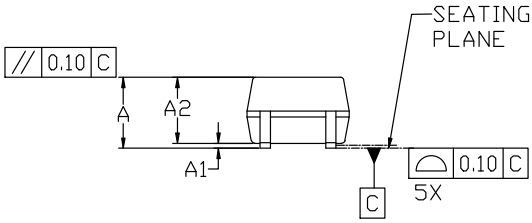
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

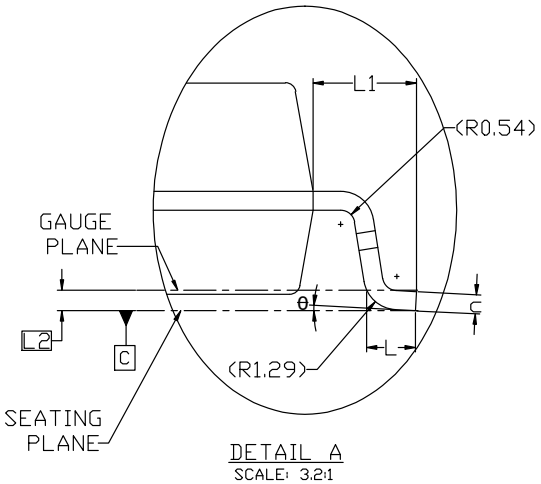


SOIC5 (6) 3.65x8.80x2.55, 1.27P
CASE 752AG
ISSUE B

DATE 24 JUL 2023

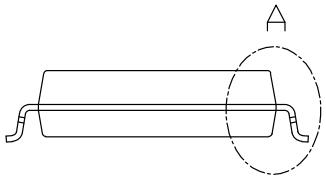




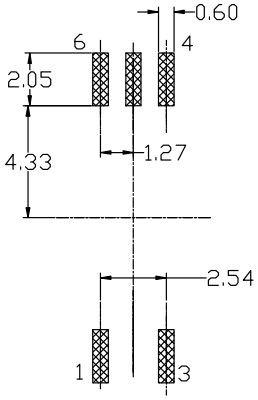


NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE DOES NOT CONFORM TO ANY STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
D) DRAWING CONFORMS TO ASME Y14.5M-1994



DIM	MILLIMETER		
	MIN.	NOM.	MAX.
A	--	--	2.95
A1	0.10	0.20	0.30
A2	2.45	2.55	2.65
b	0.31	0.41	0.51
c	0.19	0.22	0.25
D	3.55	3.65	3.75
E	11.20	11.30	11.40
E1	8.70	8.80	8.90
E1/2	4.20 BSC		
e	1.27 BSC		
e1	2.54 BSC		
L	0.44	0.59	0.74
L1	1.15	1.25	1.35
L2	0.25 BSC		
θ	0°	--	8°



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**SOIC5 (6) 3.65x8.80x2.55, 1.27P**		**PAGE 1 OF 1**

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