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ON Semiconductor®

FDY100PZ

Single P-Channel (– 2.5V) Specified PowerTrench® MOSFET

General Description

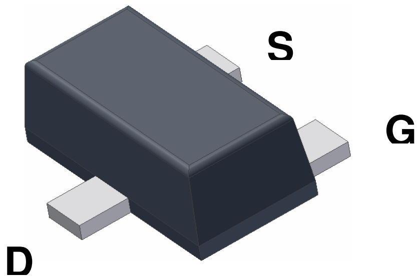
This Single P-Channel MOSFET has been designed using ON Semiconductor's advanced Power Trench process to optimize the $R_{DS(ON)}$ @ V_{GS} = – 2.5v.

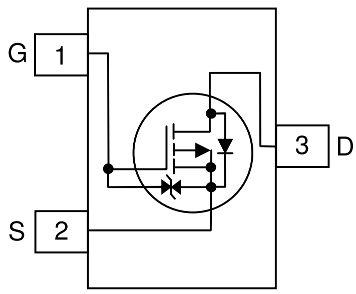
Applications

- Li-Ion Battery Pack

Features

- – 350 mA, – 20 V $R_{DS(ON)}$ = 1.2 Ω @ V_{GS} = – 4.5 V
  $R_{DS(ON)}$ = 1.6 Ω @ V_{GS} = – 2.5 V
- ESD protection diode (note 3)
- RoHS Compliant





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		– 20	V
V_{GSS}	Gate-Source Voltage		± 8	V
I_D	Drain Current – Continuous	(Note 1a)	– 350	mA
	– Pulsed		– 1000	
P_D	Power Dissipation (Steady State)	(Note 1a)	625	mW
		(Note 1b)	446	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	200	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
A	FDY100PZ	7''	8mm	3000 units

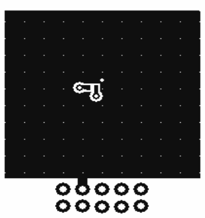
Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

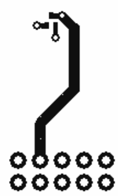
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250\ \mu A$	– 20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu A$, Referenced to 25°C		15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16$ V, $V_{GS} = 0$ V			– 3	µA
I_{GSS}	Gate–Body Leakage,	$V_{GS} = \pm 8$ V, $V_{DS} = 0$ V			± 10	µA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	– 0.65	–1.0	– 1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu A$, Referenced to 25°C		–3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5$ V, $I_D = -350$ mA $V_{GS} = -2.5$ V, $I_D = -300$ mA $V_{GS} = -1.8$ V, $I_D = -150$ mA $V_{GS} = -4.5$ V, $I_D = -350$ mA, $T_J = 125°C$		0.5 0.8 1.3 0.7	1.2 1.6 2.7 1.6	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5$ V, $I_D = -350$ mA		1		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10$ V, $V_{GS} = 0$ V, f = 1.0 MHz		100		pF
C_{oss}	Output Capacitance			30		pF
C_{rss}	Reverse Transfer Capacitance			15		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10$ V, $I_D = -0.5$ A, $V_{GS} = -4.5$ V, $R_{GEN} = 6\ \Omega$		6	12	ns
t_r	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			8	16	ns
t_f	Turn–Off Fall Time			1	2	ns
Q_g	Total Gate Charge	$V_{DS} = -10$ V, $I_D = -350$ mA, $V_{GS} = -4.5$ V		1.0	1.4	nC
Q_{gs}	Gate–Source Charge			0.2		nC
Q_{gd}	Gate–Drain Charge			0.3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -150$ mA (Note 2)		–0.8	– 1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -350$ mA, $dI_F/dt = 100$ A/µs		11		ns
Q_{rr}	Diode Reverse Recovery Charge			2		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 200°C/W when mounted on a 1in² pad of 2 oz copper



b) 280°C/W when mounted on a minimum pad of 2 oz copper
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection againts ESD. No gate overvoltage rating is implied.

Typical Characteristics

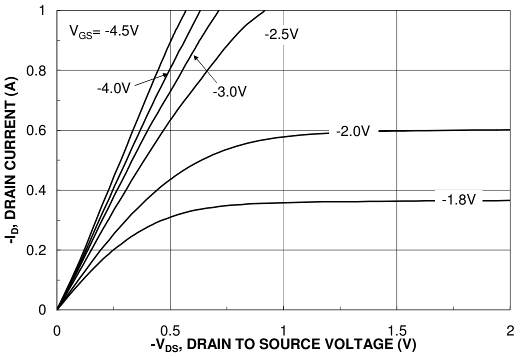


Figure 1. On-Region Characteristics.

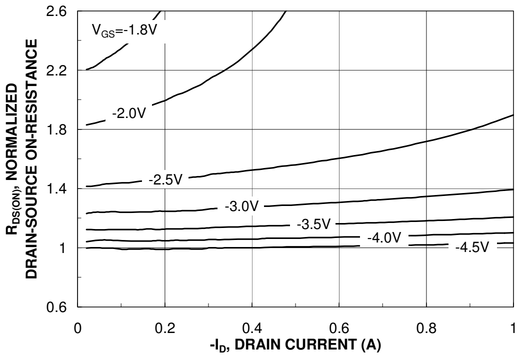


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

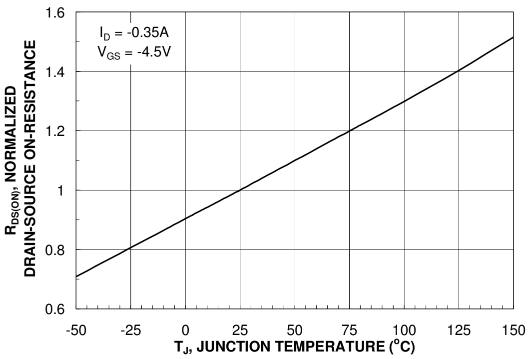


Figure 3. On-Resistance Variation with Temperature.

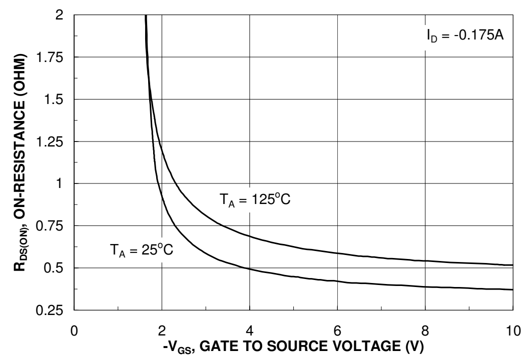


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

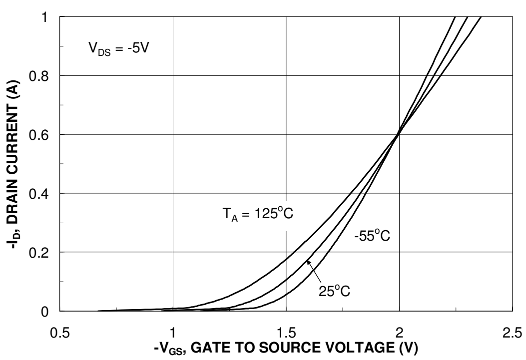


Figure 5. Transfer Characteristics.

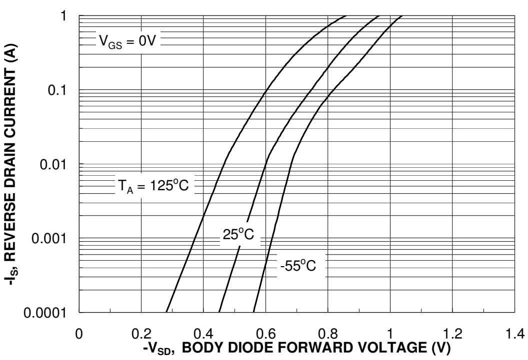


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

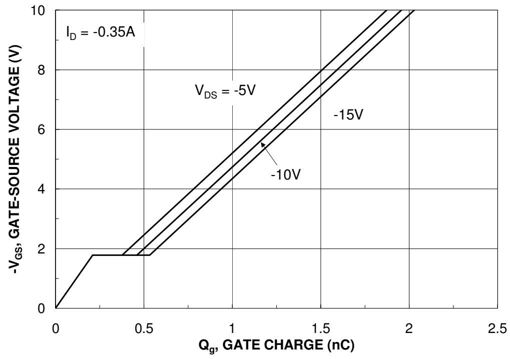


Figure 7. Gate Charge Characteristics.

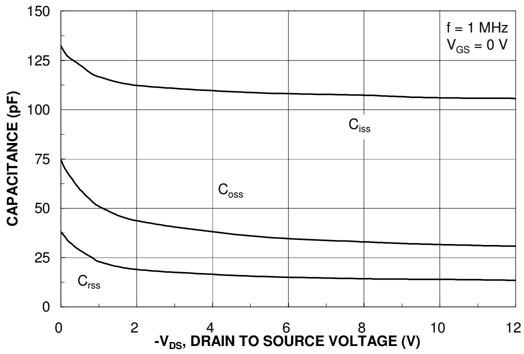


Figure 8. Capacitance Characteristics.

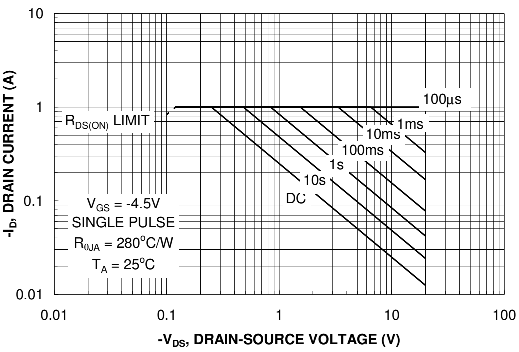


Figure 9. Maximum Safe Operating Area.

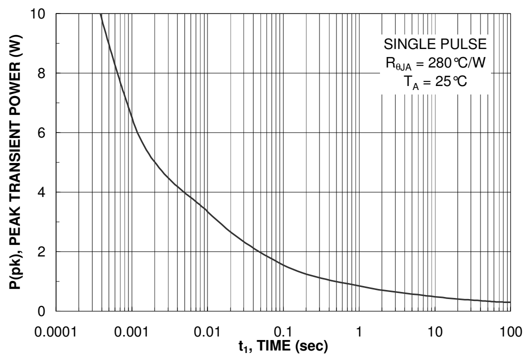


Figure 10. Single Pulse Maximum Power Dissipation.

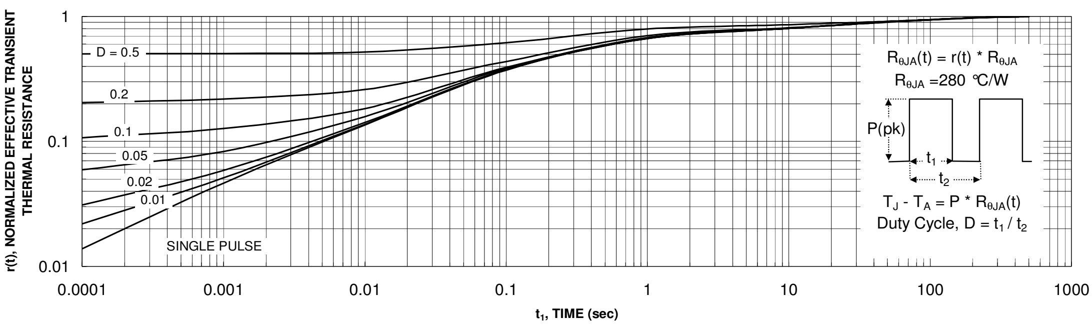
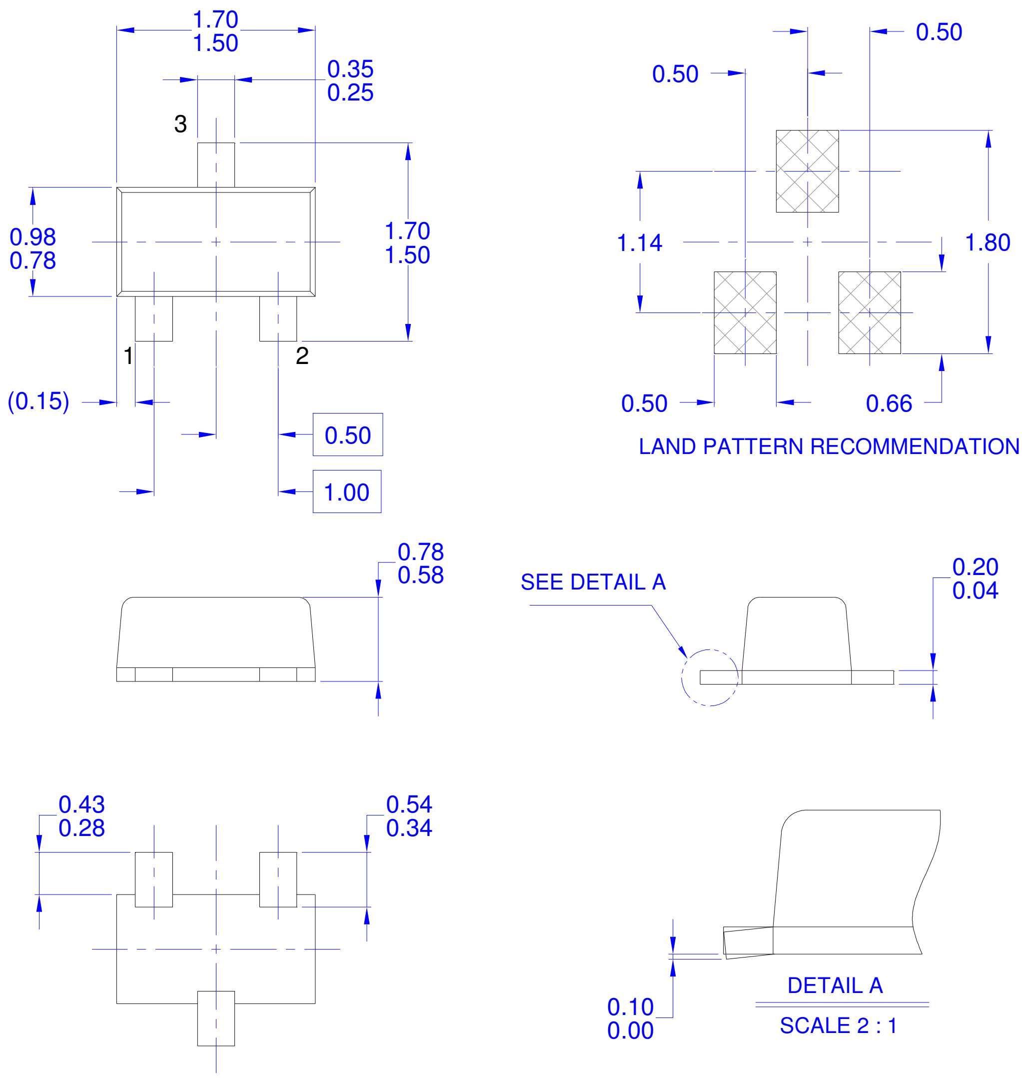


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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