

MOSFET – N-Channel, POWERTRENCH®

100 V, 3.3 A, 100 mΩ

FDT86113LZ

General Description

This N-Channel logic Level MOSFET is produced using onsemi's advanced POWERTRENCH process that has been special tailored to minimize the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

Features

- Max $r_{DS(on)}$ = 100 mΩ at $V_{GS} = 10$ V, $I_D = 3.3$ A
- Max $r_{DS(on)}$ = 145 mΩ at $V_{GS} = 4.5$ V, $I_D = 2.7$ A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- HBM ESD Protection Level > 3 kV Typical (Note 4)
- 100% UIL Tested
- This Device is Pb-Free and Halide Free

Applications

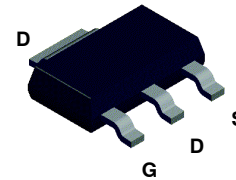
- DC – DC Switch

Specifications

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

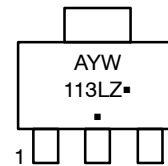
Symbol	Parameter	Ratings	Unit	
V_{DS}	Drain to Source Voltage	100	V	
V_{GS}	Gate to Source Voltage	±20	V	
I_D	Drain Current	-Continuous	3.3	A
		-Pulsed	12	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	9	mJ	
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	2.2	W
		$T_A = 25^\circ\text{C}$ (Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



SOT-223
CASE 318H

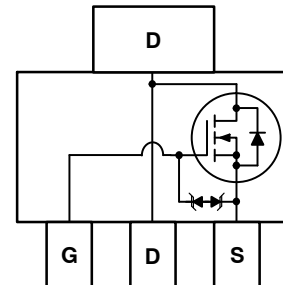
MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- 113LZ = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDT86113LZ

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C		71		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.0	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 3.3 \text{ A}$		75	100	m Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 2.7 \text{ A}$		95	145	
		$V_{GS} = 10 \text{ V}, I_D = 3.3 \text{ A}, T_J = 125^\circ\text{C}$		140	189	
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 3.3 \text{ A}$		8		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		234	315	pF
C_{oss}	Output Capacitance			46	65	pF
C_{rss}	Reverse Transfer Capacitance			3.1	5	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 3.3 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		3.8	10	ns
t_r	Rise Time			1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			10	20	ns
t_f	Fall Time			1.5	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}, V_{DD} = 50 \text{ V}, I_D = 3.3 \text{ A}$		4.1	6.8	nC
		$V_{GS} = 0 \text{ V to } 5 \text{ V}, V_{DD} = 50 \text{ V}, I_D = 3.3 \text{ A}$		2.3	3.9	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 50 \text{ V}, I_D = 3.3 \text{ A}$		0.68		nC
Q_{gd}	Gate to Drain "Miller" Charge			0.85		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

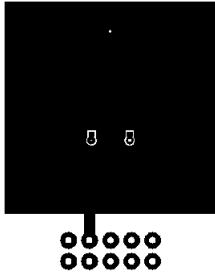
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 3.3 \text{ A}$ (Note 2)		0.86	1.3	V
		$V_{GS} = 0 \text{ V}, I_S = 1.0 \text{ A}$ (Note 2)		0.77	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 3.3 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		31	49	ns
Q_{rr}	Reverse Recovery Charge			21	34	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.
 $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 55°C/W when mounted on a 1 in² pad of 2 oz copper



b. 118°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
3. Starting $T_J = 25^\circ\text{C}$, $L = 0.3$ mH, $I_{AS} = 8$ A, $V_{DD} = 90$ V, $V_{GS} = 10$ V.
4. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

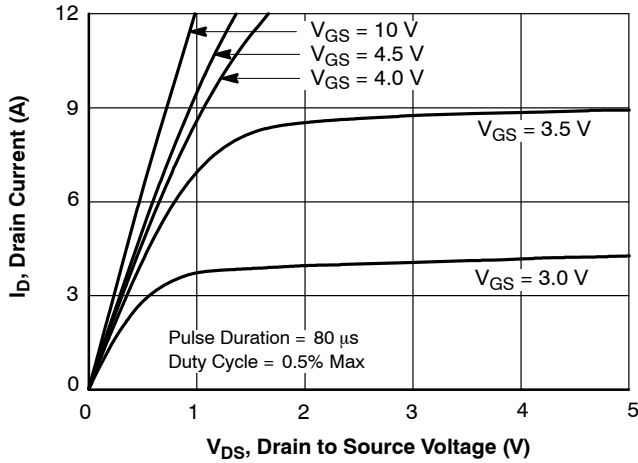


Figure 1. On Region Characteristics

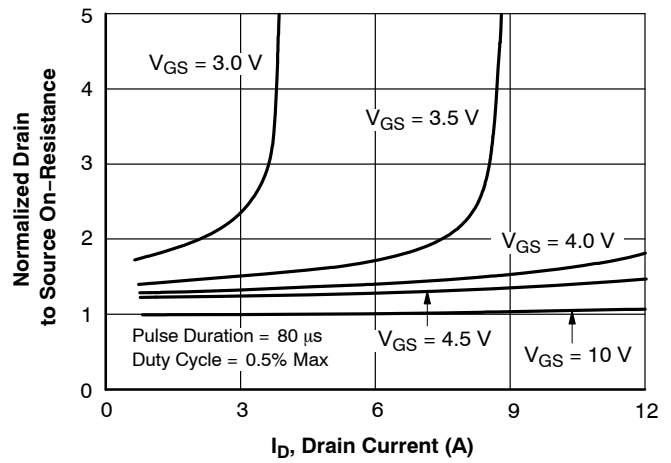


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

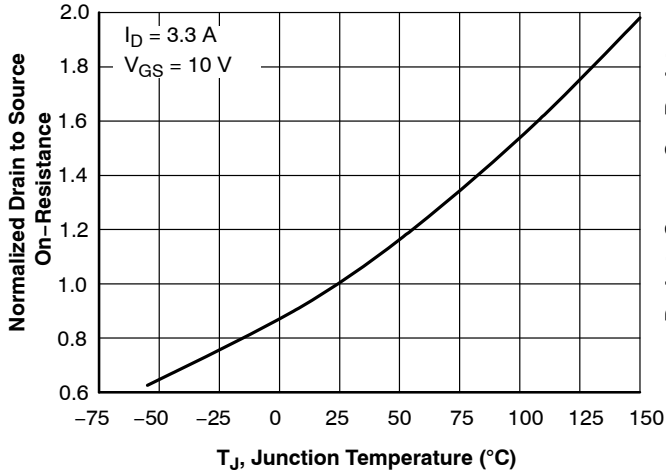


Figure 3. Normalized On Resistance vs. Junction Temperature

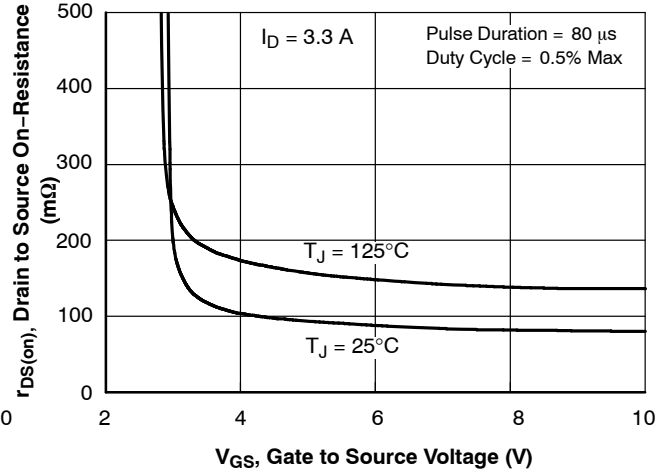


Figure 4. On-Resistance vs. Gate to Source Voltage

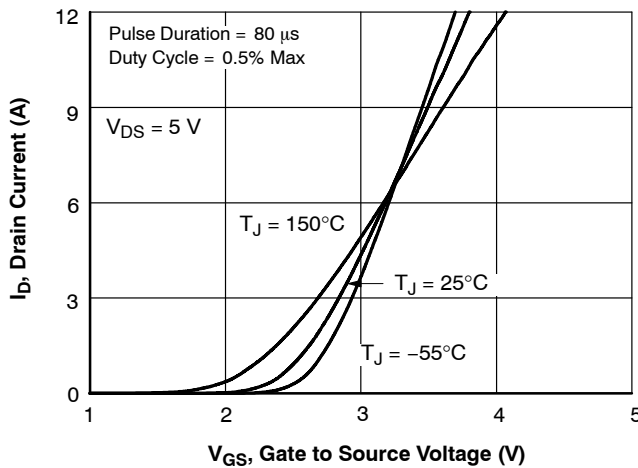


Figure 5. Transfer Characteristics

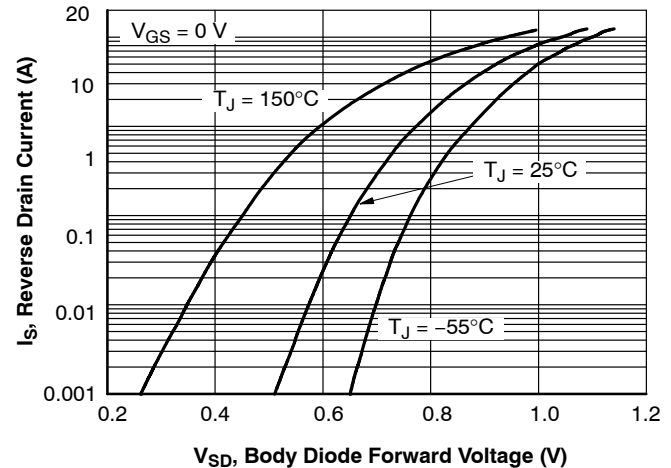


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

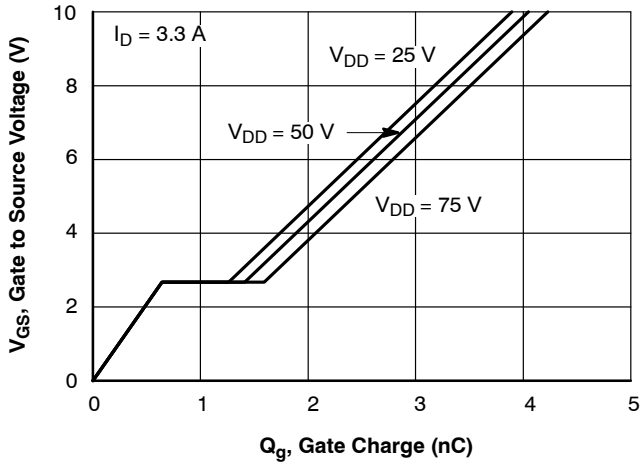


Figure 7. Gate Charge Characteristics

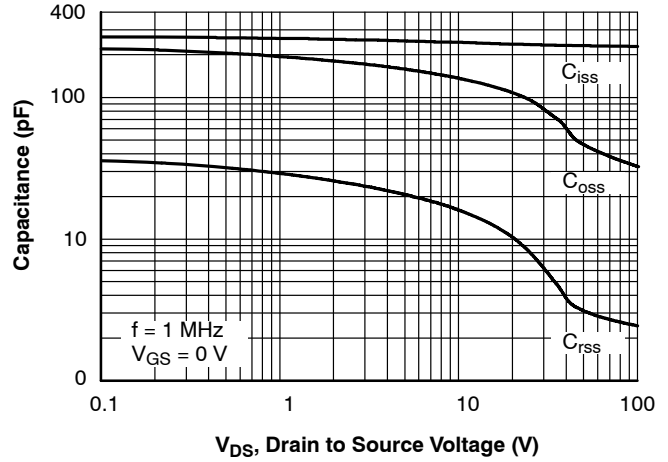


Figure 8. Capacitance vs. Drain to Source Voltage

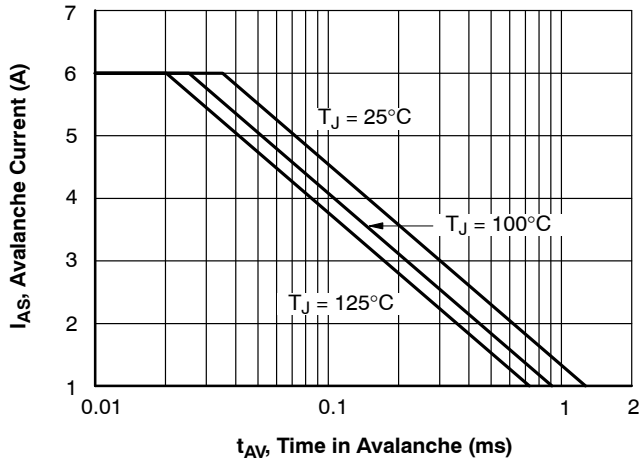


Figure 9. Unclamped Inductive Switching Capability

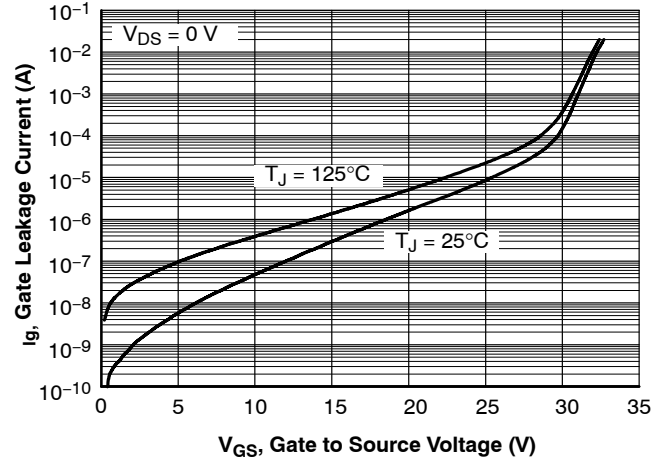


Figure 10. Gate Leakage Current vs Gate to Source Voltage

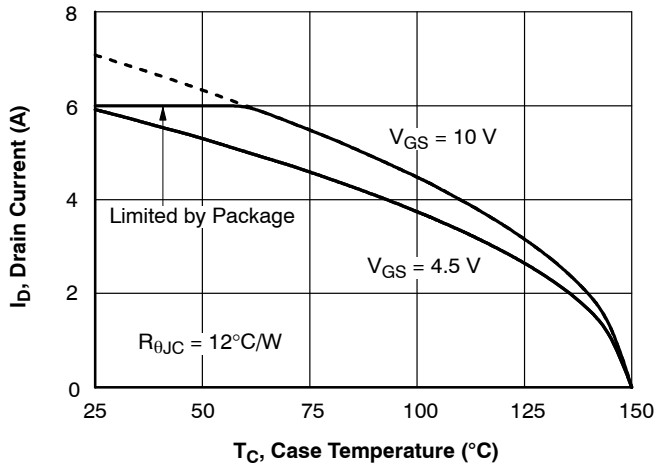


Figure 11. Maximum Continuous Drain Current vs Case Temperature

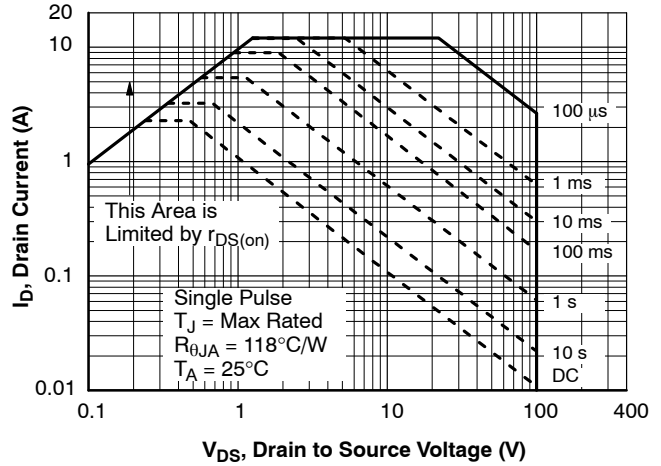


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

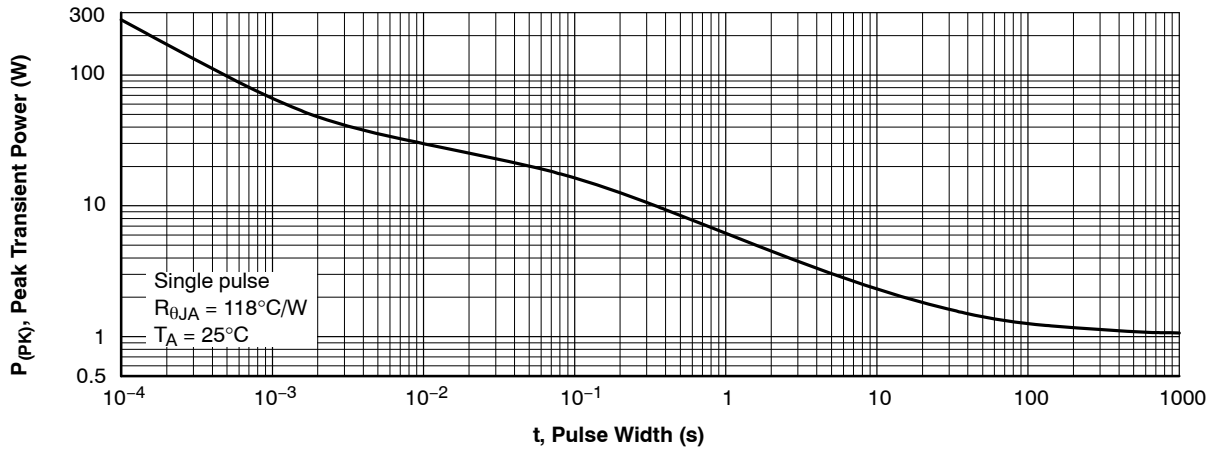


Figure 13. Single Pulse Maximum Power Dissipation

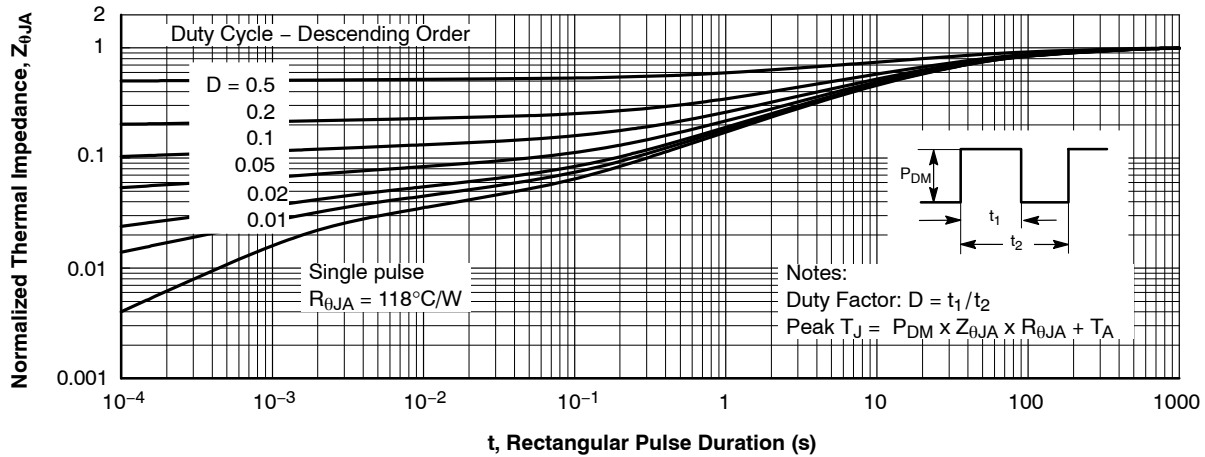


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDT86113LZ	113LZ	SOT-223 (Pb-Free)	4000 units / Tape & Reel

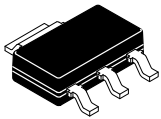
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

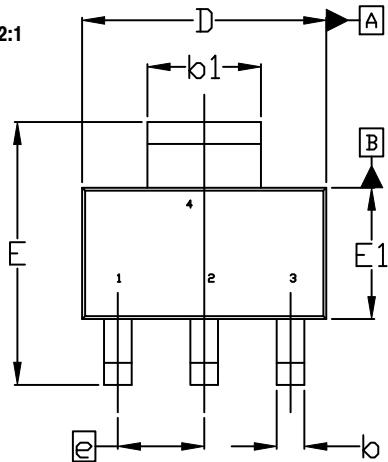
ON Semiconductor®



SOT-223
CASE 318H
ISSUE B

DATE 13 MAY 2020

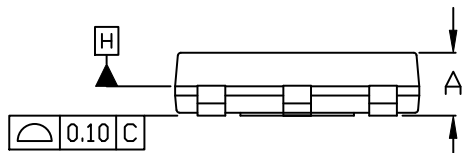
SCALE 2:1



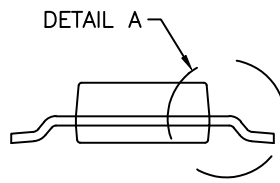
TOP VIEW

$\Phi 0.10 \text{ (M)}$ C A B

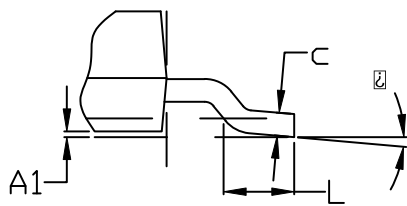
NOTE 7



SIDE VIEW



END VIEW

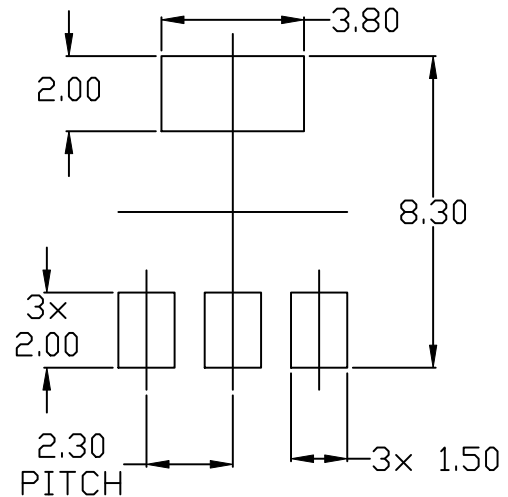


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

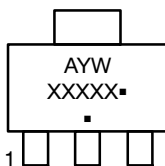
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
\square	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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