

# MOSFET - POWERTRENCH<sup>®</sup>, N-Channel, DUAL COOL<sup>®</sup> 56

60 V, 108 A, 2.3 mΩ

## FDMS86500DC

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH<sup>®</sup> process. Advancements in both silicon and DUAL COOL<sup>®</sup> package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

### Features

- DUAL COOL<sup>®</sup> Top Side Cooling DFN8 Package
- Max  $r_{DS(on)}$  = 2.3 mΩ at  $V_{GS} = 10$  V,  $I_D = 29$  A
- Max  $r_{DS(on)}$  = 3.3 mΩ at  $V_{GS} = 8$  V,  $I_D = 24$  A
- High Performance Technology for Extremely Low  $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

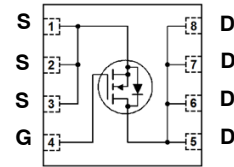
### Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation Vcore Low Side

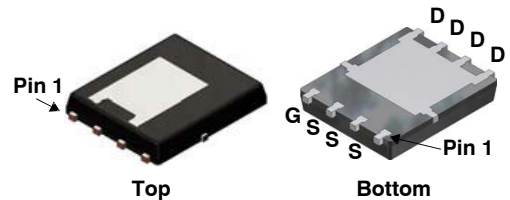
### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current: Continuous, $T_C = 25^\circ\text{C}$ Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed	108 29 200	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	294	mJ
$P_D$	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	125 3.2	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### ELECTRICAL CONNECTION

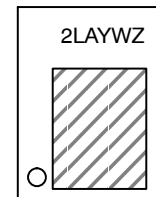


N-Channel MOSFET



DFN8, DUAL COOL<sup>®</sup>  
CASE 506EG

### MARKING DIAGRAM



- 2L = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDMS86500DC

**Table 1. THERMAL CHARACTERISTICS**

Symbol	Characteristic	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.8	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	

## ORDERING INFORMATION AND PACKAGE MARKING

Device	Top Marking	Package	Shipping <sup>†</sup>
FDMS86500DC	86500	DFN8	3000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	60			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		30		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}$ , $V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	2.5	3.7	4.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-12		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 29 \text{ A}$		1.9	2.3	m $\Omega$
		$V_{GS} = 8 \text{ V}$ , $I_D = 24 \text{ A}$		2.4	3.3	
		$V_{GS} = 10 \text{ V}$ , $I_D = 29 \text{ A}$ , $T_J = 125^\circ\text{C}$		3.0	3.7	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}$ , $I_D = 29 \text{ A}$		98		S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 30 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		5775	7680	pF
$C_{oss}$	Output Capacitance			1605	2680	pF
$C_{rss}$	Reverse Transfer Capacitance			48	95	pF
$R_g$	Gate Resistance			0.1	1	3

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}$ , $I_D = 29 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 6 \Omega$		35	56	ns
$t_r$	Rise Time			25	40	ns
$t_{d(off)}$	Turn-Off Delay Time			34	54	ns
$t_f$	Fall Time			8.2	17	ns

# FDMS86500DC

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS

$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}, V_{DD} = 30\text{ V}, I_D = 29\text{ A}$		76	107	nC
		$V_{GS} = 0\text{ V to }8\text{ V}, V_{DD} = 30\text{ V}, I_D = 29\text{ A}$		62	87	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 30\text{ V}, I_D = 29\text{ A}$		31		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			15		nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.7\text{ A}$ (Note 2)		0.71	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 29\text{ A}$ (Note 2)		0.79	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 29\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		59	95	ns
$Q_{rr}$	Reverse Recovery Charge			46	74	nC

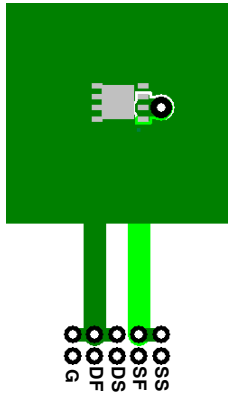
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## THERMAL CHARACTERISTICS

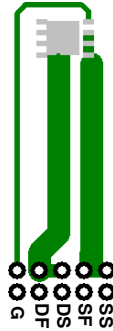
Symbol	Parameter	Max	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case (Top Source)	2.8	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1a)	38	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1b)	81	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1c)	27	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1d)	34	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1e)	16	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1f)	19	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1g)	26	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1h)	61	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1i)	16	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1j)	23	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1k)	11	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1l)	13	

### NOTES:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R<sub>θCA</sub> is determined by the user's board design.



a) 38°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 81°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

- Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
  - Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
  - Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
  - Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
  - 200FPM Airflow, No Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
  - 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
  - 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
  - 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
  - 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
  - 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
  - Starting T<sub>J</sub> = 25°C; N-ch: L = 0.3 mH, I<sub>AS</sub> = 46 A, V<sub>DD</sub> = 54 V, V<sub>GS</sub> = 10 V.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

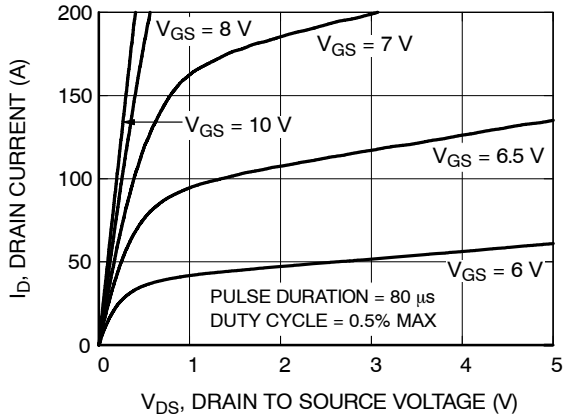


Figure 1. On-Region Characteristics

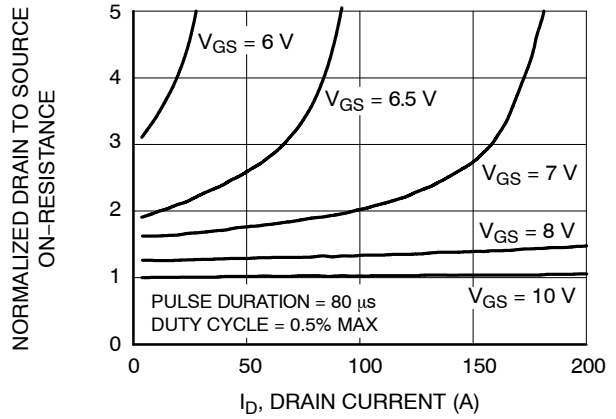


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

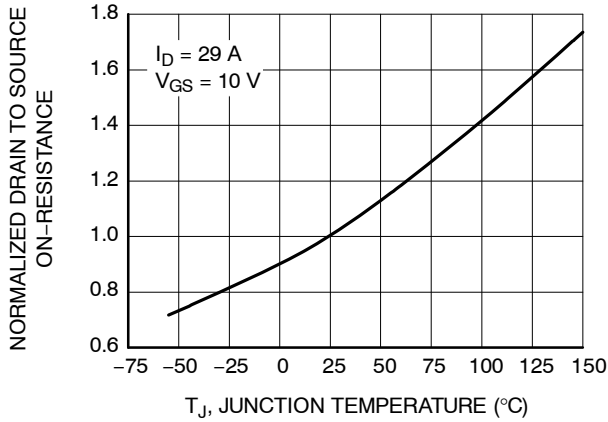


Figure 3. Normalized On-Resistance vs. Junction Temperature

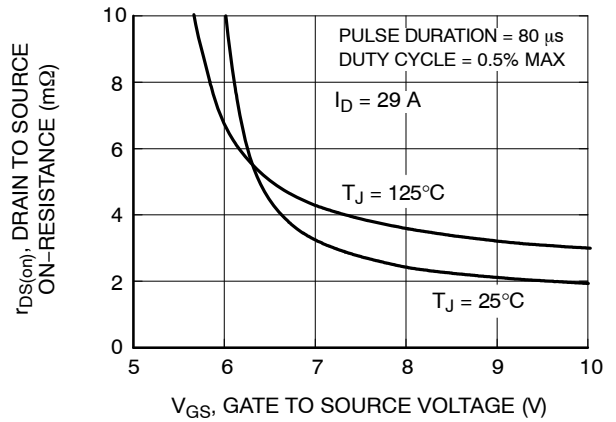


Figure 4. On-Resistance vs. Gate to Source Voltage

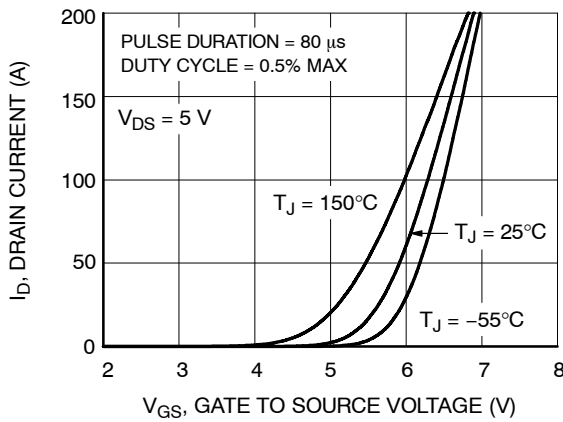


Figure 5. Transfer Characteristics

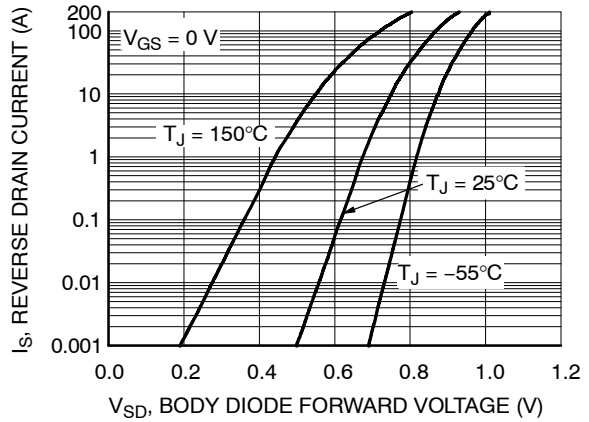
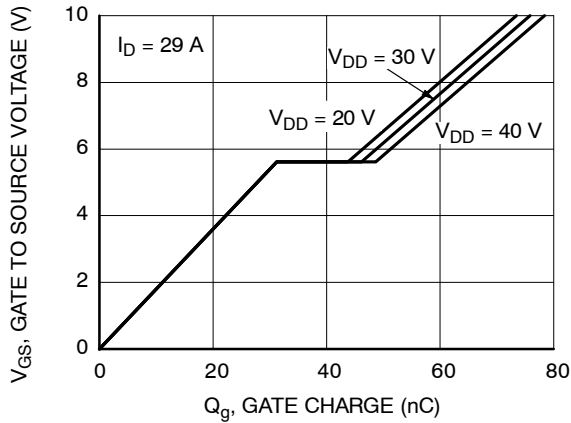


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

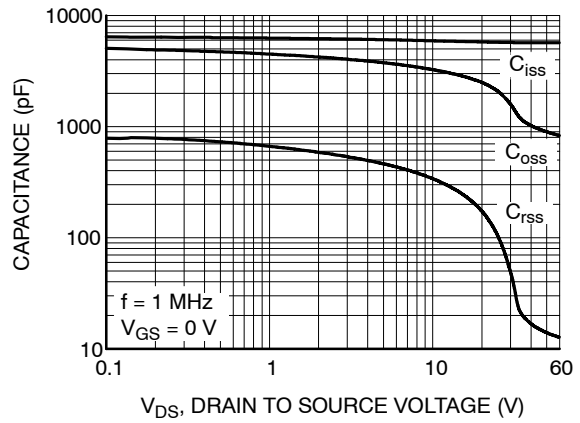
# FDMS86500DC

## TYPICAL CHARACTERISTICS (continued)

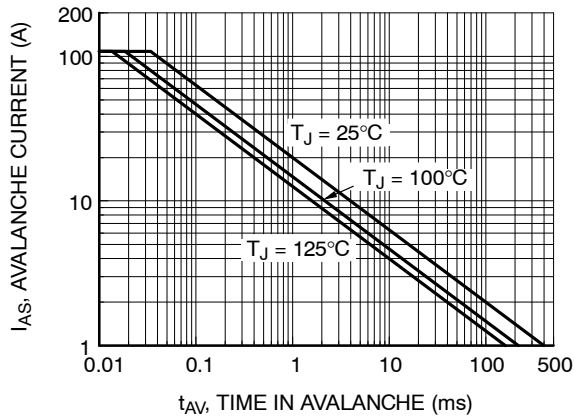
( $T_J = 25^\circ\text{C}$  unless otherwise noted)



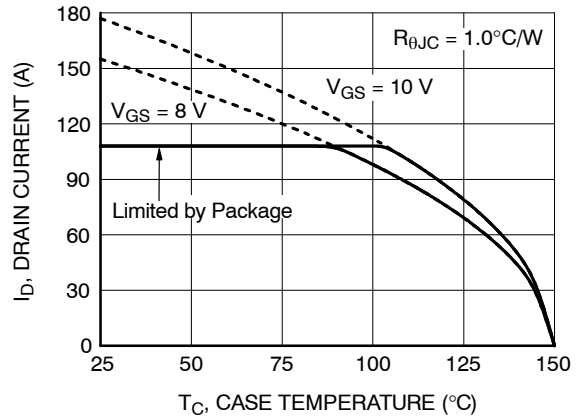
**Figure 7. Gate Charge Characteristics**



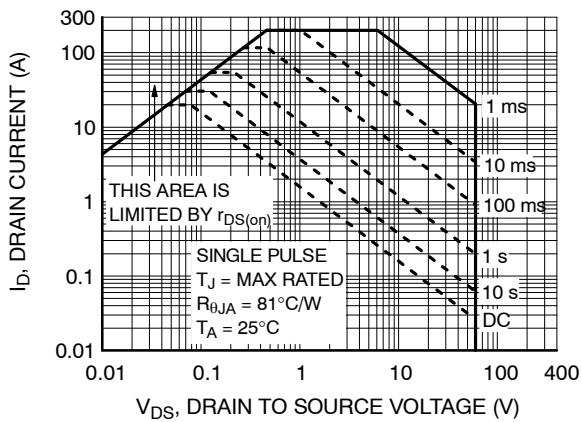
**Figure 8. Capacitance vs. Drain to Source Voltage**



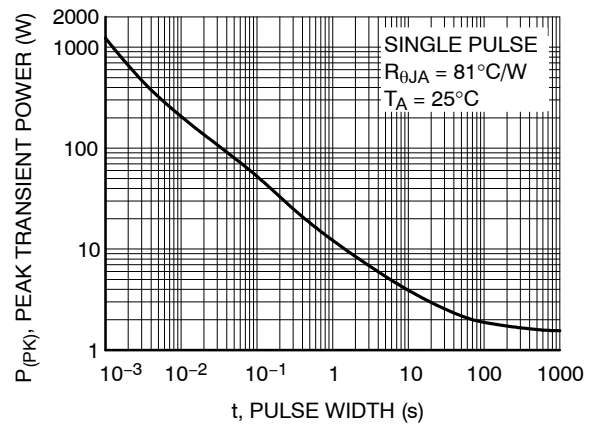
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

# FDMS86500DC

## TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

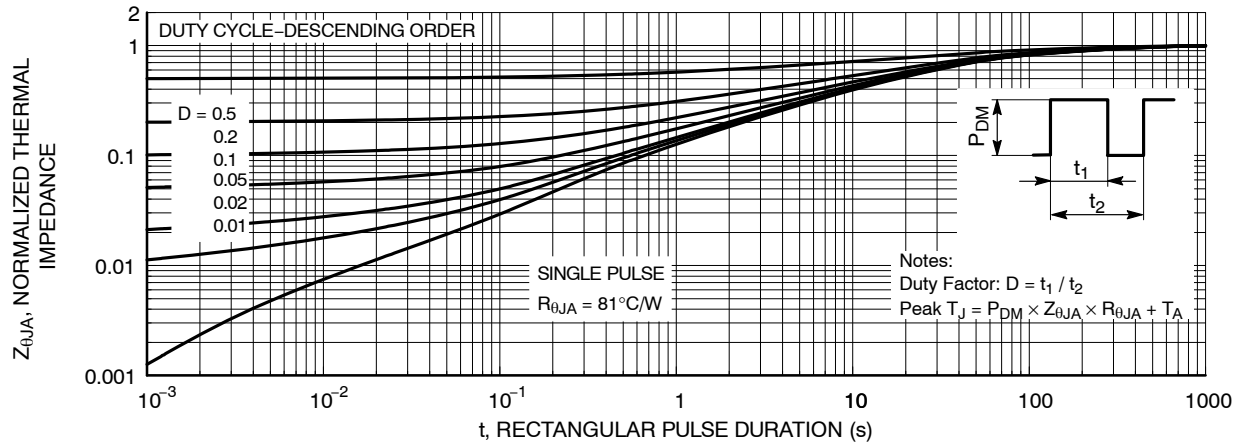


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

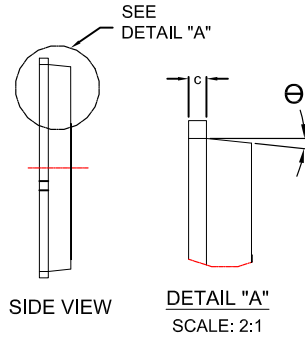
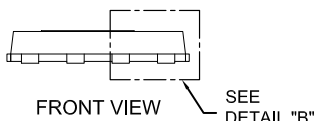
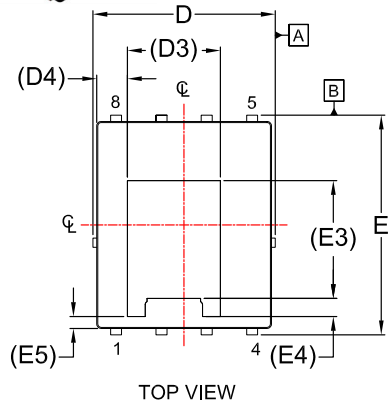
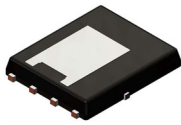
## PACKAGE DIMENSIONS

ON Semiconductor®



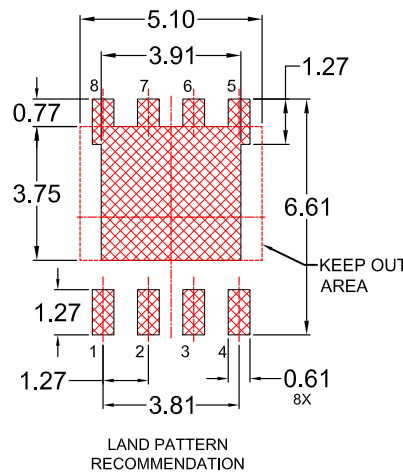
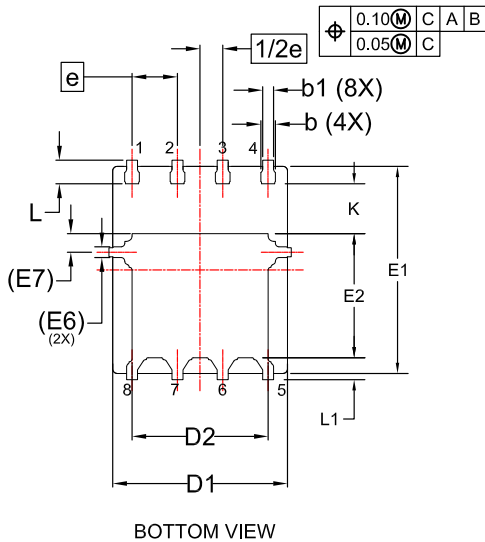
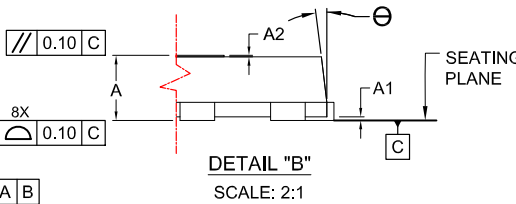
### DFN8 5x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D

DATE 25 AUG 2020



NOTES:

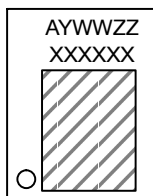
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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