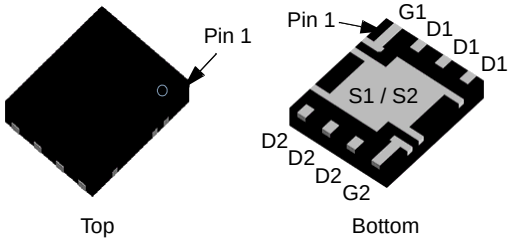
MOSFET – Dual, N-Channel, Shielded Gate, POWERTRENCH®

100 V, 39 A, 10.5 mΩ

FDMD86100

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
100 V	10.5 mΩ @ 10 V	39 A
	17.3 mΩ @ 6 V	



PQFN8 5X6, 1.27P
(Power 5 x 6)
CASE 483AS

General Description

This package integrates two N−Channel devices connected internally in common−source configuration and incorporates Shielded Gate technology. This enables very low package parasitics and optimized thermal path to the common source pad on the bottom. Provides a very small footprint (5 x 6 mm) for higher power density.

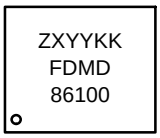
Features

- Common Source Configuration to Eliminate PCB Routing
- Large Source Pad on Bottom of Package for Enhanced Thermals
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 10.5 mΩ at V_{GS} = 10 V, I_D = 10 A
- Max $r_{DS(on)}$ = 17.3 mΩ at V_{GS} = 6 V, I_D = 7.8 A
- Ideal for Flexible Layout in Secondary Side Synchronous Rectification
- 100% UIL tested
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

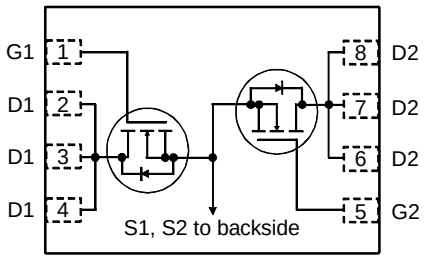
- Isolated DC−DC Synchronous Rectifiers
- Common Ground Load Switches

MARKING DIAGRAM



ZZ = Assembly Site Code
X = Year Code
YY = Weekly Code
KK = Lot Code
FDMD86100 = Device Code

PIN ASSIGNMENT



MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current − Continuous T_C = 25°C (Note 5) − Continuous T_C = 100°C (Note 5) − Continuous T_A = 25°C (Note 1a) − Pulsed (Note 4)	 39 24 10 299	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	337	mJ
P_D	Power Dissipation T_C = 25°C T_A = 25°C (Note 1a)	 33 2.2	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

ORDERING INFORMATION

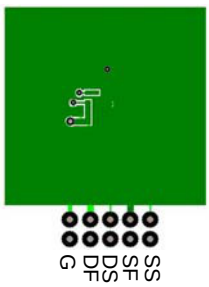
See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

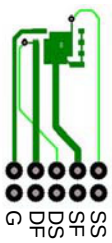
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	7	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−10	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 10 A	–	7.8	10.5	mΩ
		V_{GS} = 6 V, I_D = 7.8 A	–	12	17.3	
		V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	–	14.5	19.5	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 10 A	–	26	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	1469	2060	pF
C_{oss}	Output Capacitance		–	321	450	pF
C_{rss}	Reverse Transfer Capacitance		–	12	20	pF
R_g	Gate Resistance		0.1	1.3	3.3	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 10 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	13	23	ns
t_r	Rise Time		–	4.3	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	18	32	ns
t_f	Fall Time		–	4.1	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 10 A	–	21	30	nC
	Total Gate Charge	V_{GS} = 0 V to 6 V, V_{DD} = 50 V, I_D = 10 A	–	13	18	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 10 A	–	6.6	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	4.1	–	nC
DRAIN−SOURCE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 10 A (Note 2)	–	0.8	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 10 A, di/dt = 100 A/μs	–	46	74	ns
Q_{rr}	Reverse Recovery Charge		–	46	74	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user’s board design.



a. 55°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 337 mJ is based on starting T_J = 25°C, L = 3 mH, I_{AS} = 15 A, V_{DD} = 100 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 47 A.
4. Pulse Id refers to Figure 11 SOA graph for for details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

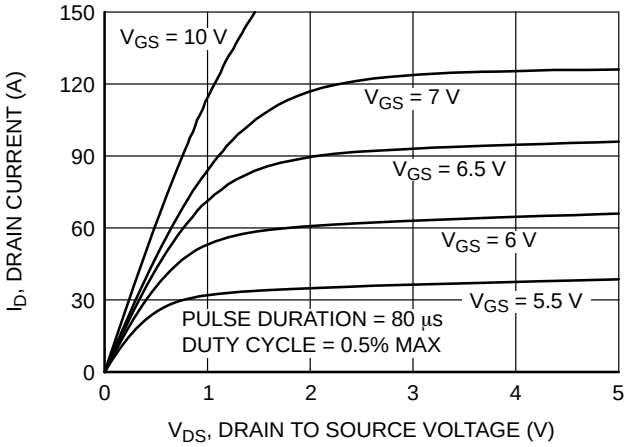


Figure 1. On−Region Characteristics

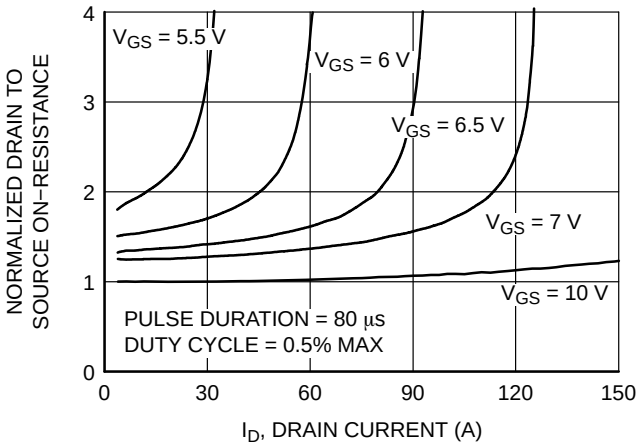


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

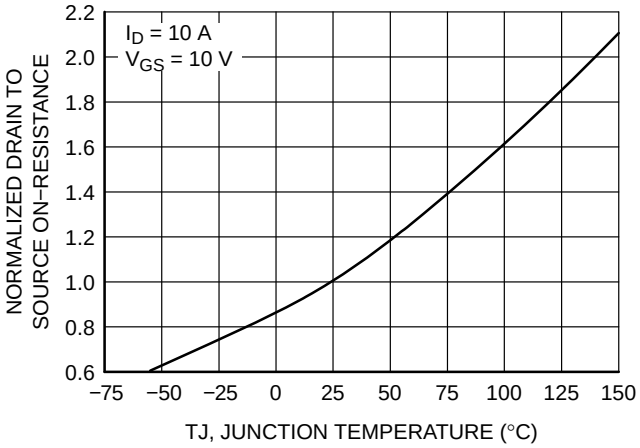


Figure 3. Normalized On−Resistance vs. Junction Temperature

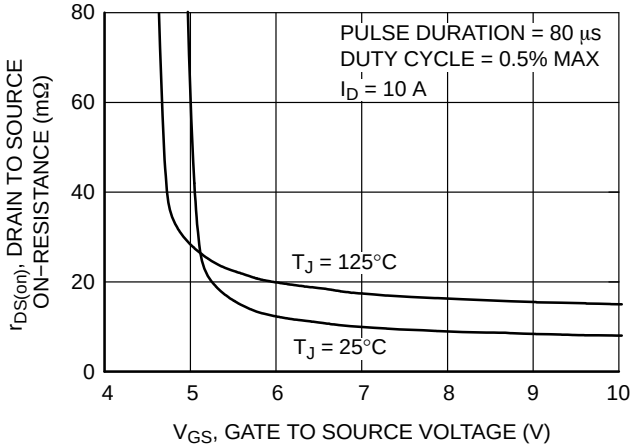


Figure 4. On−Resistance vs. Gate to Source Voltage

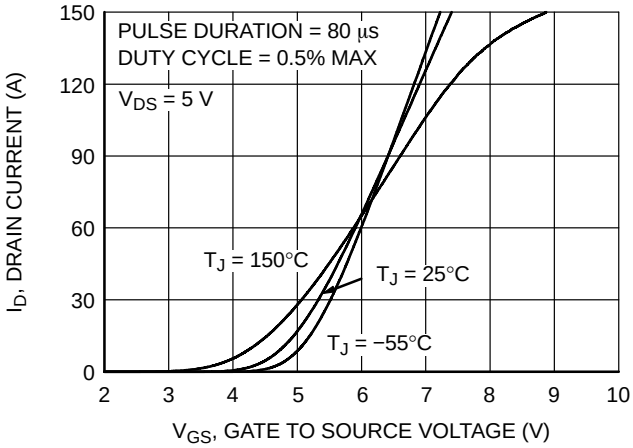


Figure 5. Transfer Characteristics

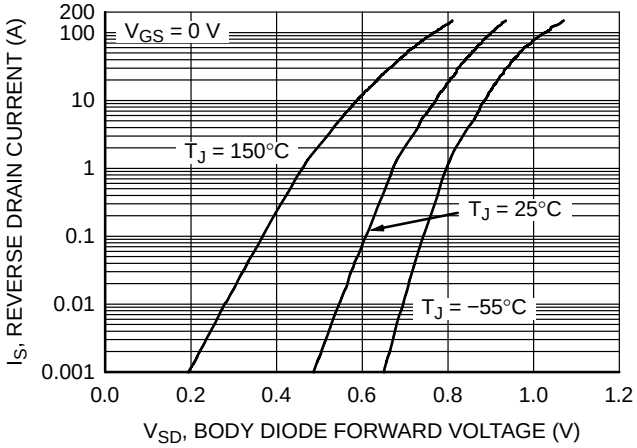


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

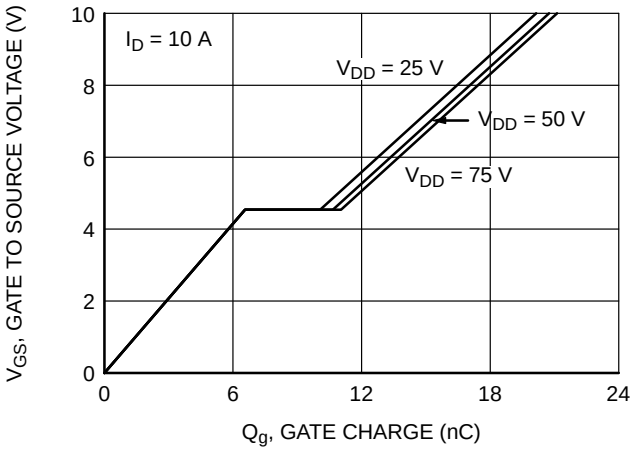


Figure 7. Gate Charge Characteristics

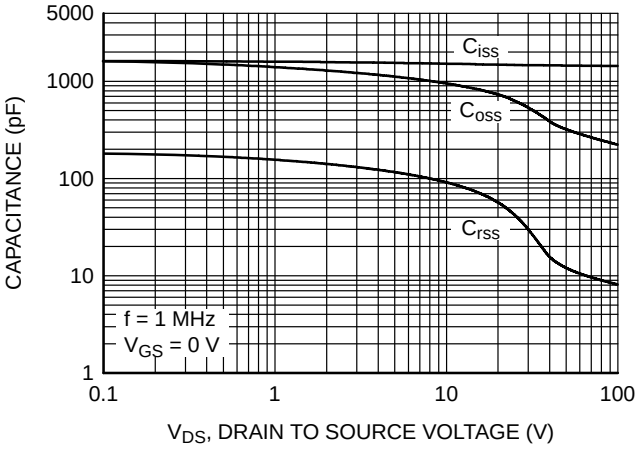


Figure 8. Capacitance vs. Drain to Source Voltage

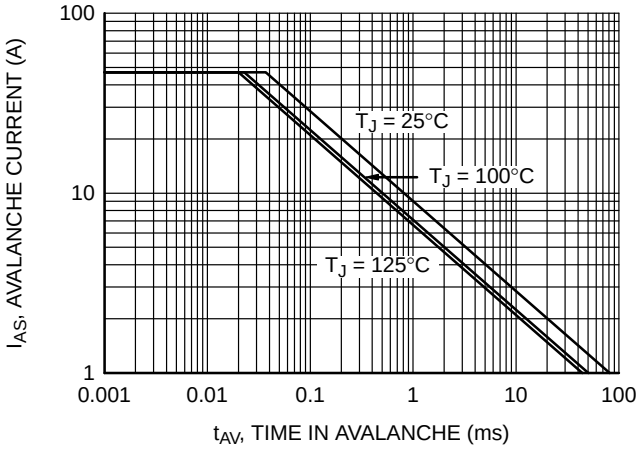


Figure 9. Unclamped Inductive Switching Capability

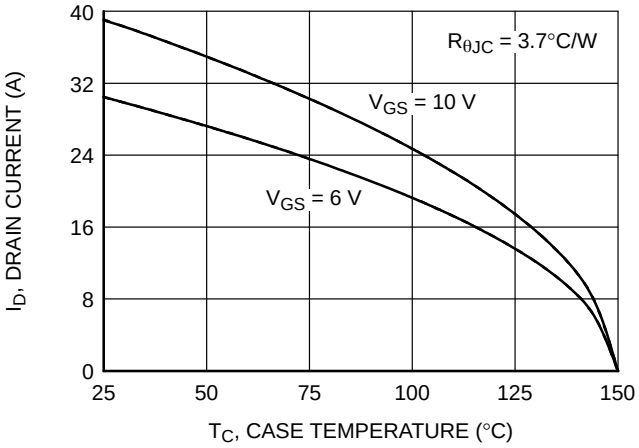


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

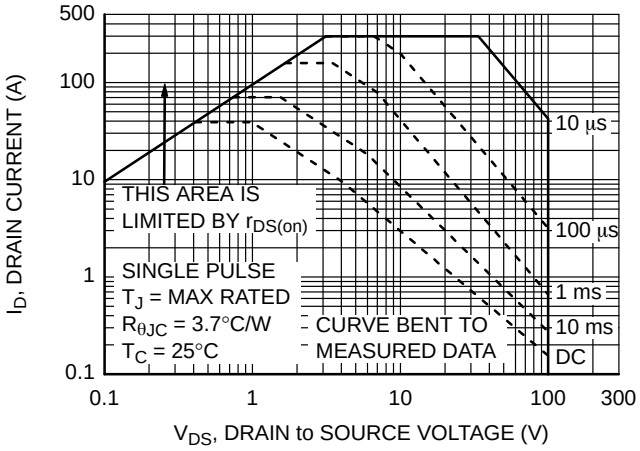


Figure 11. Forward Bias Safe Operating Area

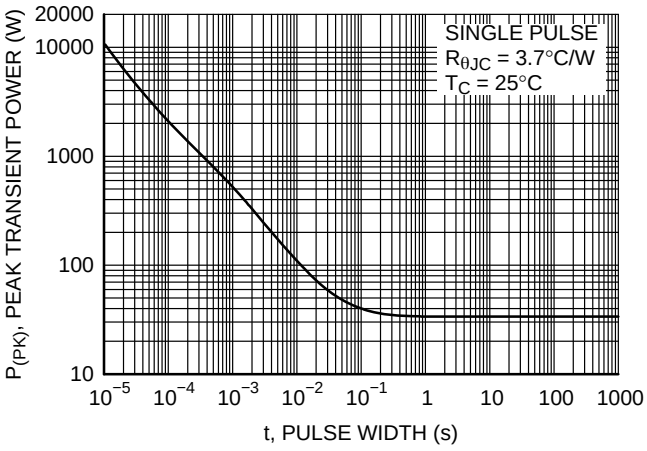


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

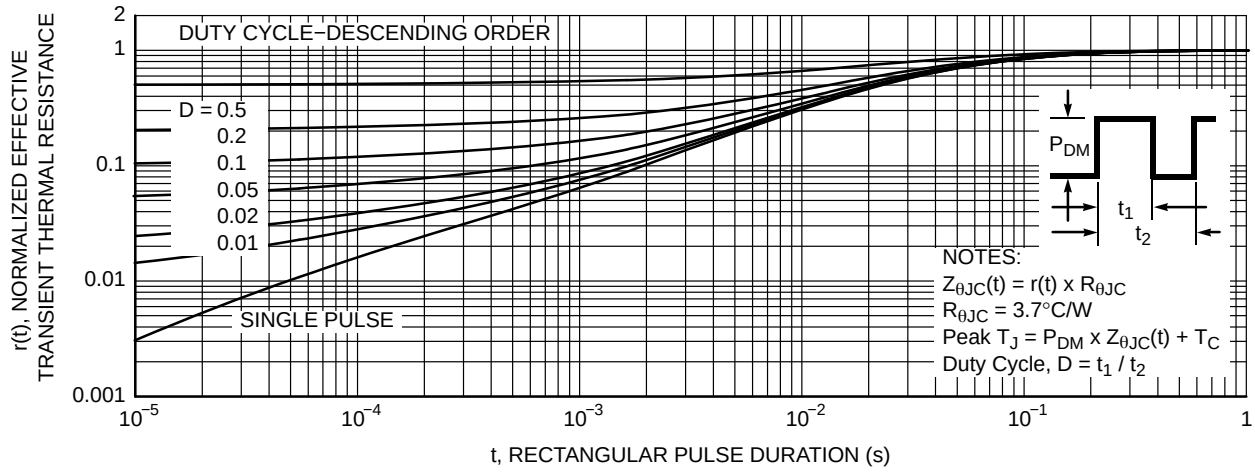


Figure 13. Junction−to−Case Transient Thermal Response Curve

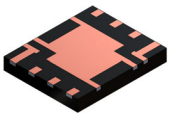
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMD86100	FDMD86100	PQFN8 5X6, 1.27P (Power 5 x 6) (Pb−Free, Halide Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

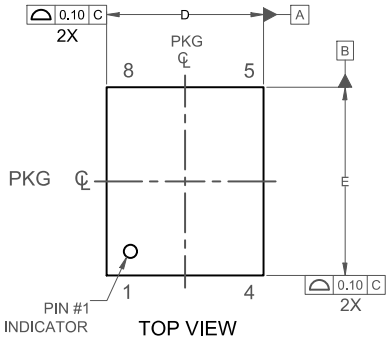
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

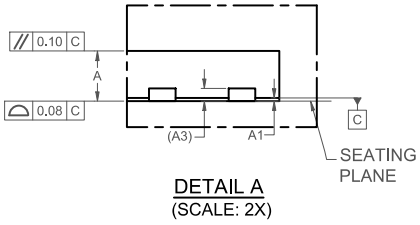


PQFN8 5X6, 1.27P
CASE 483AS
ISSUE A

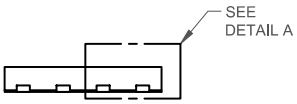
DATE 17 MAY 2021



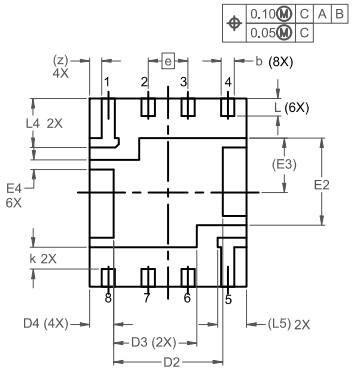
TOP VIEW



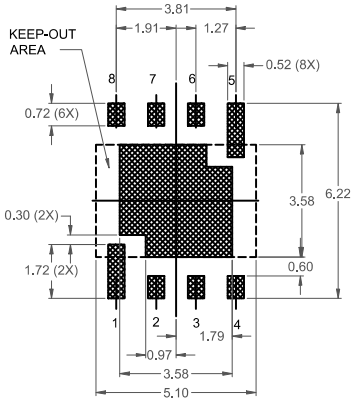
DETAIL A
(SCALE: 2X)



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

A) PACKAGE REFERENCE :
TO JEDEC REGISTRATION, MO-240B, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP-OUT AREA

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.37	0.42	0.47
A3		0.20 REF	
D	4.90	5.00	5.10
D2	3.38	3.48	3.58
D3	2.55	2.65	2.75
D4	0.66	0.76	0.86
E	5.90	6.00	6.10
E2	2.68	2.78	2.88
E3		1.74 REF	
E4	0.25	0.30	0.35
e		1.27 BSC	
k	0.60	0.70	0.80
L	0.46	0.56	0.66
L4	1.46	1.56	1.66
L5	0.82	0.92	1.02
z		0.39 REF	

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DESCRIPTION:	**PQFN8 5X6, 1.27P**		**PAGE 1 OF 1**

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