

MOSFET – Dual, N-Channel, POWERTRENCH®

Q1: 40 V, 156 A, 1.5 mΩ

Q2: 40 V, 156 A, 1.5 mΩ

FDMD8540L

General Description

This device includes two 40 V N-Channel MOSFETs in a dual Power (5 mm x 6 mm) package. HS source and LS drain internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}/Q_g$ FOM silicon.

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 1.5 mΩ at $V_{GS} = 10$ V, $I_D = 33$ A
- Max $r_{DS(on)}$ = 2.2 mΩ at $V_{GS} = 4.5$ V, $I_D = 26$ A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.5 mΩ at $V_{GS} = 10$ V, $I_D = 33$ A
- Max $r_{DS(on)}$ = 2.2 mΩ at $V_{GS} = 4.5$ V, $I_D = 26$ A

- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- This Device is Pb-Free and are RoHS Compliant

Applications

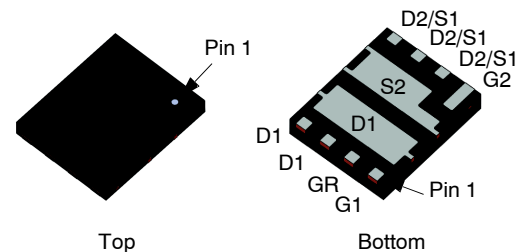
- POL Synchronous Dual
- One Phase Motor Half Bridge
- Half/Full Bridge Secondary Synchronous Rectification



ON Semiconductor®

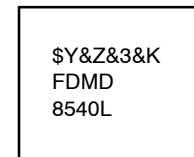
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V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
40 V	1.5 mΩ @ 10 V	156 A
	2.2 mΩ @ 4.5 V	

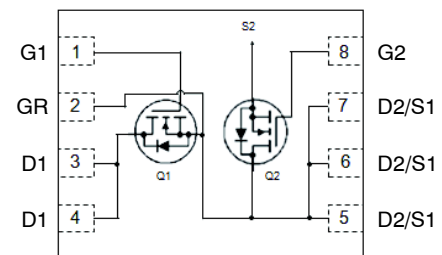


PQFN8 5X6, 1.27P
Power 5 x 6
CASE 483AT

MARKING DIAGRAM



FDMD8540L = Specific Device Code
 \$Y = ON Semiconductor Logo
 &Z = Assembly Plant Code
 &3 = 3-Digit Date Code Format
 &K = 2-Digits Lot Run Traceability Data



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

FDMD8540L

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit	
V_{DS}	Drain to Source Voltage		40	40	V	
V_{GS}	Gate to Source Voltage		± 20	± 20	V	
I_D	Drain Current	- Continuous	$T_C = 25^\circ\text{C}$ (Note 3)	156	156	A
		- Continuous	$T_C = 100^\circ\text{C}$ (Note 3)	99	99	
		- Continuous	$T_A = 25^\circ\text{C}$	33 (Note 4a)	33 (Note 4b)	
		- Pulsed	(Note 2)	886	886	
E_{AS}	Single Pulse Avalanche Energy (Note 1)		541	541	mJ	
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	62	62	W	
	Power Dissipation	$T_A = 25^\circ\text{C}$	2.3 (Note 4a)	2.3 (Note 4b)		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		$^\circ\text{C}$	

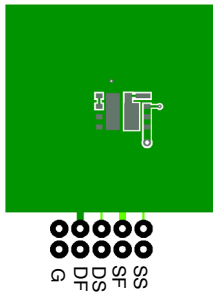
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Q1: E_{AS} of 541 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3$ mH, $I_{AS} = 19$ A, $V_{DD} = 40$ V, $V_{GS} = 10$ V. 100% tested at $L = 0.1$ mH, $I_{AS} = 59$ A.
Q2: E_{AS} of 541 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3$ mH, $I_{AS} = 19$ A, $V_{DD} = 40$ V, $V_{GS} = 10$ V. 100% tested at $L = 0.1$ mH, $I_{AS} = 59$ A.
- Pulsed I_D please refer to Figure 11 and Figure 24 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

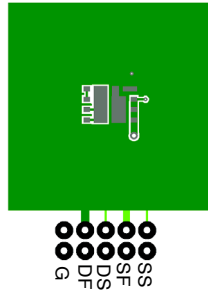
THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.0	2.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	55 (Note 4a)	55 (Note 4b)	

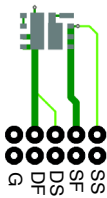
- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



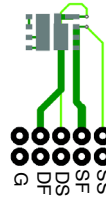
a. $55^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $55^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



c. $155^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper



d. $155^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	Q1 Q2	40 40	– –	– –	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 mA, referenced to 25°C	Q1 Q2	– –	20 20	– –	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V	Q1 Q2	– –	– –	1 1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	Q1 Q2	– –	– –	±100 ±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 mA	Q1 Q2	1.0 1.0	1.8 1.8	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	Q1 Q2	– –	–6 –6	– –	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 33 A	Q1	–	1.25	1.5	mΩ
		V _{GS} = 4.5 V, I _D = 26 A		–	1.65	2.2	
		V _{GS} = 10 V, I _D = 33 A, T _J = 125°C		–	1.7	2.1	
		V _{GS} = 10 V, I _D = 33 A	Q2	–	1.25	1.5	
		V _{GS} = 4.5 V, I _D = 26 A		–	1.65	2.2	
		V _{GS} = 10 V, I _D = 33 A, T _J = 125°C		–	1.7	2.1	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 33 A	Q1 Q2	– –	178 178	– –	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V f = 1 MHz	Q1 Q2	– –	5670 5670	7940 7940	pF
C _{oss}	Output Capacitance		Q1 Q2	– –	1668 1668	2335 2335	pF
C _{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	75 75	135 135	pF
R _g	Gate Resistance		Q1 Q2	0.1 0.1	1.6 1.6	3.2 3.2	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 20 V, I _D = 33 A V _{GS} = 10 V, R _{GEN} = 6 Ω		Q1 Q2	– –	15 15	28 28	ns
t _r	Rise Time			Q1 Q2	– –	13 13	24 24	ns
t _{d(off)}	Turn-Off Delay Time			Q1 Q2	– –	51 51	81 81	ns
t _f	Fall Time			Q1 Q2	– –	14 14	25 25	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V	V _{DD} = 20 V, I _D = 33 A	Q1 Q2	– –	81 81	113 113	nC
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 4.5 V	V _{DD} = 20 V, I _D = 33 A	Q1 Q2	– –	38 38	54 54	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 20 V, I _D = 33 A		Q1 Q2	– –	15 15	– –	nC
Q _{gd}	Gate to Drain "Miller" Charge	V _{DD} = 20 V, I _D = 33 A		Q1 Q2	– –	11 11	– –	nC

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 33\text{ A}$ (Note 5)	Q1 Q2	- -	0.8 0.8	1.3 1.3	V
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 5)	Q1 Q2	- -	0.7 0.7	1.2 1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 33\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2	- -	54 54	86 86	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2	- -	38 38	60 60	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

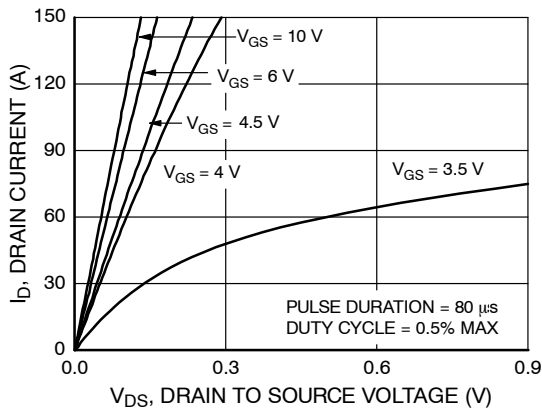


Figure 1. On Region Characteristics

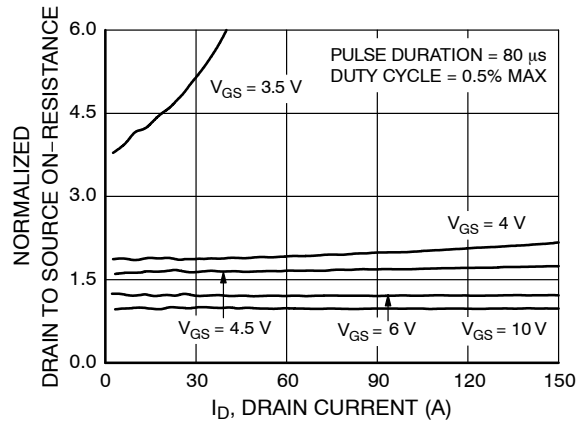


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

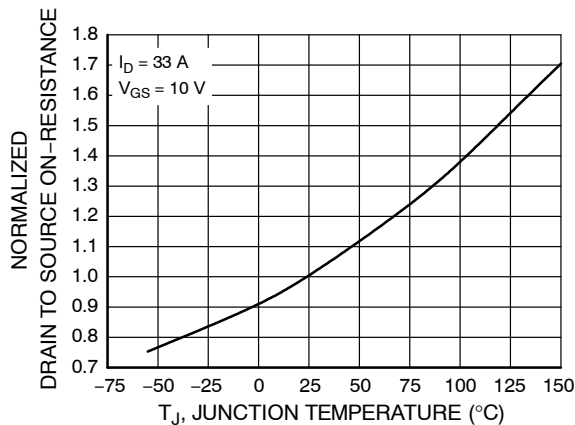


Figure 3. Normalized On Resistance vs. Junction Temperature

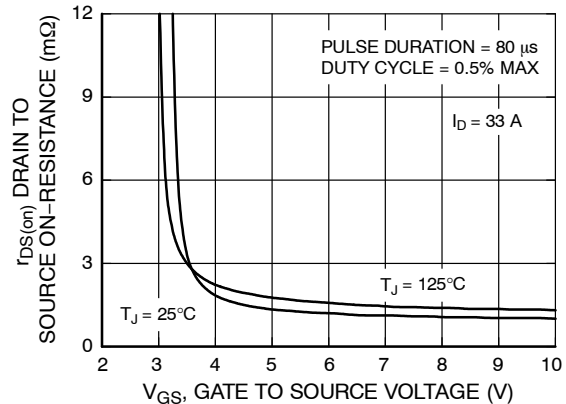


Figure 4. On-Resistance vs. Gate to Source Voltage

FDMD8540L

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

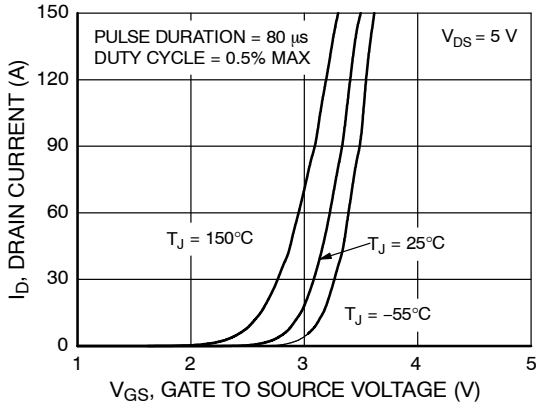


Figure 5. Transfer Characteristics

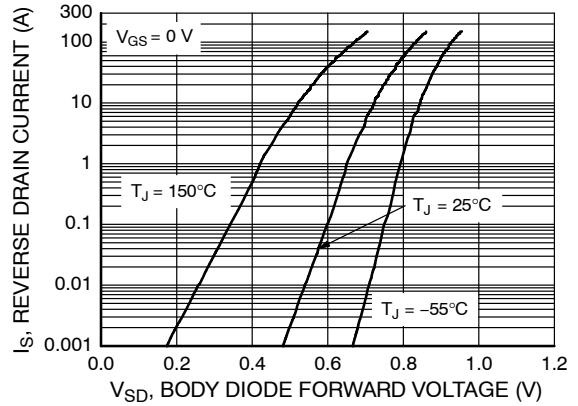


Figure 6. Source to Gate Diode Forward Voltage vs. Source Current

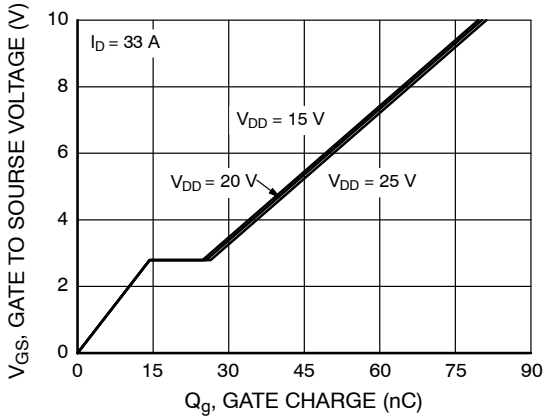


Figure 7. Gate Charge Characteristics

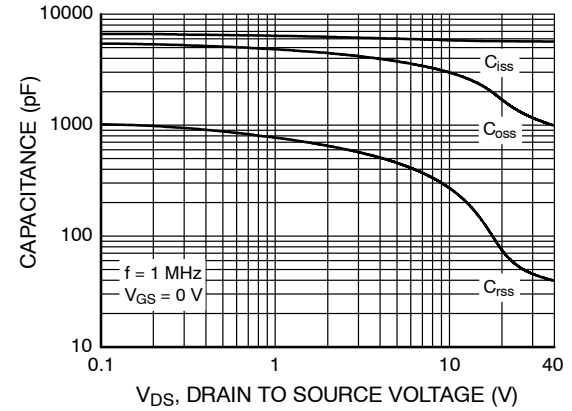


Figure 8. Capacitance vs. Drain to Source Voltage

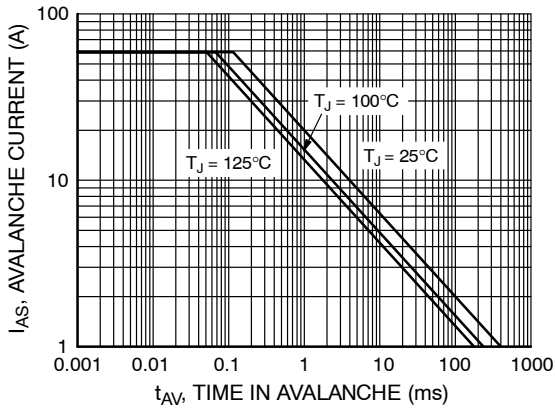


Figure 9. Unclamped Inductive Switching Capability

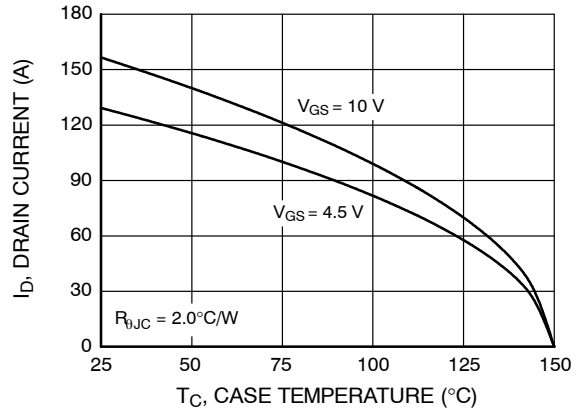


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

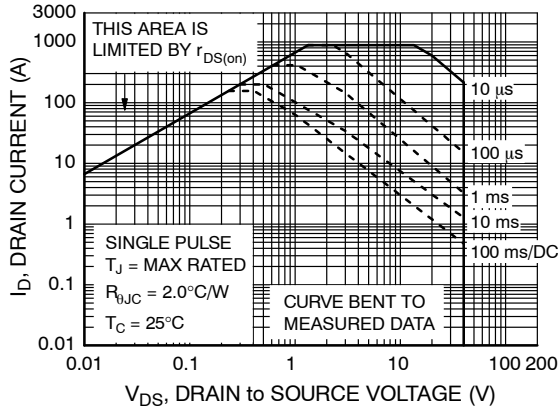


Figure 11. Forward Bias Safe Operating Area

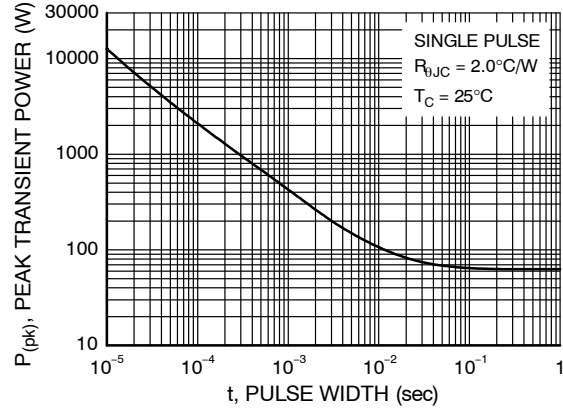


Figure 12. Single Pulse Maximum Power Dissipation

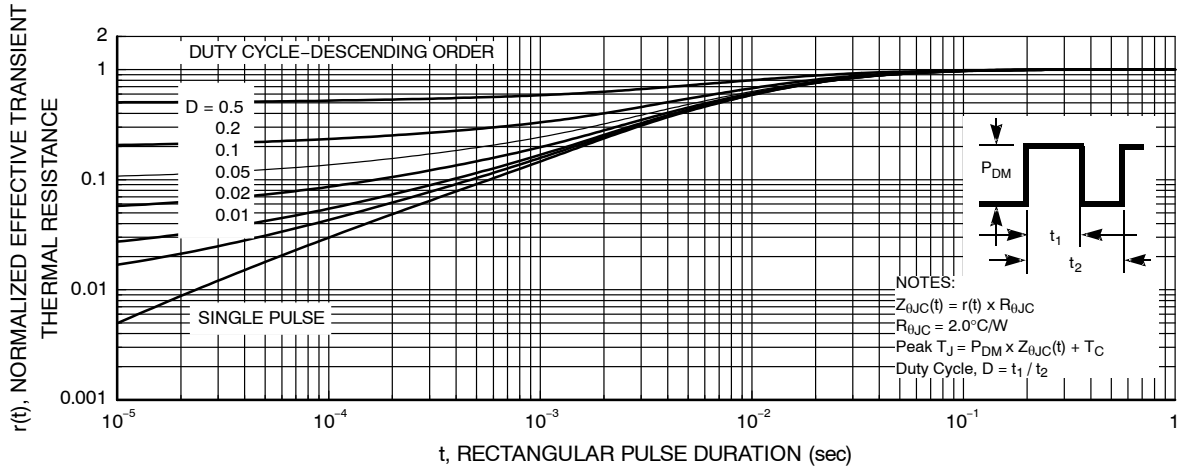


Figure 13. Junction-to-Case Transient Thermal Response Curve

FDMD8540L

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

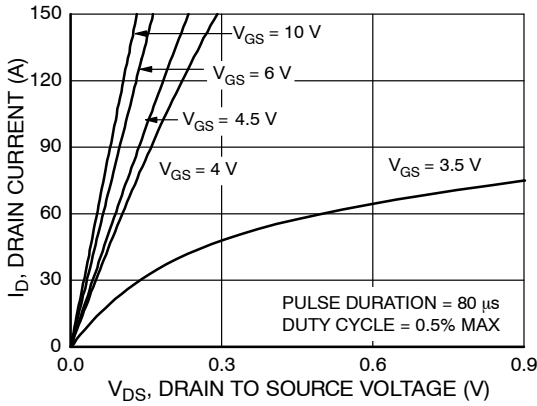


Figure 14. On-Region Characteristics

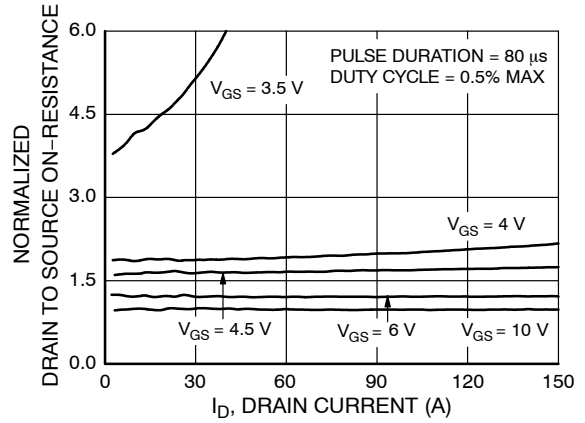


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

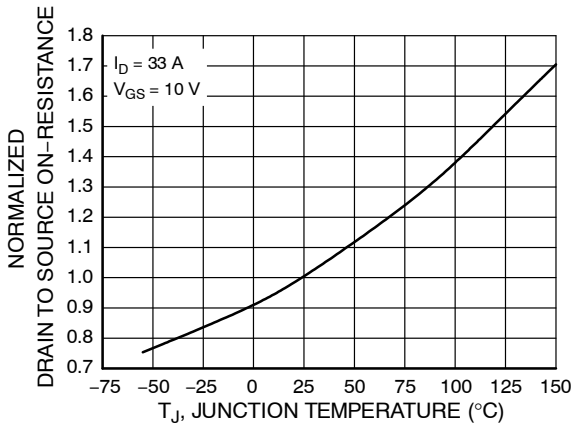


Figure 16. Normalized On Resistance vs. Junction Temperature

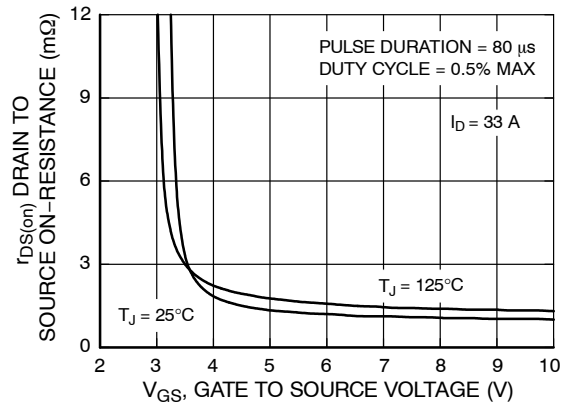


Figure 17. On-Resistance vs. Gate to Source Voltage

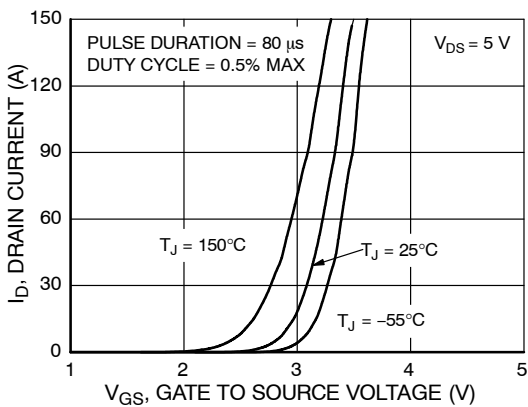


Figure 18. Transfer Characteristics

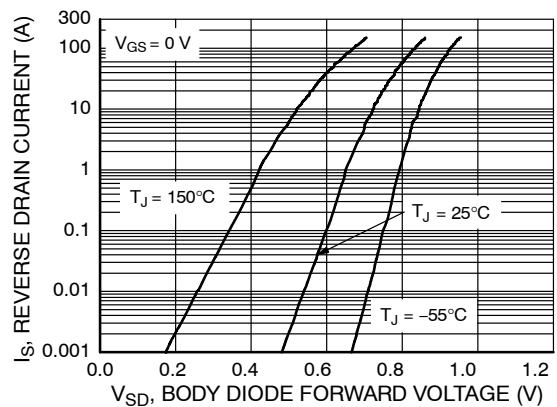


Figure 19. Source to Gate Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

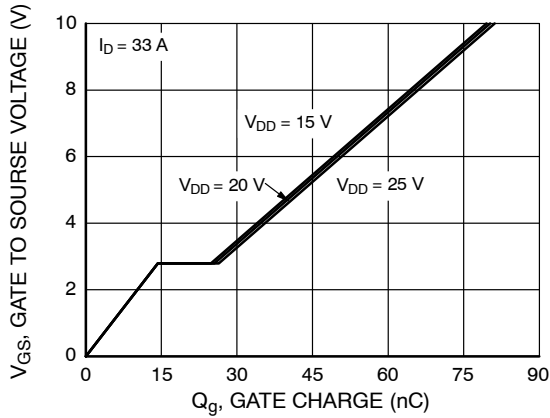


Figure 20. Gate Charge Characteristics

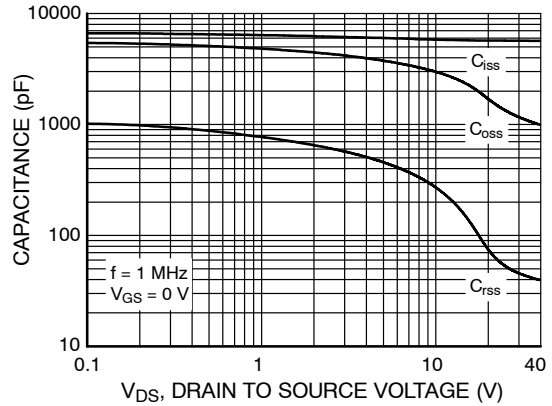


Figure 21. Capacitance vs. Drain to Source Voltage

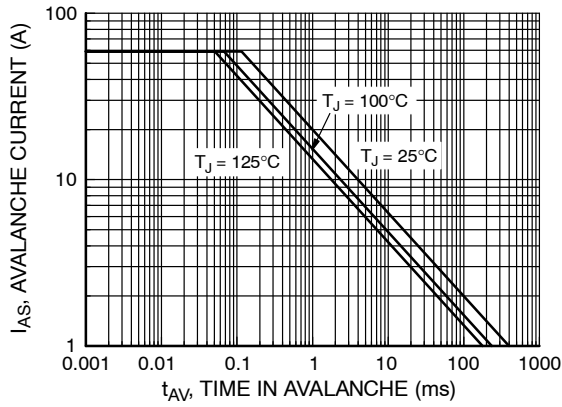


Figure 22. Unclamped Inductive Switching Capability

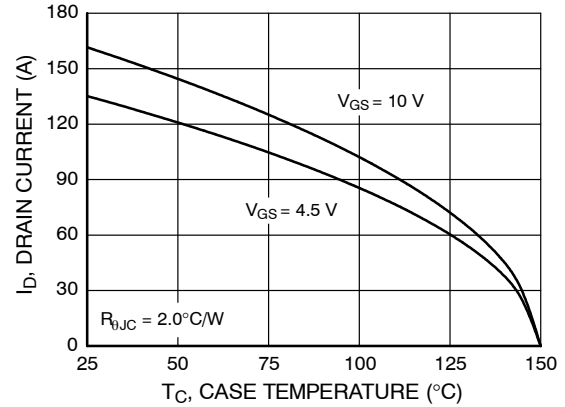


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

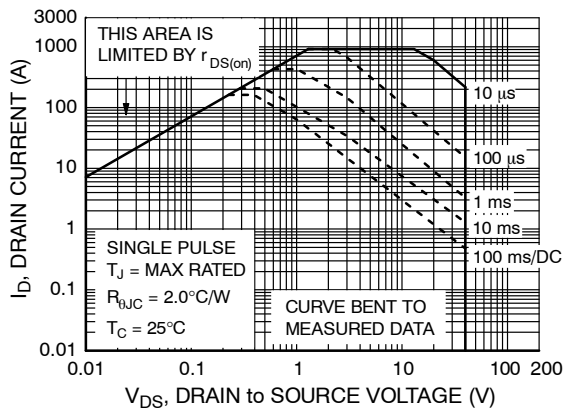


Figure 24. Forward Bias Safe Operating Area

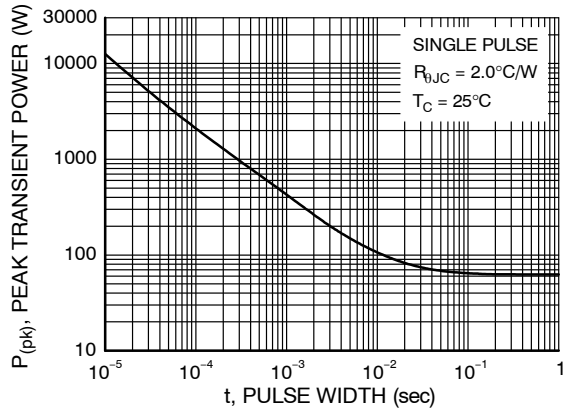


Figure 25. Single Pulse Maximum Power Dissipation

FDMD8540L

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

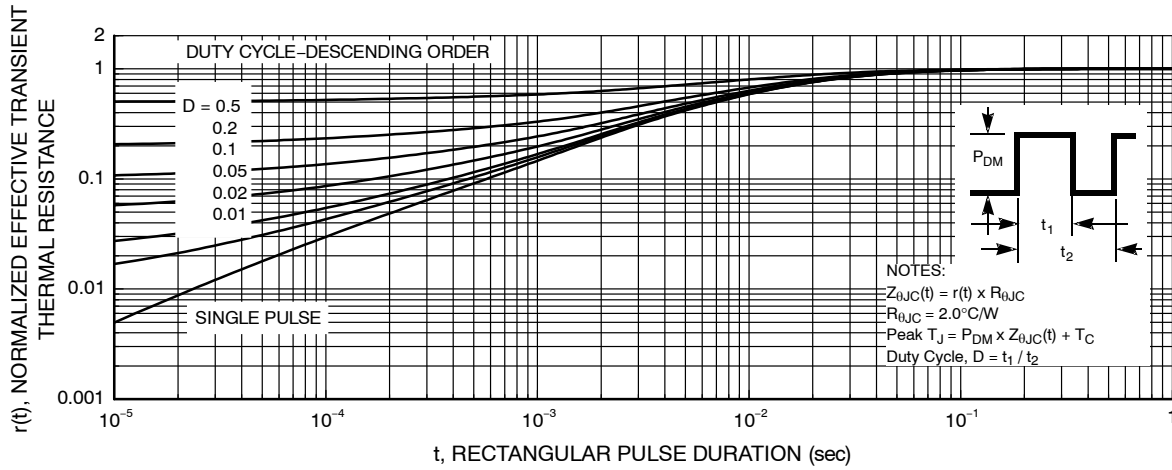


Figure 26. Junction-to-Case Transient Thermal Response Curve

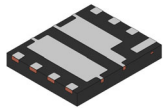
PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package Type	Reel Size	Tape Width	Shipping [†]
FDMD8540L	FDMD8540L	PQFN8 5X6, 1.27P Power 5 x 6 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

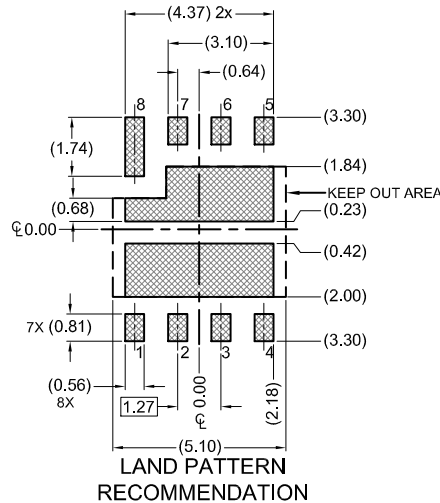
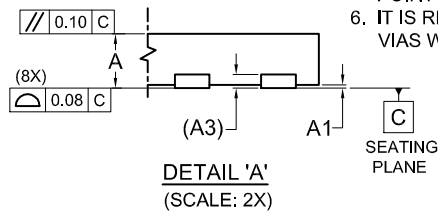
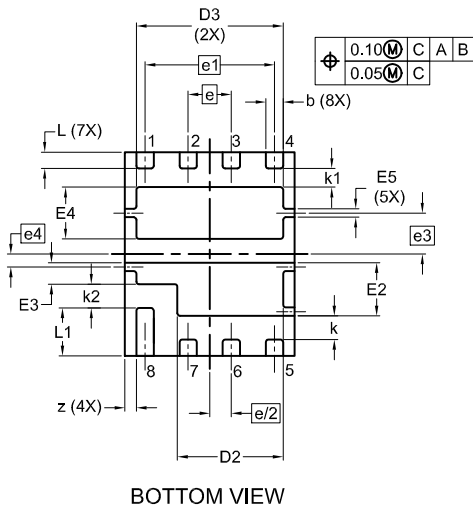
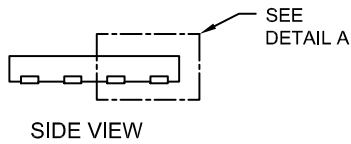
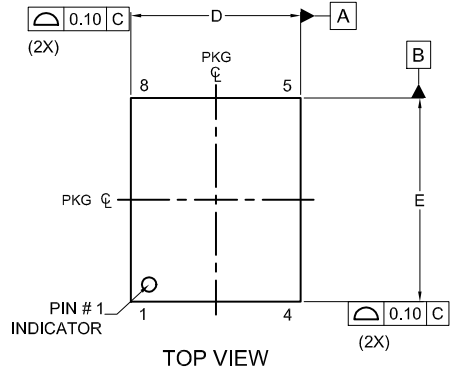
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



PQFN8 5X6, 1.27P CASE 483AT ISSUE B

DATE 28 APR 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.41	0.51	0.61
D	4.90	5.00	5.10
D2	3.01	3.11	3.21
D3	4.22	4.32	4.42
E	5.90	6.00	6.10
E2	1.47	1.57	1.67
E3	0.53	0.63	0.73
E4	1.42	1.52	1.62
E5	0.20	0.25	0.30
e	1.27 BSC		
e1	3.81 BSC		
e/2	0.64 BSC		
e3	1.08 BSC		
e4	0.25 BSC		
k	0.60	0.70	0.80
k1	0.45	0.55	0.65
k2	0.60	0.70	0.80
L	0.38	0.48	0.58
L1	1.31	1.41	1.51
z	0.34 REF		

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	PQFN8 5X6, 1.27P	PAGE 1 OF 1

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