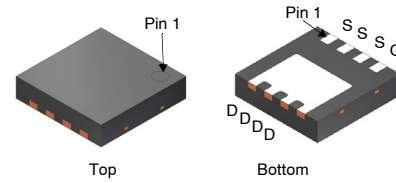


# MOSFET – N-Channel, Shielded Gate POWERTRENCH®

60 V, 84 A, 4.3 mΩ

## FDMC86570L



WDFN8 3.3x3.3, 0.65P  
CASE 483AW

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 4.3 mΩ at  $V_{GS} = 10$  V,  $I_D = 18$  A
- Max  $r_{DS(on)}$  = 6.5 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 15$  A
- High Performance Technology for Extremely Low  $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

### Application

- DC-DC Conversion

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

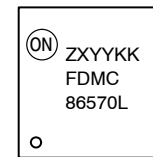
Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current		A
	–Continuous $T_C = 25^\circ\text{C}$ (Note 5)	84	
	–Continuous $T_C = 100^\circ\text{C}$ (Note 5)	53	
	–Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	18	
	–Pulsed (Note 4)	416	
EAS	Single Pulse Avalanche Energy (Note 3)	253	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	54	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

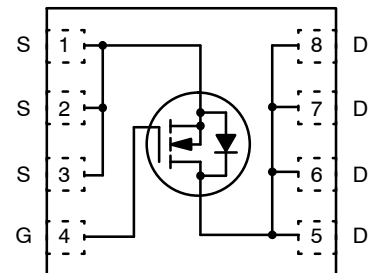
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	53	$^\circ\text{C}/\text{W}$

### MARKING DIAGRAM



- Z = Assembly Plant Code
- X = Year Code
- YY = Week Code
- KK = Lot Code
- FDMC = Specific Device Code
- 86570L = Specific Device Code

### PIN ASSIGNMENT



N-Channel MOSFET

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDMC86570L

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	60			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C		30		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0	1.8	3.0	V
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C		-7		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18 A		3.1	4.3	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		4.7	6.5	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18 A, T <sub>J</sub> = 125°C		5.0	6.9	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 18 A		75		S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4790	6705	pF
C <sub>oss</sub>	Output Capacitance			821	1150	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			19	30	pF
R <sub>g</sub>	Gate Resistance		0.1	0.9	2.7	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 18 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		19	34	ns
t <sub>r</sub>	Rise Time			6.2	12	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			38	61	ns
t <sub>f</sub>	Fall Time			3.9	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	V <sub>DD</sub> = 30 V I <sub>D</sub> = 18 A	63	88	nC
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 4.5 V		29	41	nC
Q <sub>gs</sub>	Gate to Source Charge			14		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			6.3		nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

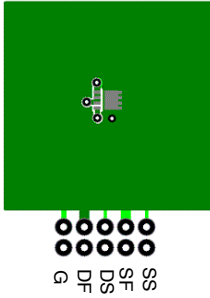
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 18 A (Note 2)		0.8	1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.9 A (Note 2)		0.7	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 18 A, di/dt = 100 A/μs		43	69	ns
Q <sub>rr</sub>	Reverse Recovery Charge			26	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

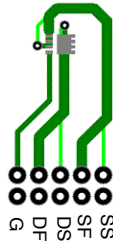
# FDMC86570L

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0 %.
3.  $E_{AS}$  of 253 mJ is based on starting  $T_J = 25$  °C,  $L = 3$  mH,  $I_{AS} = 13$  A,  $V_{DD} = 60$  V,  $V_{GS} = 10$  V. 100% test at  $L = 0.1$  mH,  $I_{AS} = 43$  A.
4. Pulsed  $I_D$  please refer to Figure 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

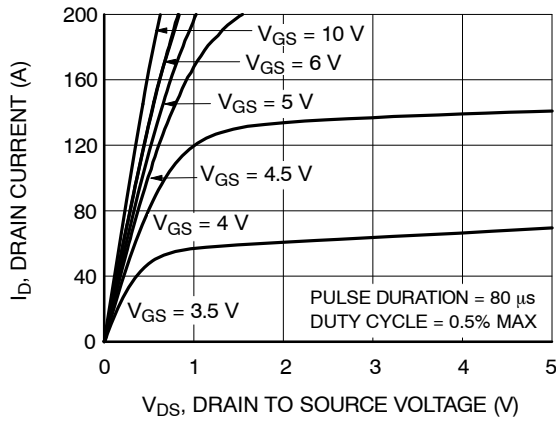


Figure 1. On-Region Characteristics

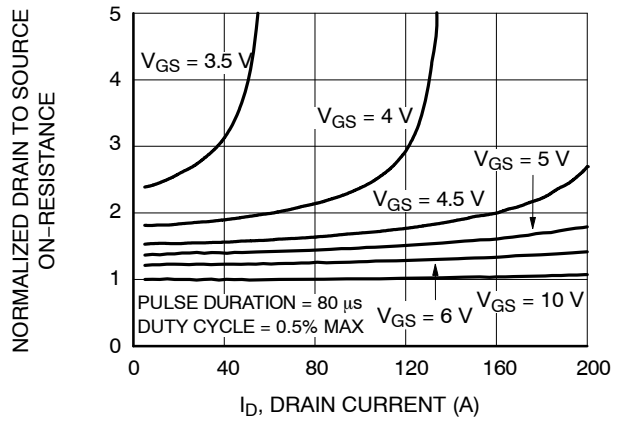


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

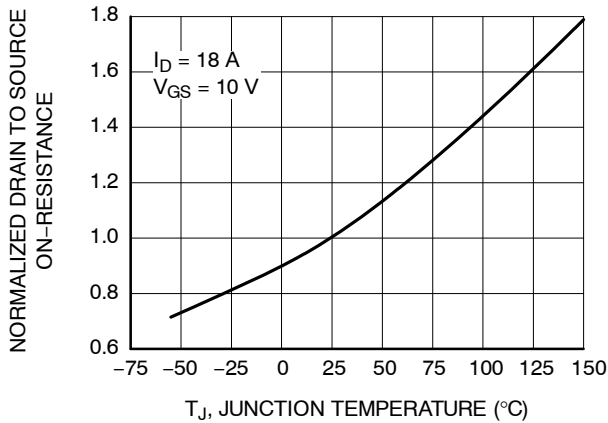


Figure 3. Normalized On-Resistance vs. Junction Temperature

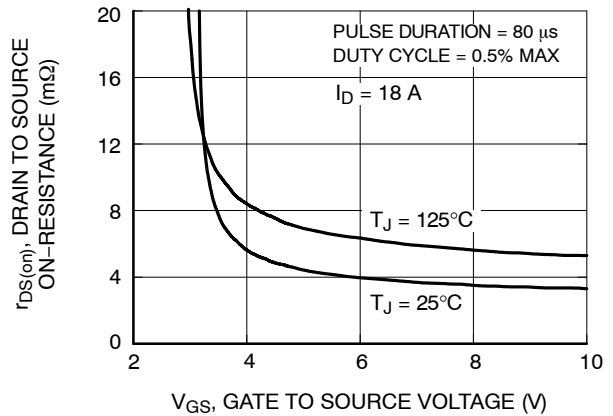


Figure 4. On-Resistance vs. Gate to Source Voltage

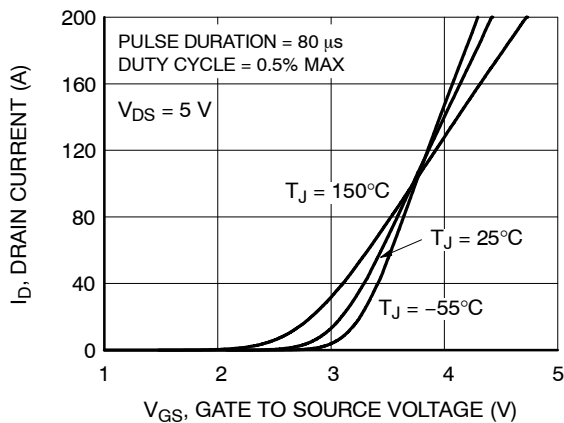


Figure 5. Transfer Characteristics

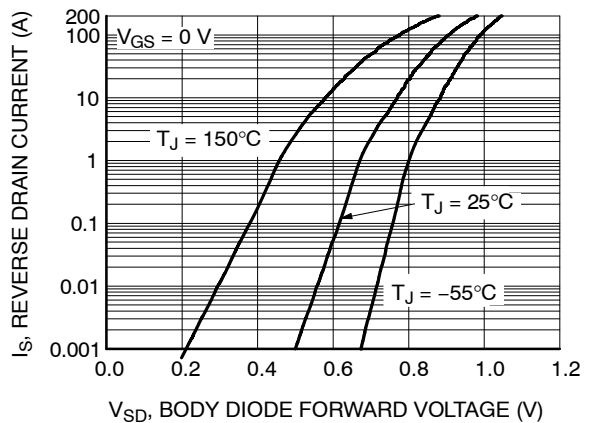


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

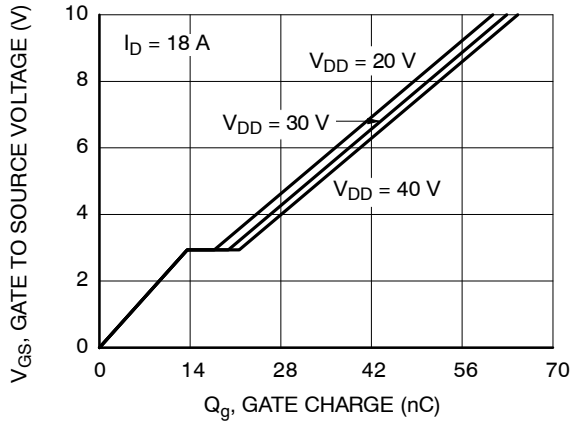


Figure 7. Gate Charge Characteristics

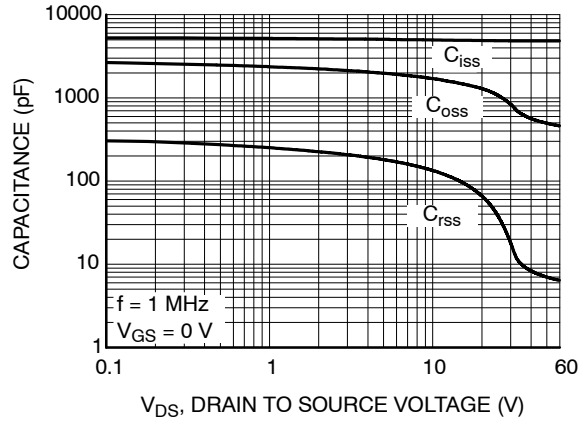


Figure 8. Capacitance vs. Drain to Source Voltage

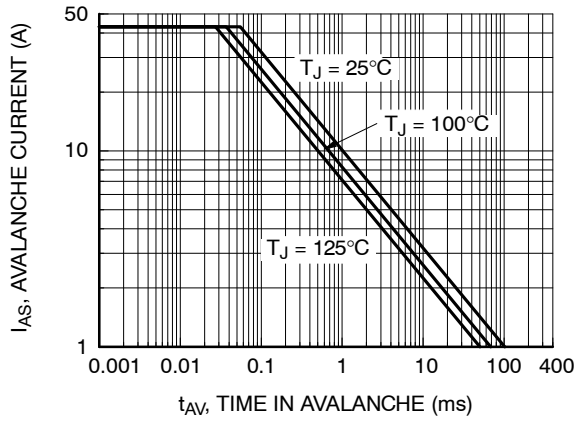


Figure 9. Unclamped Inductive Switching Capability

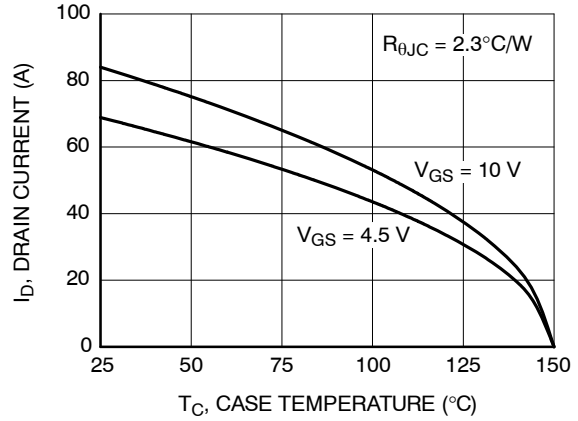


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

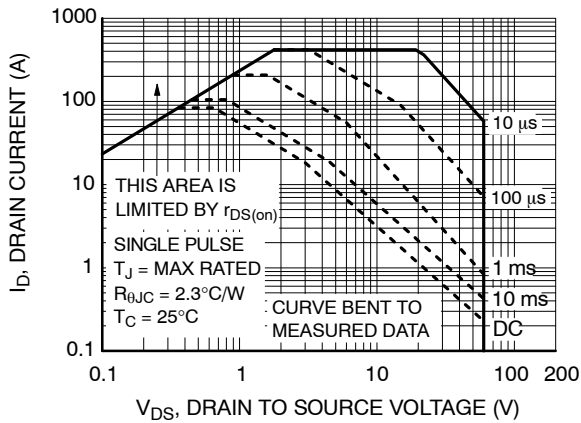


Figure 11. Forward Bias Safe Operating Area

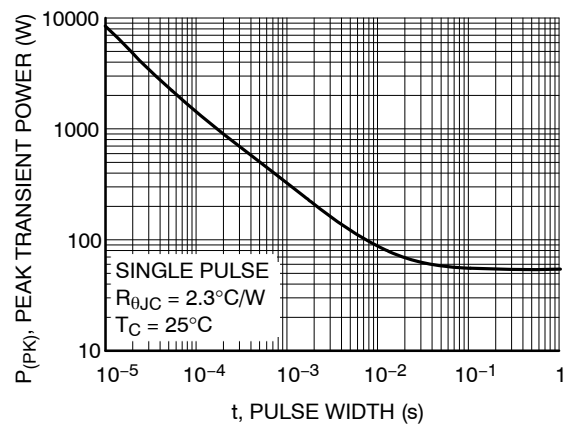


Figure 12. Single Pulse Maximum Power Dissipation

# FDMC86570L

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

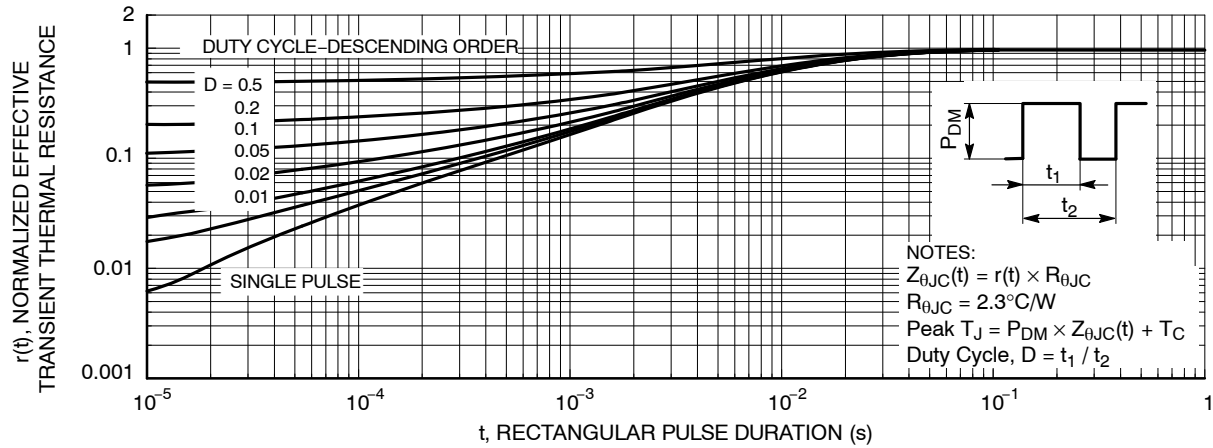


Figure 13. Junction-to-Case Transient Thermal Response Curve

### ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping <sup>†</sup>
FDMC86570L	FDMC86570L	WDFN8 3.3x3.3, 0.65P (Pb-Free)	3000 / Tape & Reel

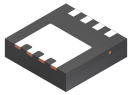
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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# MECHANICAL CASE OUTLINE

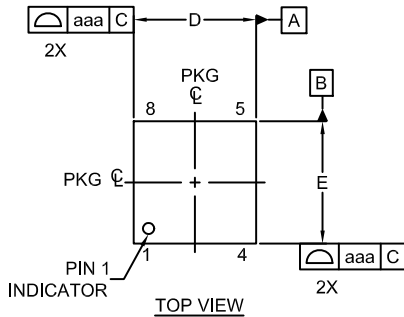
## PACKAGE DIMENSIONS

ON Semiconductor®

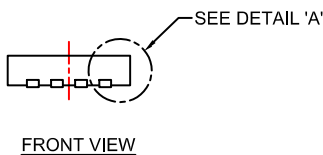


**WDFN8 3.3X3.3, 0.65P**  
**CASE 483AW**  
**ISSUE A**

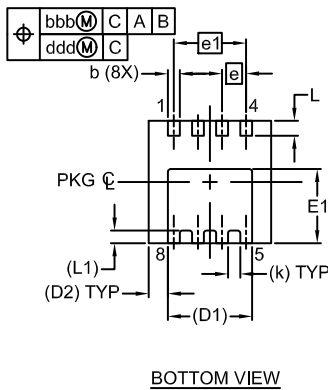
DATE 10 SEP 2019



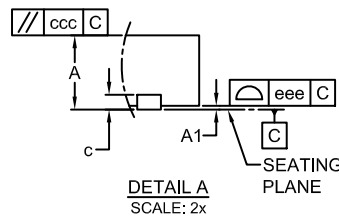
TOP VIEW



FRONT VIEW

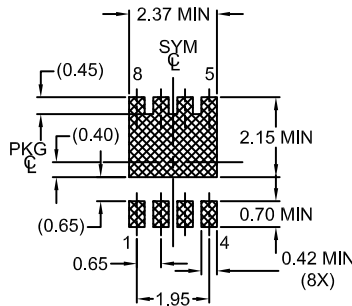


BOTTOM VIEW



DETAIL A  
SCALE: 2x

### LAND PATTERN RECOMMENDATION\*



### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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