

# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

150 V, 25 A, 34 mΩ

## FDMC86260

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Features

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)}$  = 34 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 5.4\text{ A}$
- Max  $R_{DS(on)}$  = 44 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 4.8\text{ A}$
- High Performance Technology for Extremely Low  $R_{DS(on)}$
- 100% UIL Tested
- Pb-Free, Halide Free and RoHS Compliant

### Applications

- DC-DC Conversion

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

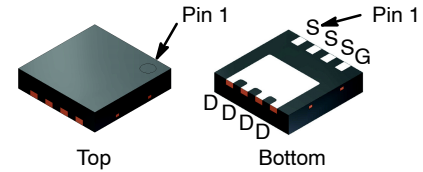
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current: Continuous, $T_C = 25^\circ\text{C}$ (Note 5) Continuous, $T_C = 100^\circ\text{C}$ (Note 5) Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed (Note 4)	25 16 5.4 135	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	121	mJ
$P_D$	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	54 2.3	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

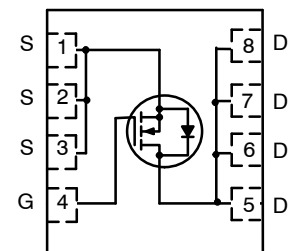
### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
150 V	34 mΩ @ 10 V	25 A
	44 mΩ @ 6 V	

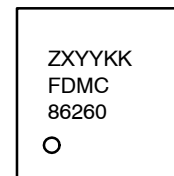


WDFN8 3.3 × 3.3, 0.65P  
CASE 483AW



N-CHANNEL MOSFET

### MARKING DIAGRAM



- Z = Assembly Plant Code
- XYY = 3-Digit Date Code Format
- KK = 2-Alphanumeric Lot Run Traceability Code
- FDMC86260 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
FDMC86260	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMC86260

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	150	–	–	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	110	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2	2.7	4	V
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–9	–	mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.4 A	–	27	34	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 4.8 A	–	31	44	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.4 A, T <sub>J</sub> = 125°C	–	55	69	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 5.4 A	–	19	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	1000	1330	pF
C <sub>oss</sub>	Output Capacitance		–	105	140	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	4.8	10	pF
R <sub>g</sub>	Gate Resistance		0.1	0.6	1.8	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 5.4 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	9.5	19	ns
t <sub>r</sub>	Rise Time		–	2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	17	30	ns
t <sub>f</sub>	Fall Time		–	3.3	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 75 V, I <sub>D</sub> = 5.4 A	–	15	21	nC
		V <sub>GS</sub> = 0 V to 6 V, V <sub>DD</sub> = 75 V, I <sub>D</sub> = 5.4 A	–	9.7	14	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 5.4 A	–	4.0	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 5.4 A	–	3.1	–	nC

# FDMC86260

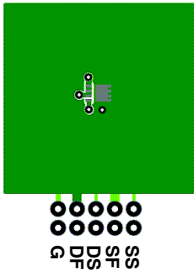
## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 5.4\text{ A}$ (Note 2)	–	0.77	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 1.9\text{ A}$ (Note 2)	–	0.72	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 5.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	–	64	102	ns
$Q_{rr}$	Reverse Recovery Charge		–	85	137	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**NOTES:**

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $53^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- $E_{AS}$  of 121 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 22\text{ A}$ .
- Pulsed  $I_d$  please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

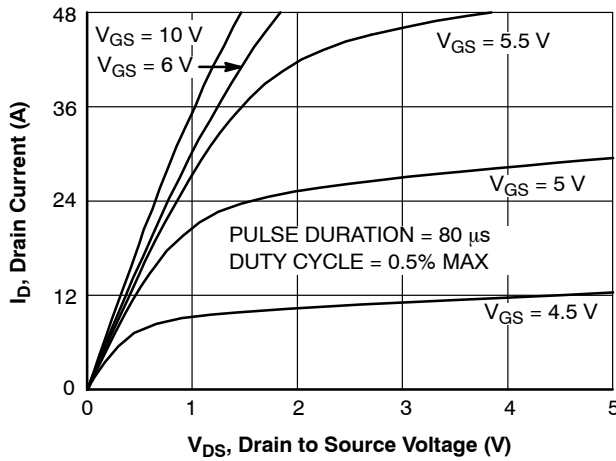


Figure 1. On-Region Characteristics

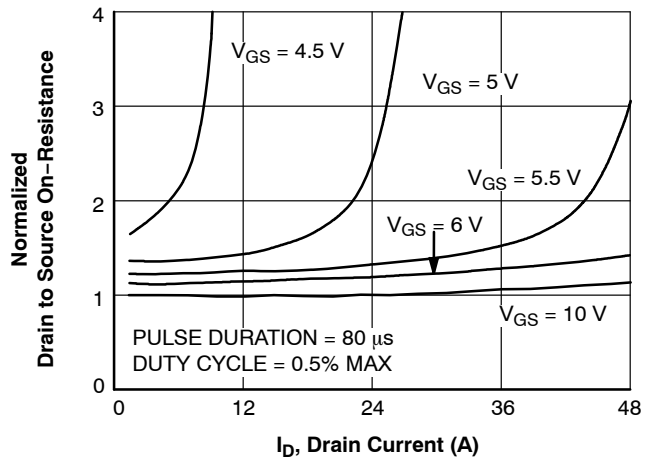


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

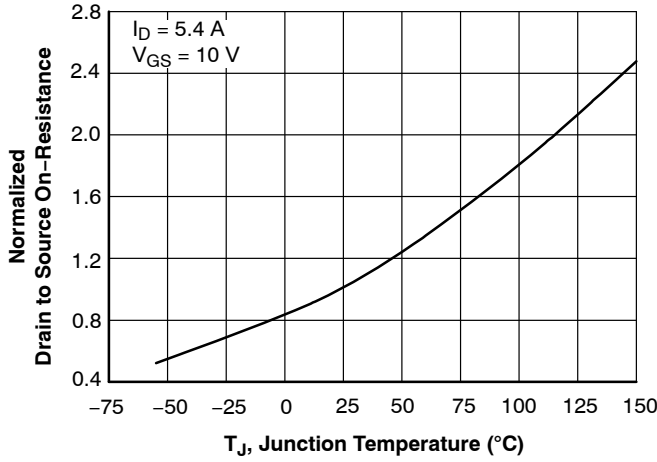


Figure 3. Normalized On-Resistance vs. Junction Temperature

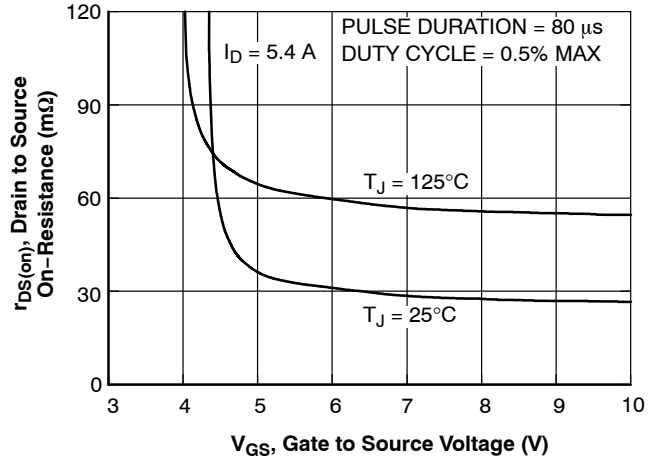


Figure 4. On-Resistance vs. Gate to Source Voltage

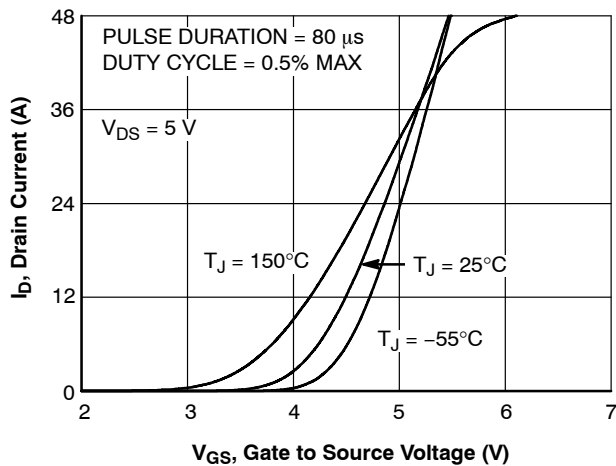


Figure 5. Transfer Characteristics

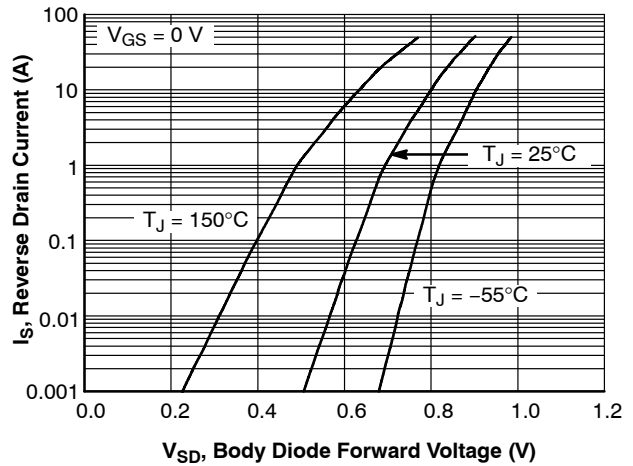


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

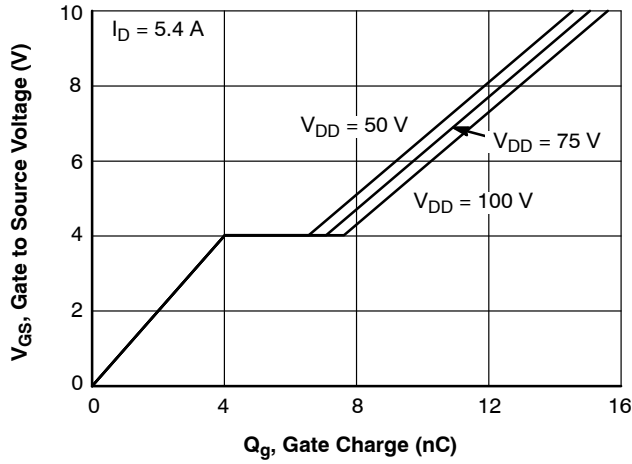


Figure 7. Gate Charge Characteristics

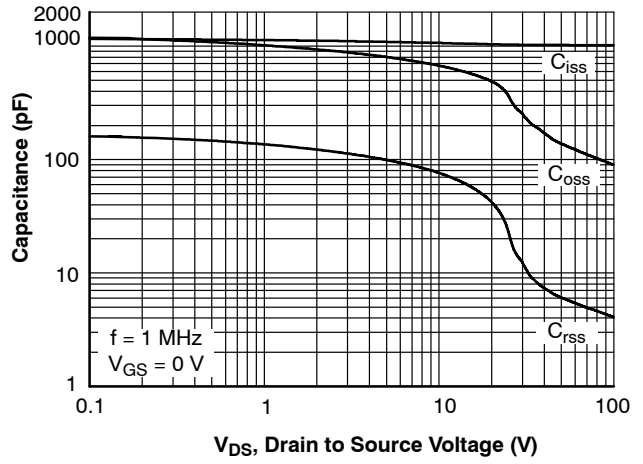


Figure 8. Capacitance vs. Drain to Source Voltage

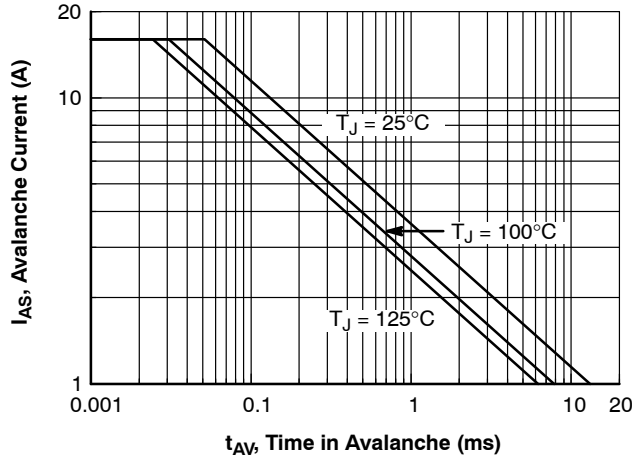


Figure 9. Unclamped Inductive Switching Capability

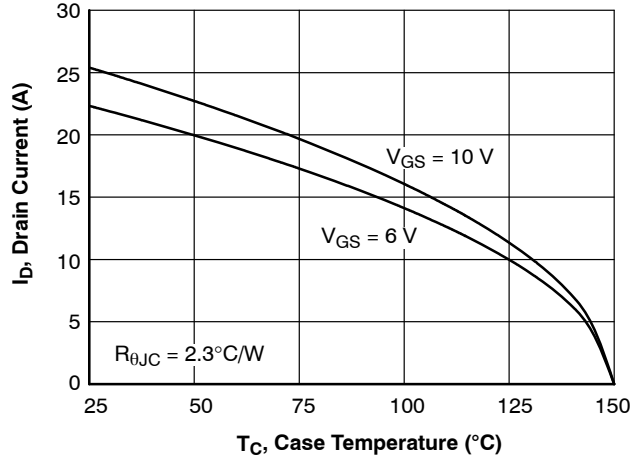


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

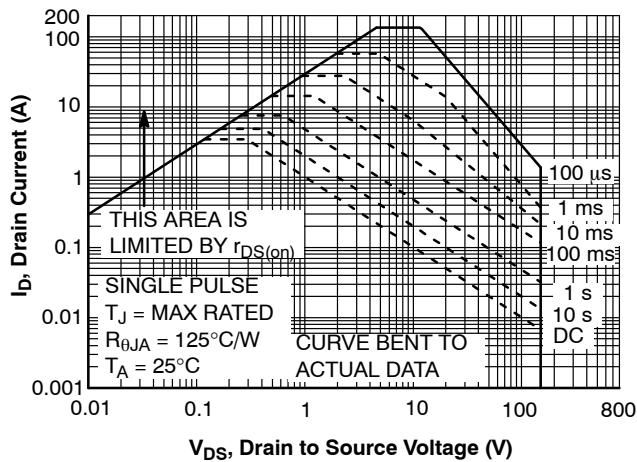


Figure 11. Forward Bias Safe Operating Area

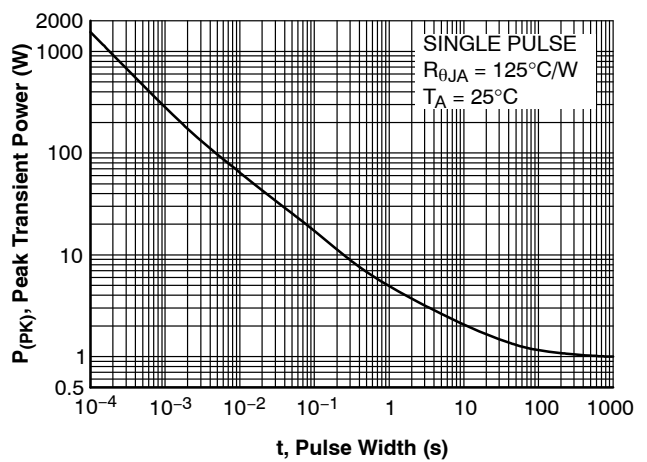


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

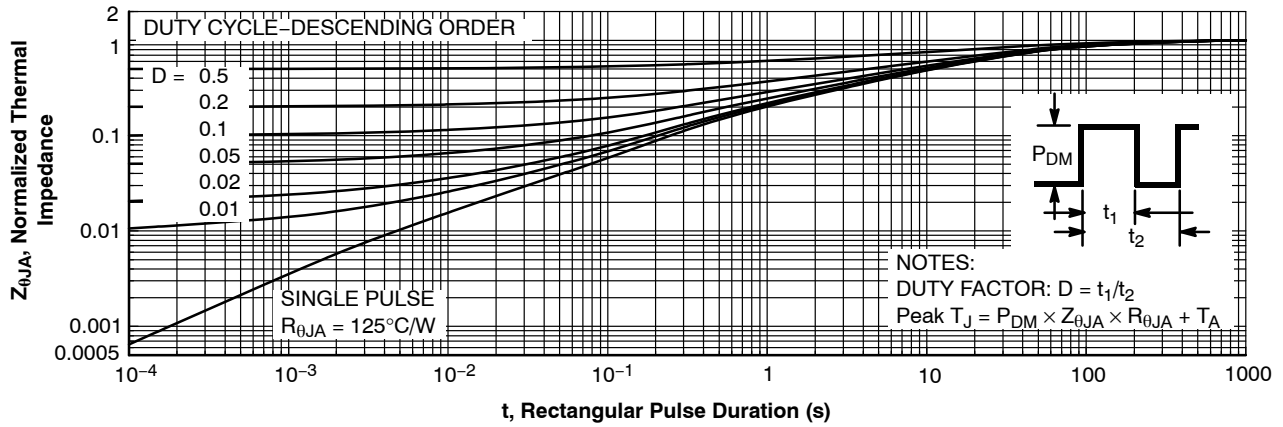
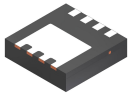


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

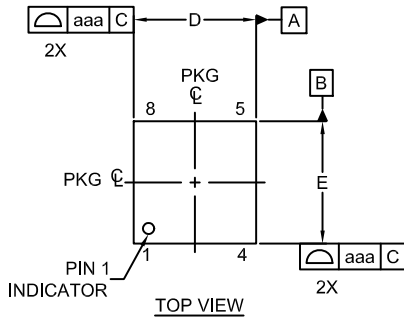
## PACKAGE DIMENSIONS

ON Semiconductor®

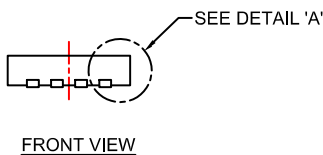


**WDFN8 3.3X3.3, 0.65P**  
**CASE 483AW**  
**ISSUE A**

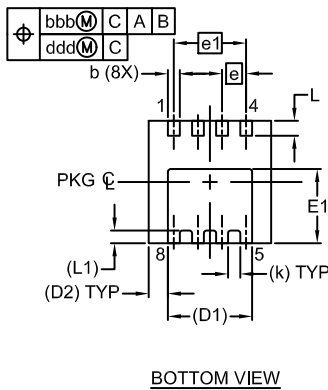
DATE 10 SEP 2019



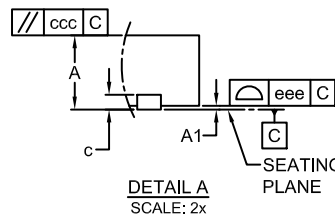
TOP VIEW



FRONT VIEW

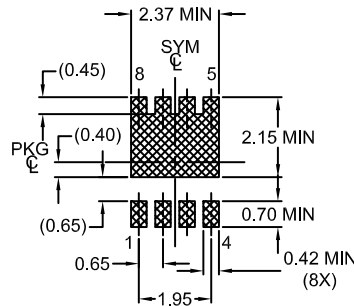


BOTTOM VIEW



DETAIL A  
SCALE: 2x

### LAND PATTERN RECOMMENDATION\*



### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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