

MOSFET – N-Channel, DUAL COOL[®] 33, POWERTRENCH[®] 40 V, 108 A, 2.5 mΩ

FDMC8321LDC

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $R_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Features

- DUAL COOL Top Side Cooling PQFN Package
- Max $R_{DS(on)}$ = 2.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 27\text{ A}$
- Max $R_{DS(on)}$ = 4.1 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 21\text{ A}$
- High Performance Technology for Extremely Low $R_{DS(on)}$
- This Device is Pb-Free, Halide Free and RoHS Compliant

Applications

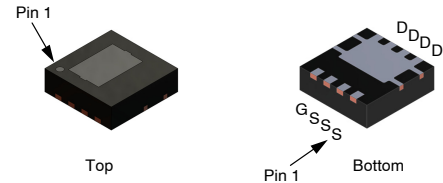
- Primary DC-DC Switch
- Motor Bridge Switch
- Synchronous Rectifier

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Rating	Unit
V_{DS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	Continuous $T_C = 25^\circ\text{C}$	108	A
		Continuous (Note 1a) $T_A = 25^\circ\text{C}$	27	
		Pulsed (Note 4)	320	
E_{AS}	Single Pulse Avalanche Energy (Note 3)		181	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	56	W
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

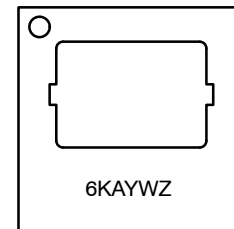
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
40 V	2.5 mΩ @ 10 V	108 A
	4.1 mΩ @ 4.5 V	



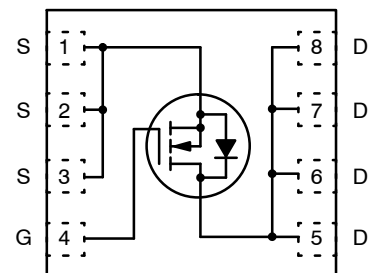
PQFN8 3.3X3.3, 0.65P
(DUAL COOL 33)
CASE 483AL

MARKING DIAGRAM



- 6K = Specific Device Code
- A = Assembly Plant Code
- YW = Date Code (Year and Week)
- Z = Lot Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

FDMC8321LDC

THERMAL CHARACTERISTICS

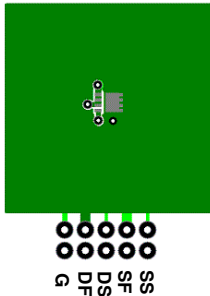
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	2.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	

THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	5.0	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	2.2	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	29	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	30	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	79	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	12	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	16	

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42°C/W when mounted on a 1 in² pad of 2 oz copper



b. 105°C/W when mounted on a minimum pad of 2 oz copper

- Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- 200FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- 200FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- 200FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- 200FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- E_{AS} of 181 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3$ mH, $I_{AS} = 11$ A, $V_{DD} = 40$ V, $V_{GS} = 10$ V, 100% tested at $L = 0.1$ mH, $I_{AS} = 35$ A.
- Pulse Id measured at 250 μs, refer to Figure 11 SOA graph for more details.

FDMC8321LDC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	40	–	–	V
$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	39	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–6	–	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 27 A	–	2.0	2.5	mΩ
		V _{GS} = 4.5 V, I _D = 21 A	–	2.8	4.1	
		V _{GS} = 10 V, I _D = 27 A, T _J = 125°C	–	3.0	3.8	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 27 A	–	126	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	–	2832	3965	pF
C _{oss}	Output Capacitance		–	777	1090	pF
C _{rss}	Reverse Transfer Capacitance		–	66	105	pF
R _g	Gate Resistance		0.1	0.7	2.5	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 20 V, I _D = 27 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	13	23	ns
t _r	Rise Time		–	5.5	11	
t _{d(off)}	Turn-Off Delay Time		–	31	50	
t _f	Fall Time		–	4.8	10	
Q _{g(TOT)}	Total Gate Charge at 10 V	V _{DD} = 20 V, I _D = 27 A	–	43	60	nC
Q _{g(TOT)}	Total Gate Charge at 5 V		–	22	31	
Q _{gs}	Gate to Source Charge		–	7.1	–	
Q _{gd}	Gate to Drain "Miller" Charge		–	6.1	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.3 A (Note 2)	–	0.7	1.2	V
		V _{GS} = 0 V, I _S = 27 A (Note 2)	–	0.8	1.3	
t _{rr}	Reverse Recovery Time	I _F = 27 A, di/dt = 100 A/μs	–	31	50	ns
Q _{rr}	Reverse Recovery Charge		–	11	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

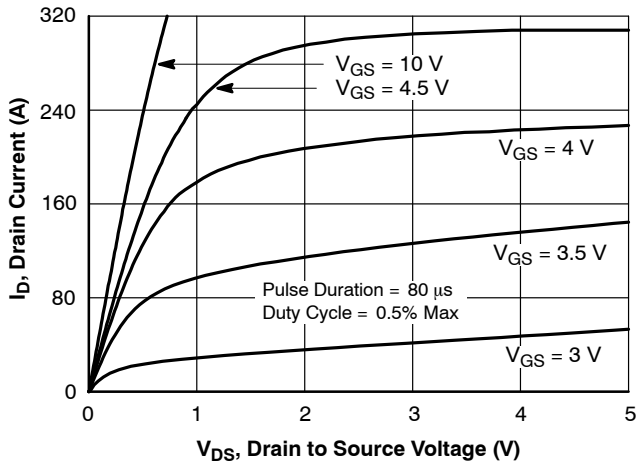


Figure 1. On Region Characteristics

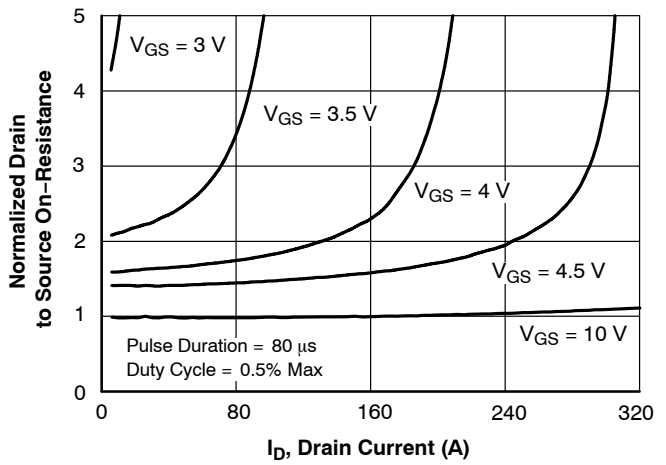


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

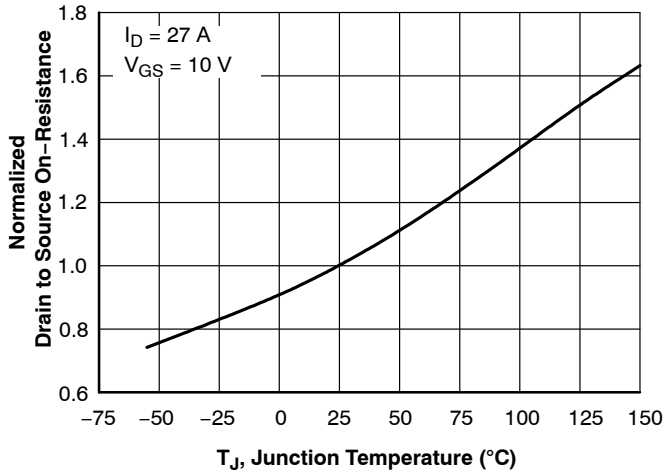


Figure 3. Normalized On Resistance vs. Junction Temperature

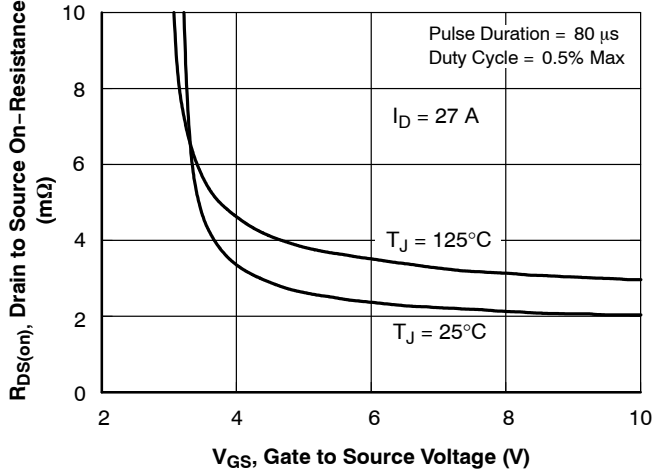


Figure 4. On-Resistance vs. Gate to Source Voltage

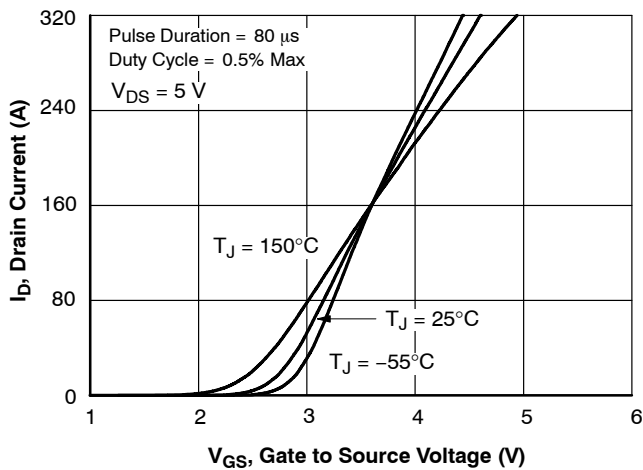


Figure 5. Transfer Characteristics

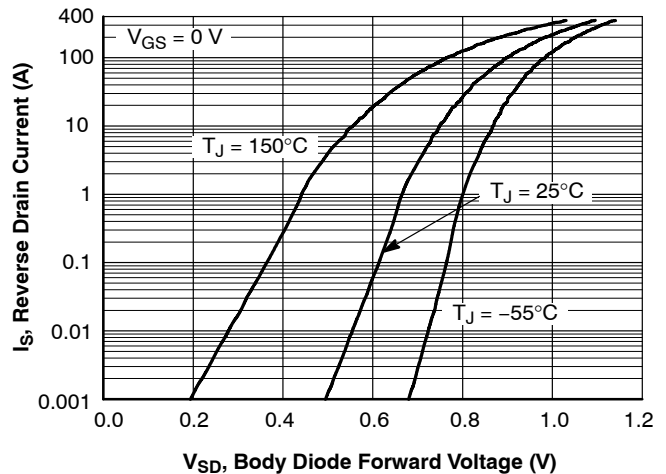


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

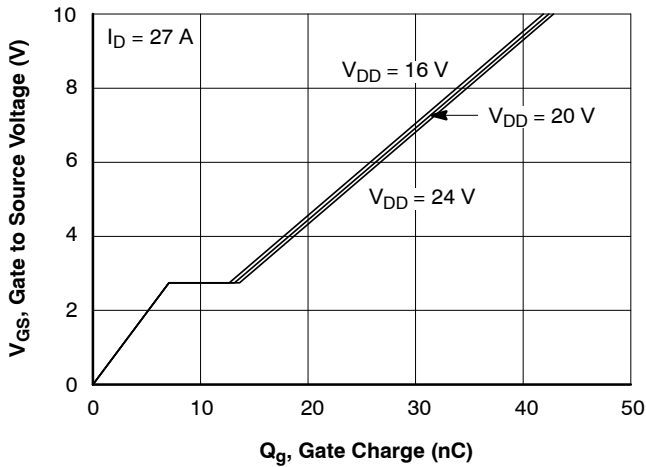


Figure 7. Gate Charge Characteristics

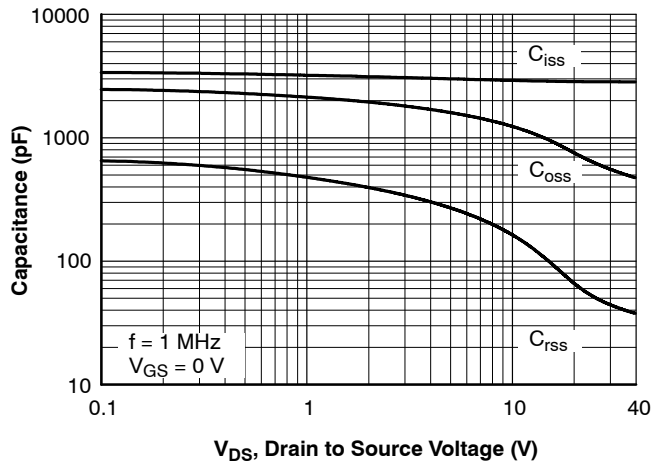


Figure 8. Capacitance vs. Drain to Source Voltage

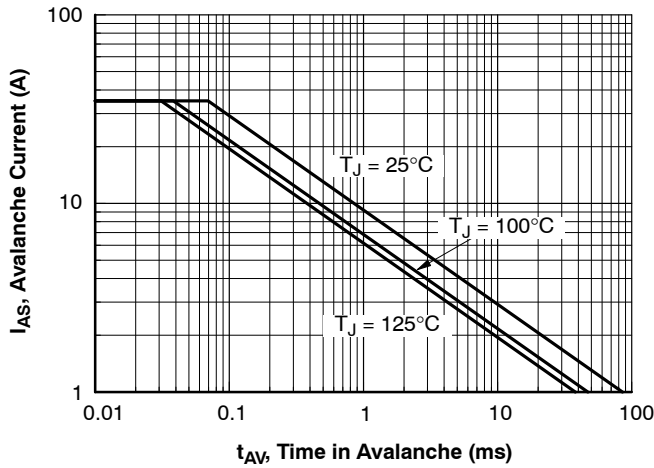


Figure 9. Unclamped Inductive Switching Capability

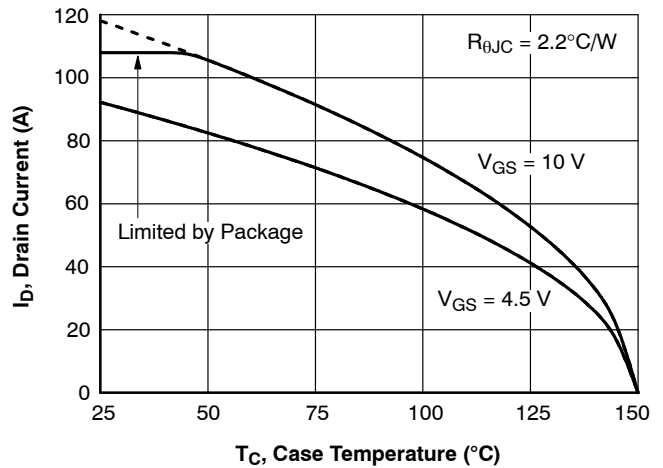


Figure 10. Maximum Continuous Drain Current vs Case Temperature

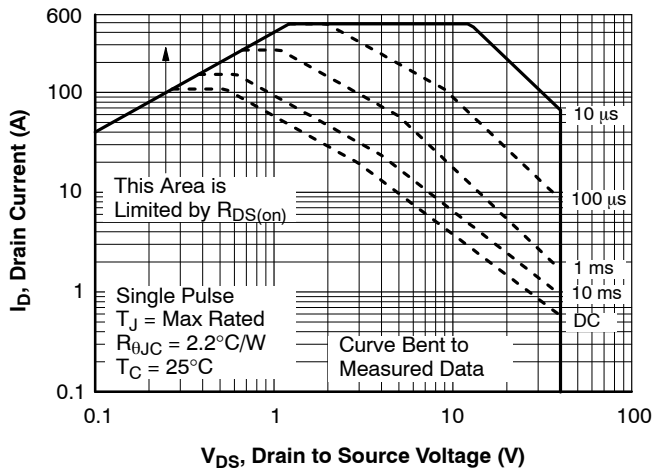


Figure 11. Forward Bias Safe Operating Area

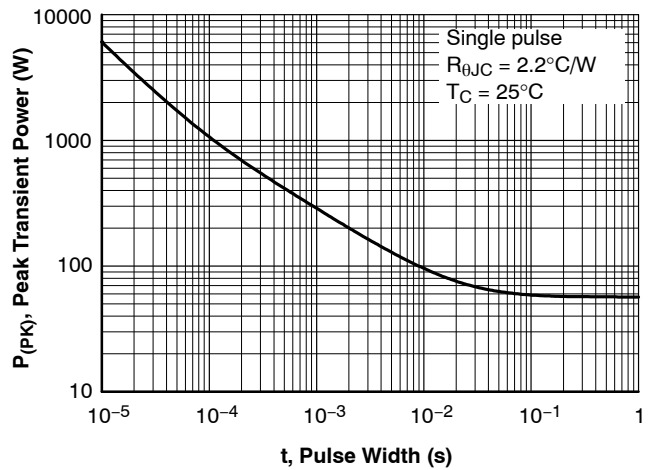


Figure 12. Single Pulse Maximum Power Dissipation

FDMC8321LDC

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

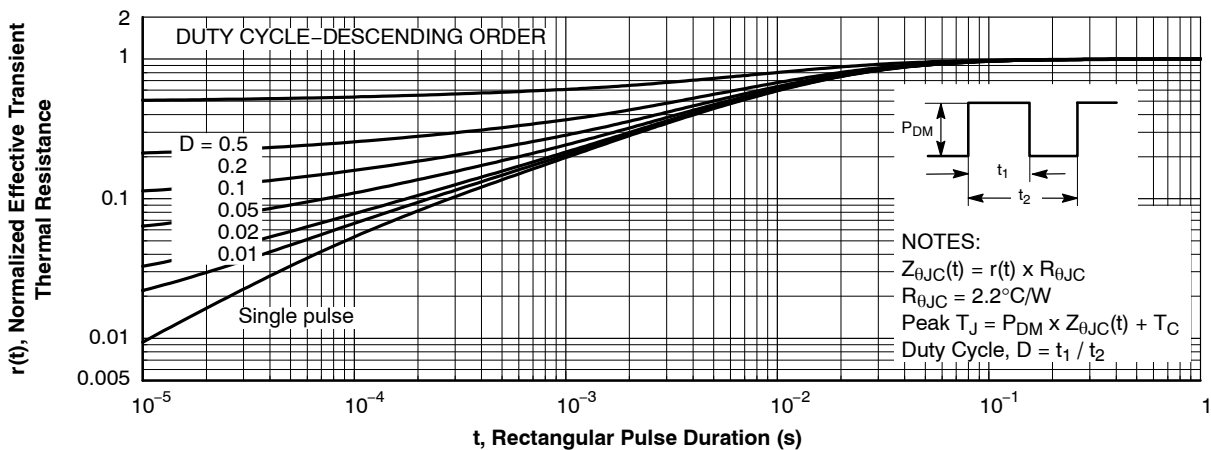


Figure 13. Junction-to-Case Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC8321LDC	6K	PQFN8 3.3 x 3.3, 0.65P (DUAL COOL 33) (Pb-Free/Halide Free)	13"	12 mm	3000 / Tape & Reel

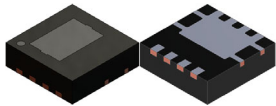
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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MECHANICAL CASE OUTLINE

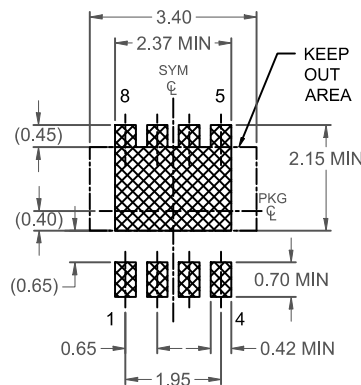
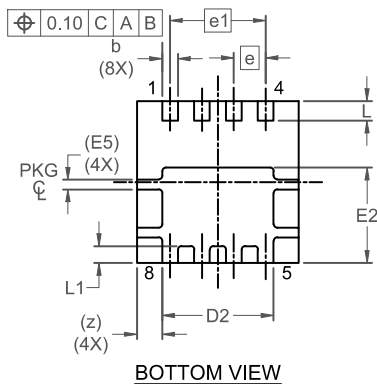
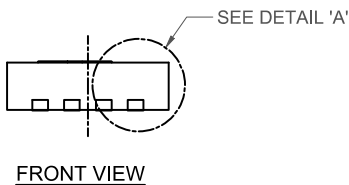
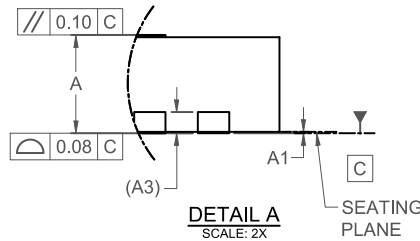
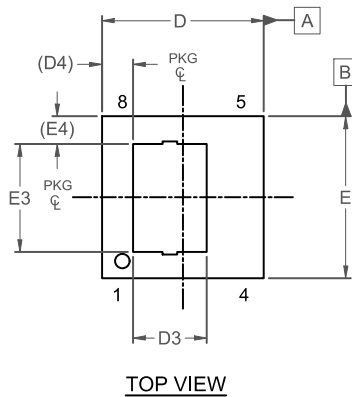
PACKAGE DIMENSIONS

ON Semiconductor®



PQFN8 3.3X3.3, 0.65P CASE 483AL ISSUE A

DATE 01 JUN 2021



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002 CONTROLLING
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.27	0.32	0.37
A3	0.20 REF		
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	1.40	1.55	1.70
D4	0.63 REF		
E	3.20	3.30	3.40
E2	1.90	2.00	2.10
E3	2.10	2.25	2.40
E4	0.56 REF		
E5	0.20 REF		
e	0.65 BSC		
e1	1.95 BSC		
L	0.30	0.40	0.50
L4	0.29	0.39	0.49
z	0.52 REF		

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