

MOSFET – P-Channel, POWERTRENCH®

-20 V, -18 A, 8.0 mΩ

FDMC510P

General Description

This P-Channel MOSFET is produced using onsemi's advanced POWERTRENCH® process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

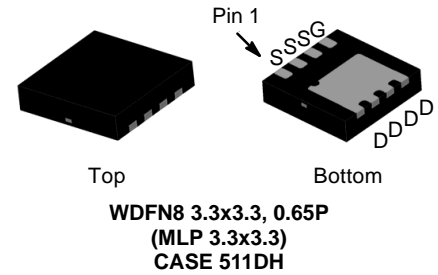
Features

- Max $r_{DS(on)}$ = 8.0 mΩ at $V_{GS} = -4.5$ V, $I_D = -12$ A
- Max $r_{DS(on)}$ = 9.8 mΩ at $V_{GS} = -2.5$ V, $I_D = -10$ A
- Max $r_{DS(on)}$ = 13 mΩ at $V_{GS} = -1.8$ V, $I_D = -9.3$ A
- Max $r_{DS(on)}$ = 17 mΩ at $V_{GS} = -1.5$ V, $I_D = -8.3$ A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- 100% UIL Tested
- HBM ESD Capability Level >2 kV Typical (Note 4)
- This Device is Pb-Free, Halide Free and is RoHS Compliant

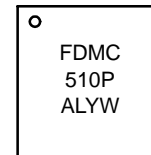
Applications

- Battery Management
- Load Switch

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
-20 V	8 mΩ @ -4.5 V	-18 A
	9.8 mΩ @ -2.5 V	
	13 mΩ @ -1.8 V	
	17 mΩ @ -1.5 V	

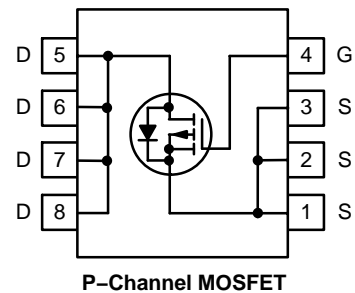


MARKING DIAGRAM



FDMC510P = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

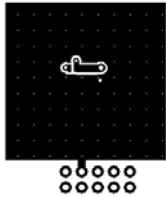
Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		-20	V
V_{GS}	Gate to Source Voltage		± 8	V
I_D	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	
		Pulsed		
E_{AS}	Single Pulse Avalanche Energy		37	mJ
P_D	Power Dissipation		$T_C = 25^\circ\text{C}$	W
	Power Dissipation (Note 1a)		$T_A = 25^\circ\text{C}$	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to + 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-12	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±8 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-0.4	-0.5	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	3	-	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -4.5 V, I _D = -12 A	-	6.4	8.0	mΩ
		V _{GS} = -2.5 V, I _D = -10 A	-	7.6	9.8	
		V _{GS} = -1.8 V, I _D = -9.3 A	-	9.2	13	
		V _{GS} = -1.5 V, I _D = -8.3 A	-	11	17	
		V _{GS} = -4.5 V, I _D = -12 A, T _J = 125°C	-	8.5	12	
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -12 A	-	75	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	5910	7860	pF
C _{oss}	Output Capacitance		-	840	1120	pF
C _{rss}	Reverse Transfer Capacitance		-	738	1110	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -10 V, I _D = -12 A, V _{GS} = -4.5 V, R _{GEN} = 6 Ω	-	15	27	ns
t _r	Rise Time		-	34	55	ns
t _{d(off)}	Turn-Off Delay Time		-	338	540	ns
t _f	Fall Time		-	170	272	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to -4.5 V, V _{DD} = -10 V, I _D = -12 A	-	83	116	nC
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to -2.5 V, V _{DD} = -10 V, I _D = -12 A	-	50	70	nC
Q _{gs}	Gate to Source Charge	V _{DD} = -10 V, I _D = -12 A	-	6.3	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	20.4	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -12 A (Note 2)	-	-0.70	-1.3	V
		V _{GS} = 0 V, I _S = -2 A (Note 2)	-	-0.53	-1.2	
t _{rr}	Reverse Recovery Time	I _F = -12 A, di/dt = 100 A/μs	-	35	57	ns
Q _{rr}	Reverse Recovery Charge		-	20	32	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; P-Ch: L = 3 mH, I_{AS} = -5 A, V_{DD} = -20 V, V_{GS} = -4.5 V.
4. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

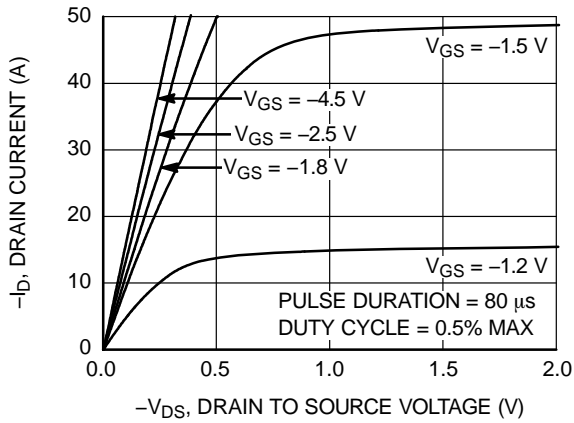


Figure 1. On Region Characteristics

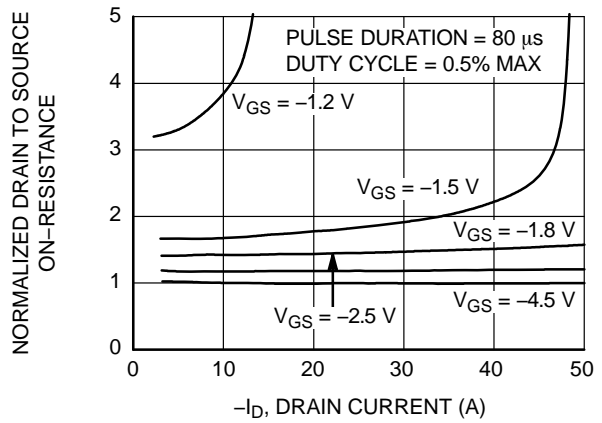


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

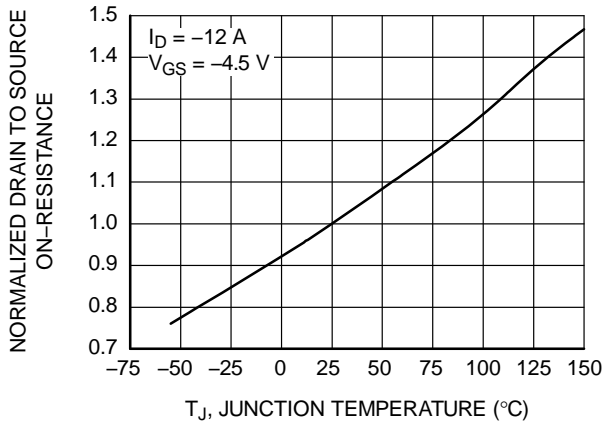


Figure 3. Normalized On Resistance vs. Junction Temperature

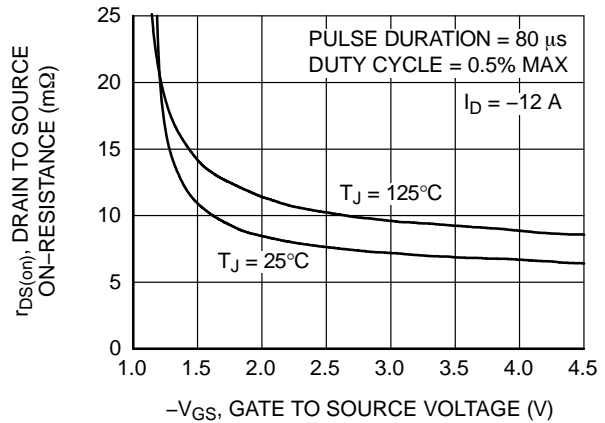


Figure 4. On-Resistance vs. Gate to Source Voltage

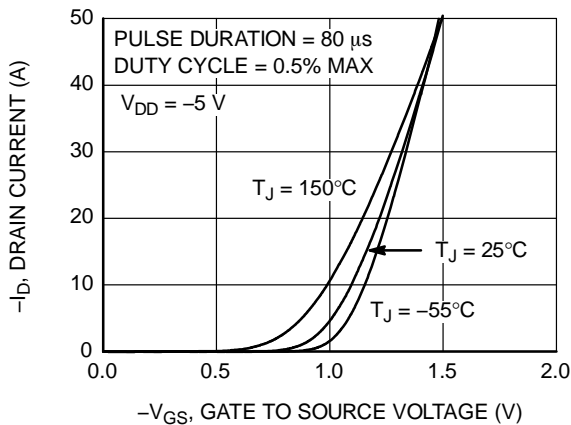


Figure 5. Transfer Characteristics

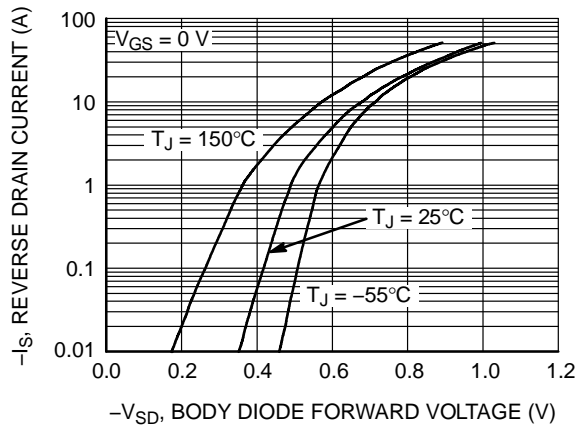


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

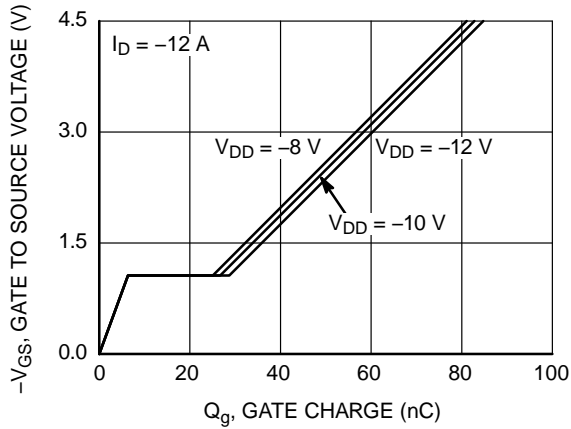


Figure 7. Gate Charge Characteristics

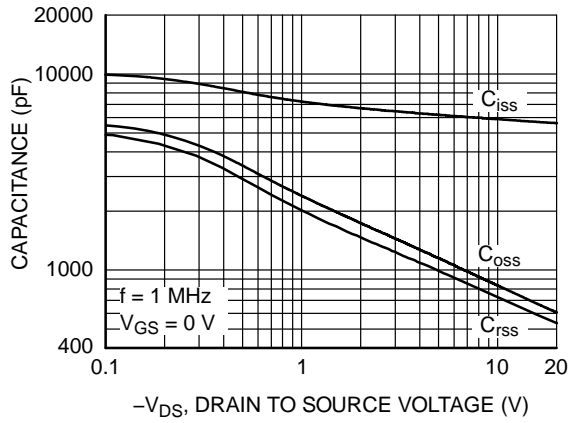


Figure 8. Capacitance vs. Drain to Source Voltage

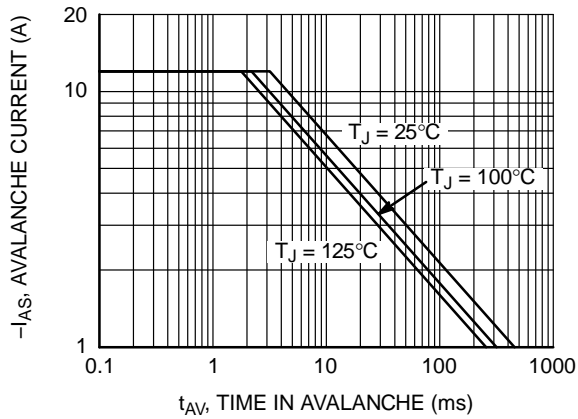


Figure 9. Unclamped Inductive Switching Capability

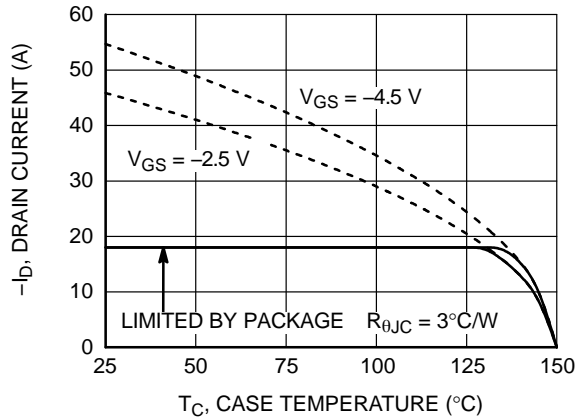


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

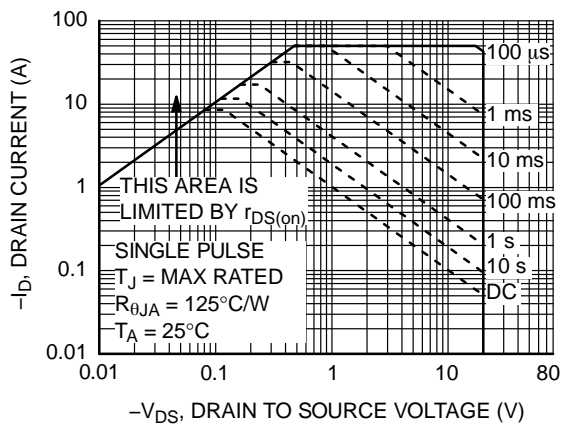


Figure 11. Forward Bias Safe Operating Area

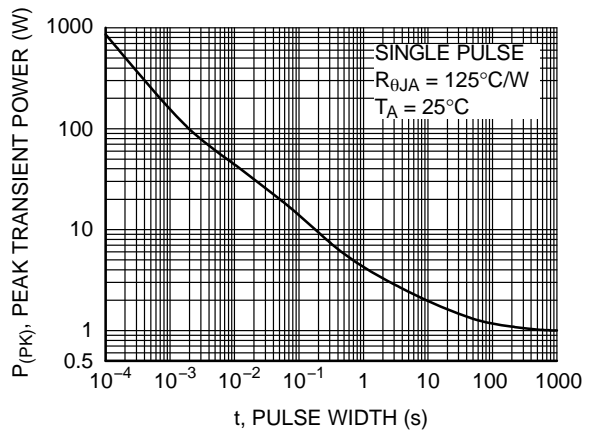


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

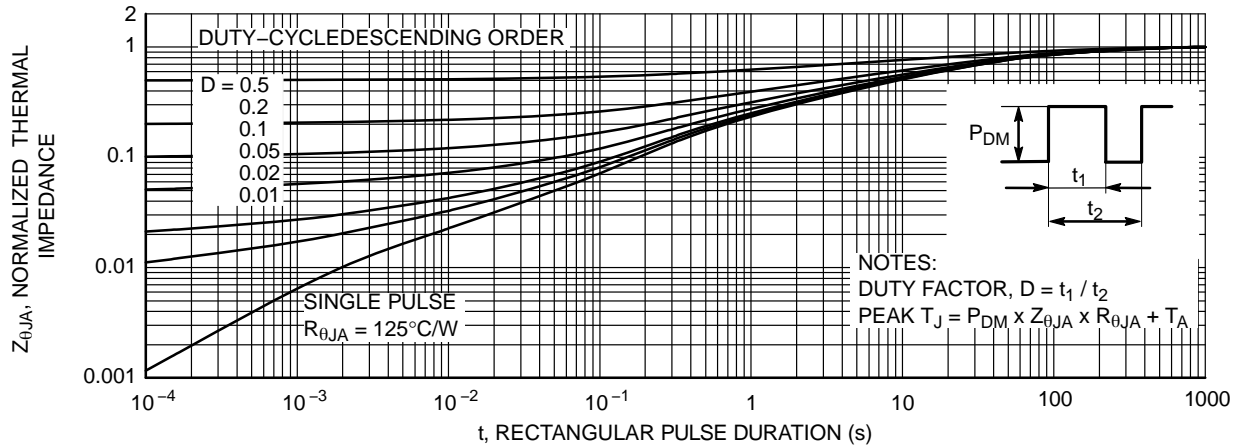


Figure 13. Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC510P	FDMC510P	WDFN8 3.3x3.3, 0.65P (MLP 3.3x3.3) (Pb-Free and Halide Free)	13"	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

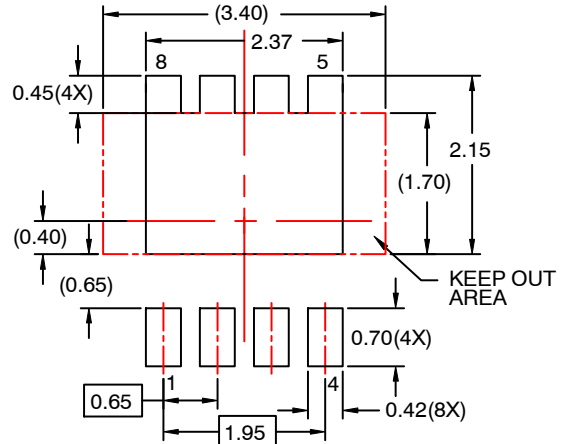
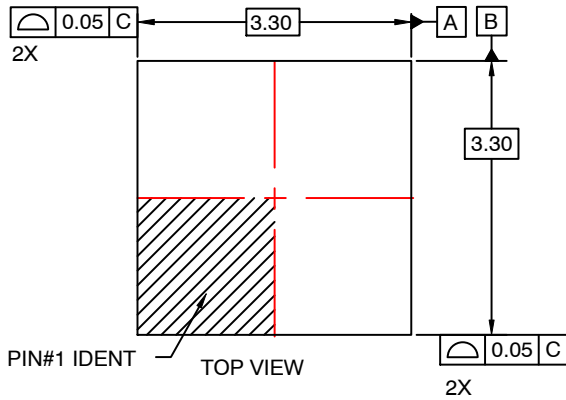
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

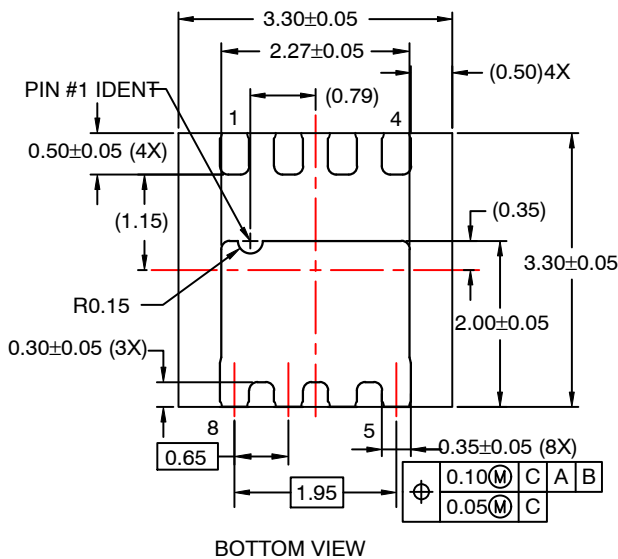
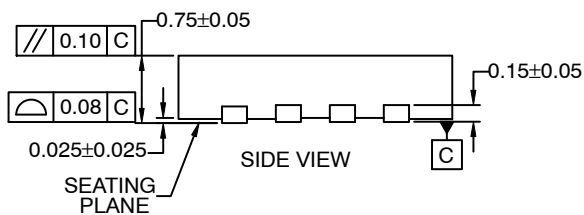
DATE 31 JUL 2016



RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW

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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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