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DATA SHEET
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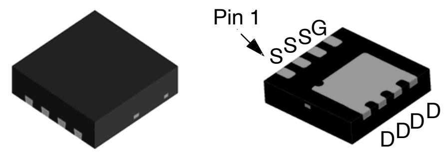
SyncFET™ – N-Channel, POWERTRENCH®

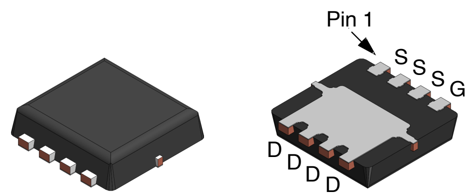
30 V, 21 A, 4.4 mΩ

FDMC0310AS, FDMC0310AS-F127

V_{DS} MAX	$r_{DS(on)}$ MAX	I_D MAX
30 V	4.4 mΩ @ 10 V	21 A
	5.2 mΩ @ 4.5 V	



WDFN8 3.3x3.3, 0.65P (MLP SAWN) CASE 511DH



WDFN8 3.3x3.3, 0.65P (MLP PUNCH) CASE 511DQ – Option C

General Description

The FDMC0310AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic schottky body diode.

Features

- Max $r_{DS(on)}$ = 4.4 mΩ at V_{GS} = 10 V, I_D = 19 A
- Max $r_{DS(on)}$ = 5.2 mΩ at V_{GS} = 4.5 V, I_D = 17.5 A
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- SyncFET Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

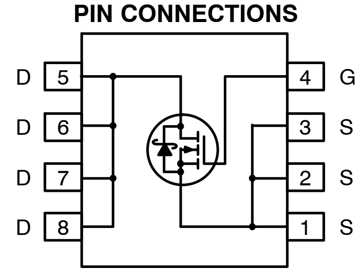
- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification

MARKING DIAGRAM

FDMC 0310AS ALYW	$Y&Z&2&K FDMC 0310AS

FDMC0310AS = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week
$Y = **onsemi** Logo
&Z = Assembly Plant Code
&2 = Numeric Date Code
&K = Lot Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		30	V
V_{DSt}	Drain to Source Transient Voltage ($t_{Transient}$ < 100 ns)		33	V
V_{GS}	Gate to Source Voltage (Note 1)		±20	V
I_D	Drain Current	Continuous, T_C = 25°C	21	A
		Continuous, T_A = 25°C (Note 3a)	19	A
		Pulsed	100	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)		66	mJ
P_D	Power Dissipation	T_C = 25°C	36	W
		T_A = 25°C (Note 3a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

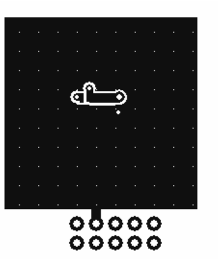
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
2. E_{AS} of 66 mJ is based on starting T_J = 25°C, L = 0.3 mH, I_{AS} = 21 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% tested at L= 3 mH, I_{AS} = 10.2 A.

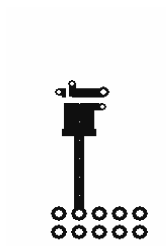
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3a)	53	

3. $R_{\theta JA}$ is determined with the device mounted on a 1 in2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C	–	26	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C	–	–5	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 19 A	–	3.8	4.4	mΩ
		V_{GS} = 4.5 V, I_D = 17.5 A	–	4.5	5.2	
		V_{GS} = 10 V, I_D = 19 A, T_J = 125°C	–	4.5	5.8	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 19 A	–	106	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	2380	3165	pF
C_{oss}	Output Capacitance		–	885	1175	pF
C_{rss}	Reverse Transfer Capacitance		–	100	150	pF
R_g	Gate Resistance		0.1	0.7	2.5	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 19 A V_{GS} = 10 V, R_{GEN} = 6 Ω	–	11	20	ns
t_r	Rise Time		–	5	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	30	48	ns
t_f	Fall Time		–	4	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V V_{DD} = 15 V, I_D = 19 A	–	37	52	nC
		V_{GS} = 0 V to 4.5 V V_{DD} = 15 V, I_D = 19 A	–	18	25	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 19 A	–	6	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	6	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 4)	–	0.6	0.8	V
		V_{GS} = 0 V, I_S = 19 A (Note 4)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 19 A, di/dt = 300 A/μs	–	29	47	ns
Q_{rr}	Reverse Recovery Charge		–	33	53	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

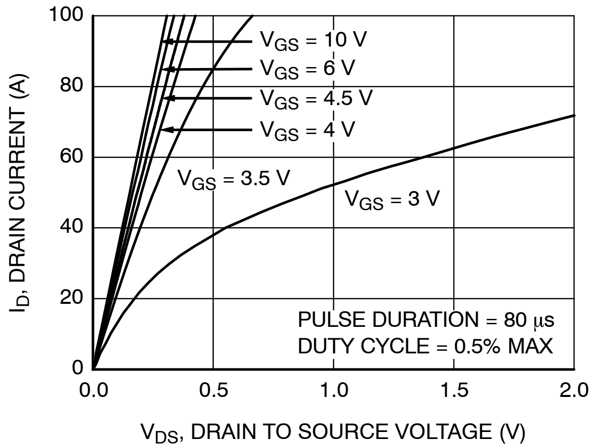


Figure 1. On Region Characteristics

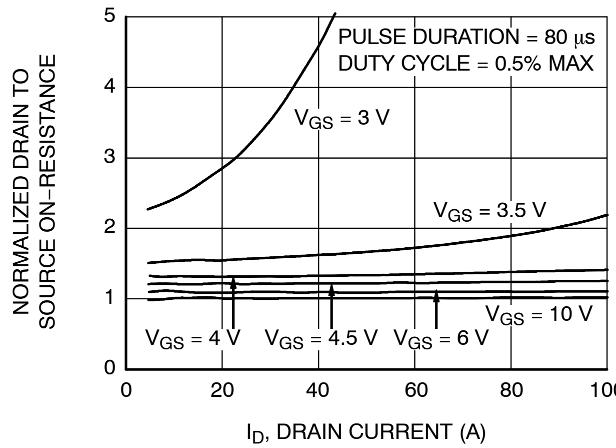


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

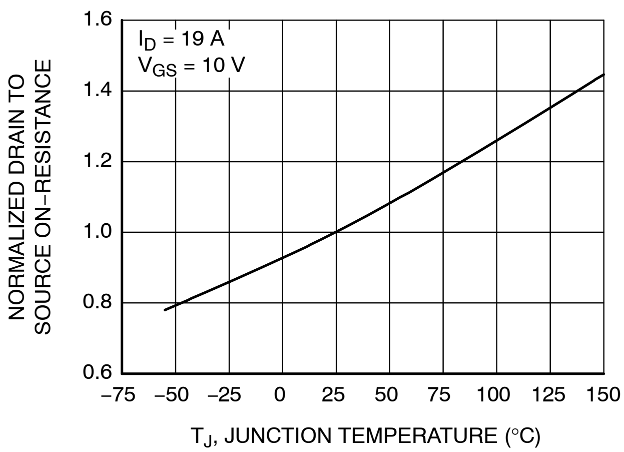


Figure 3. Normalized On−Resistance vs. Junction Temperature

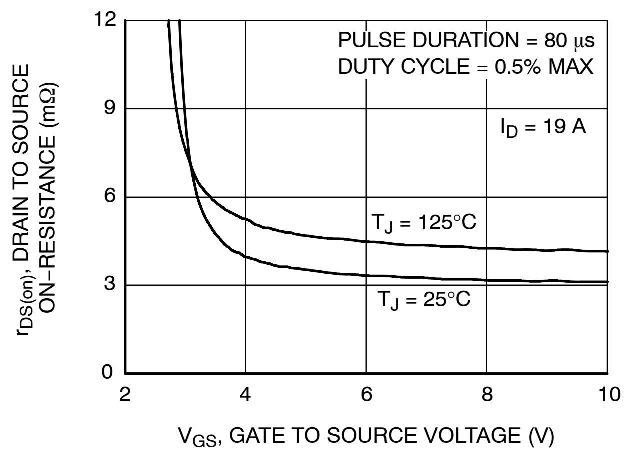


Figure 4. On−Resistance vs. Gate to Source Voltage

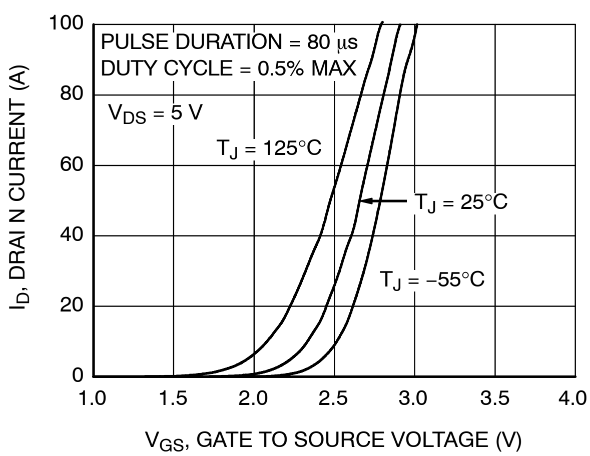


Figure 5. Transfer Characteristics

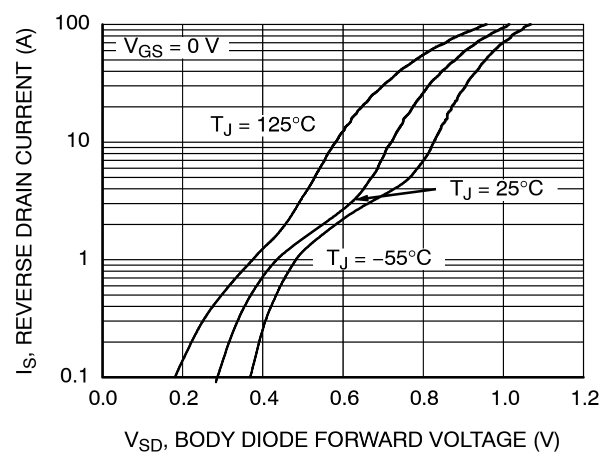


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted) (continued)

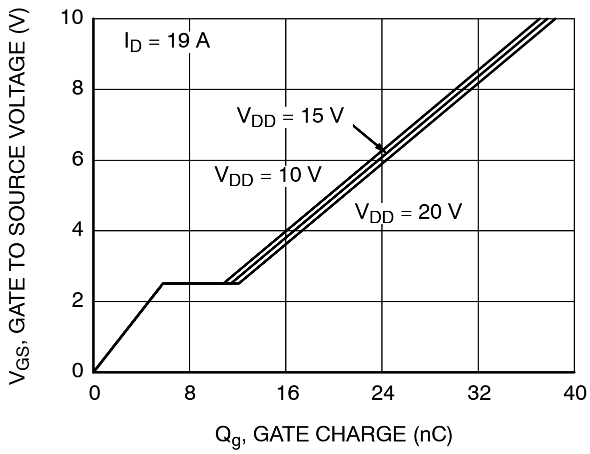


Figure 7. Gate Charge Characteristics

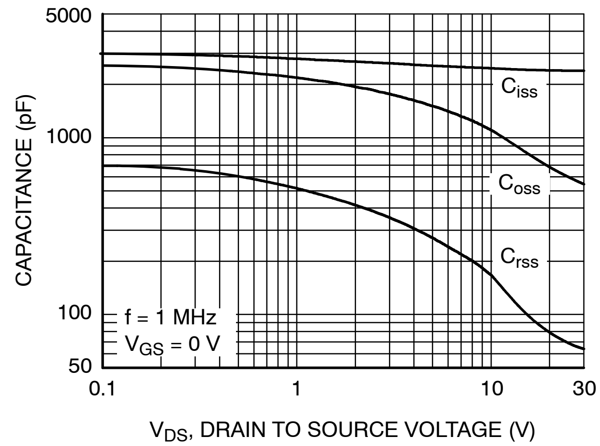


Figure 8. Capacitance vs. Drain to Source Voltage

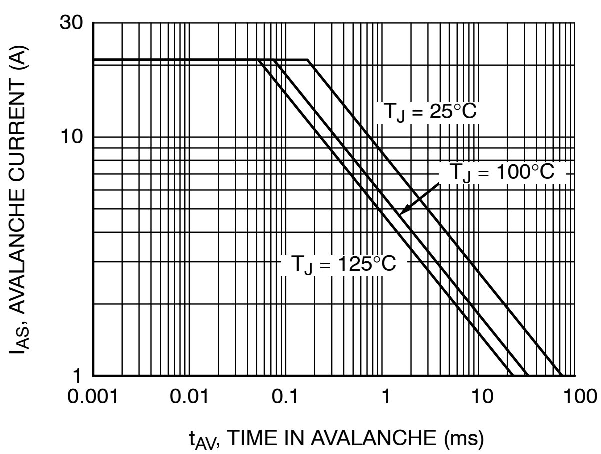


Figure 9. Unclamped Inductive Switching Capability

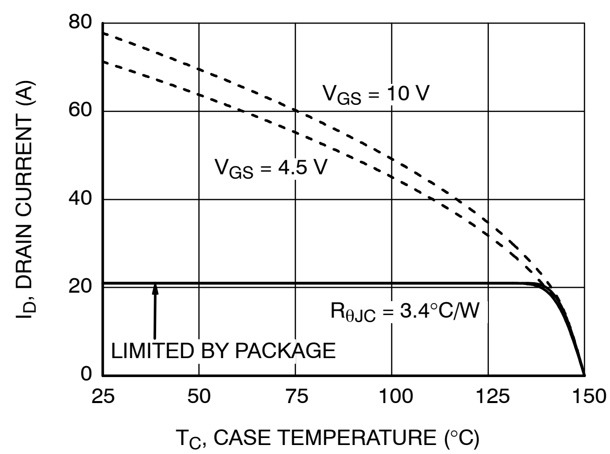


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

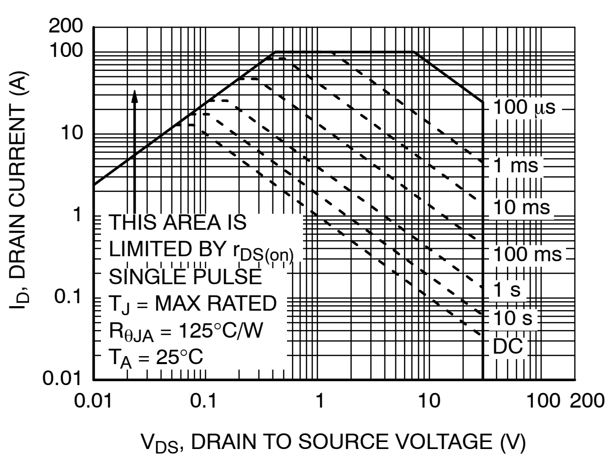


Figure 11. Forward Bias Safe Operating Area

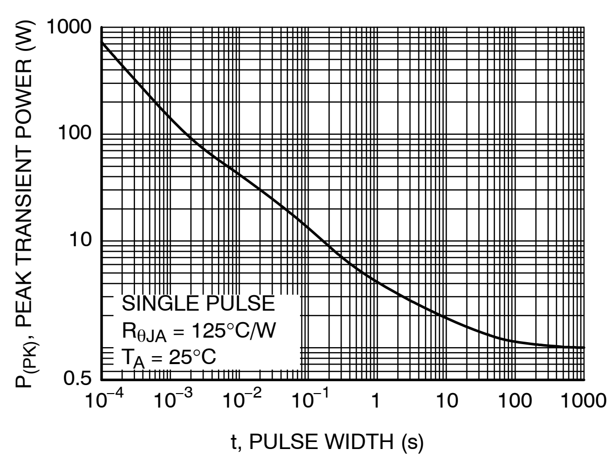


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted) (continued)

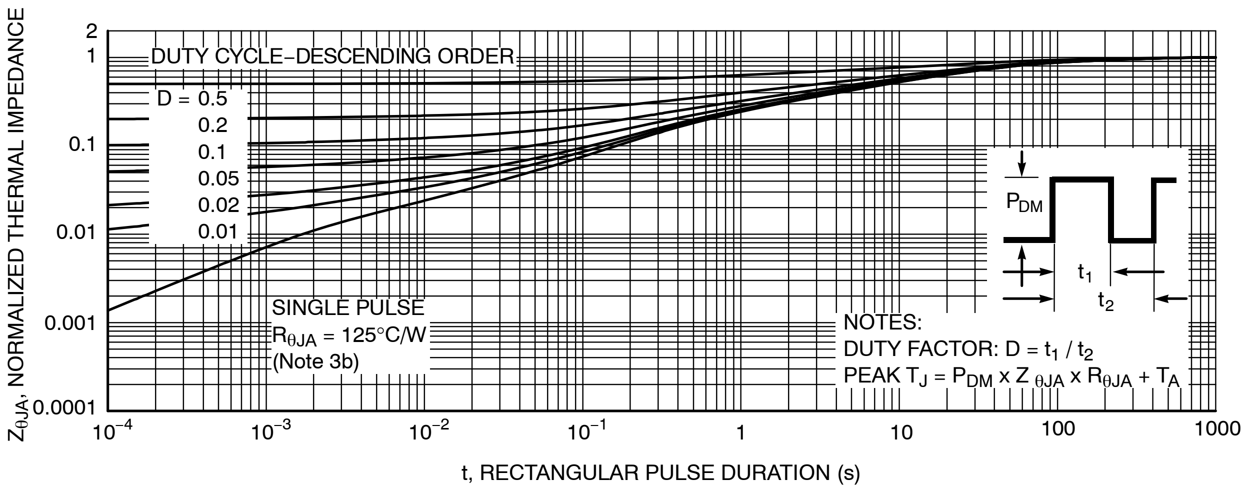


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMC0310AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

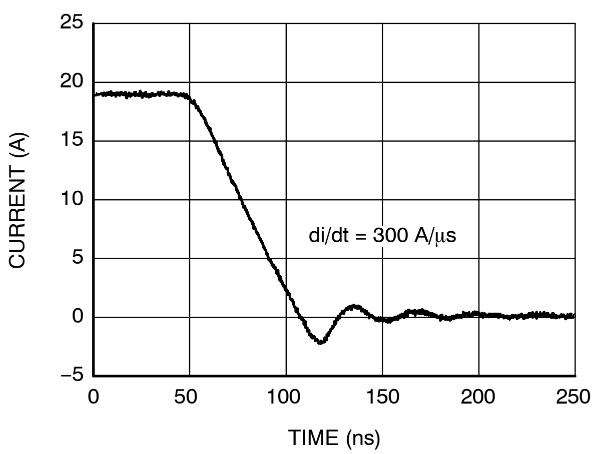


Figure 14. SyncFET Body Diode Reverse Recovery Characteristics

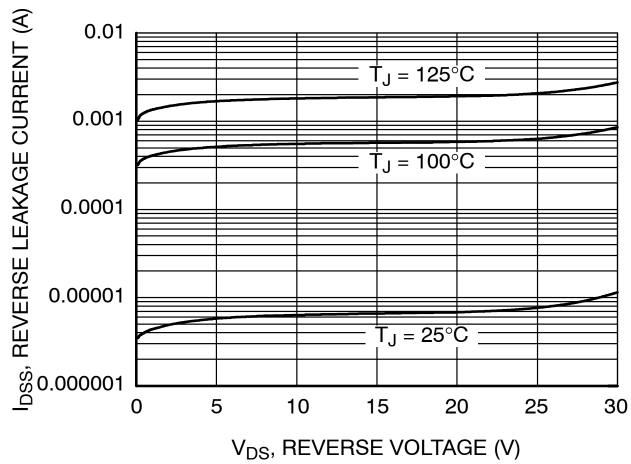


Figure 15. SyncFET Body Diode Reverse Leakage vs. Drain−Source Voltage

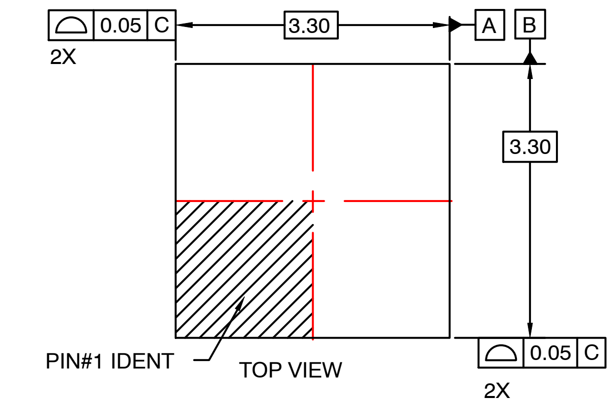
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMC0310AS	FDMC0310AS	WDFN8 3.3x3.3, 0.65P MLP (SAWN) (Pb−Free)	13”	12 mm	3000 / Tape & Reel
FDMC0310AS−F127	FDMC0310AS	WDFN8 3.3x3.3, 0.65P MLP (PUNCH) (Pb−Free)	13”	12 mm	3000 / Tape & Reel

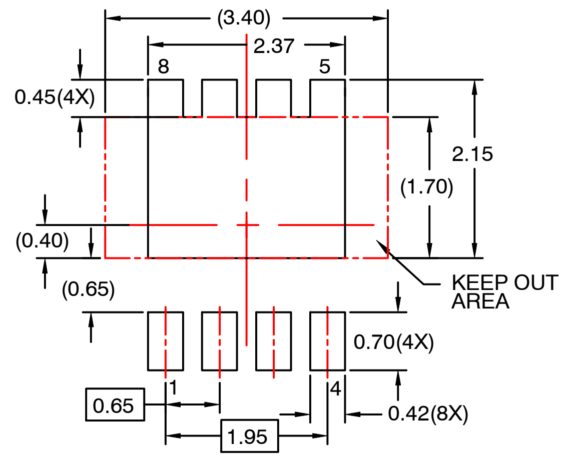
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

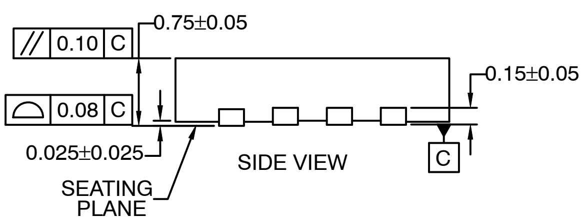
DATE 31 JUL 2016



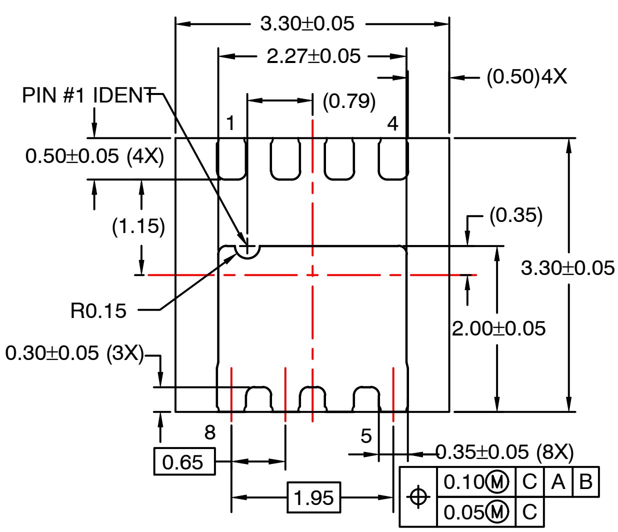
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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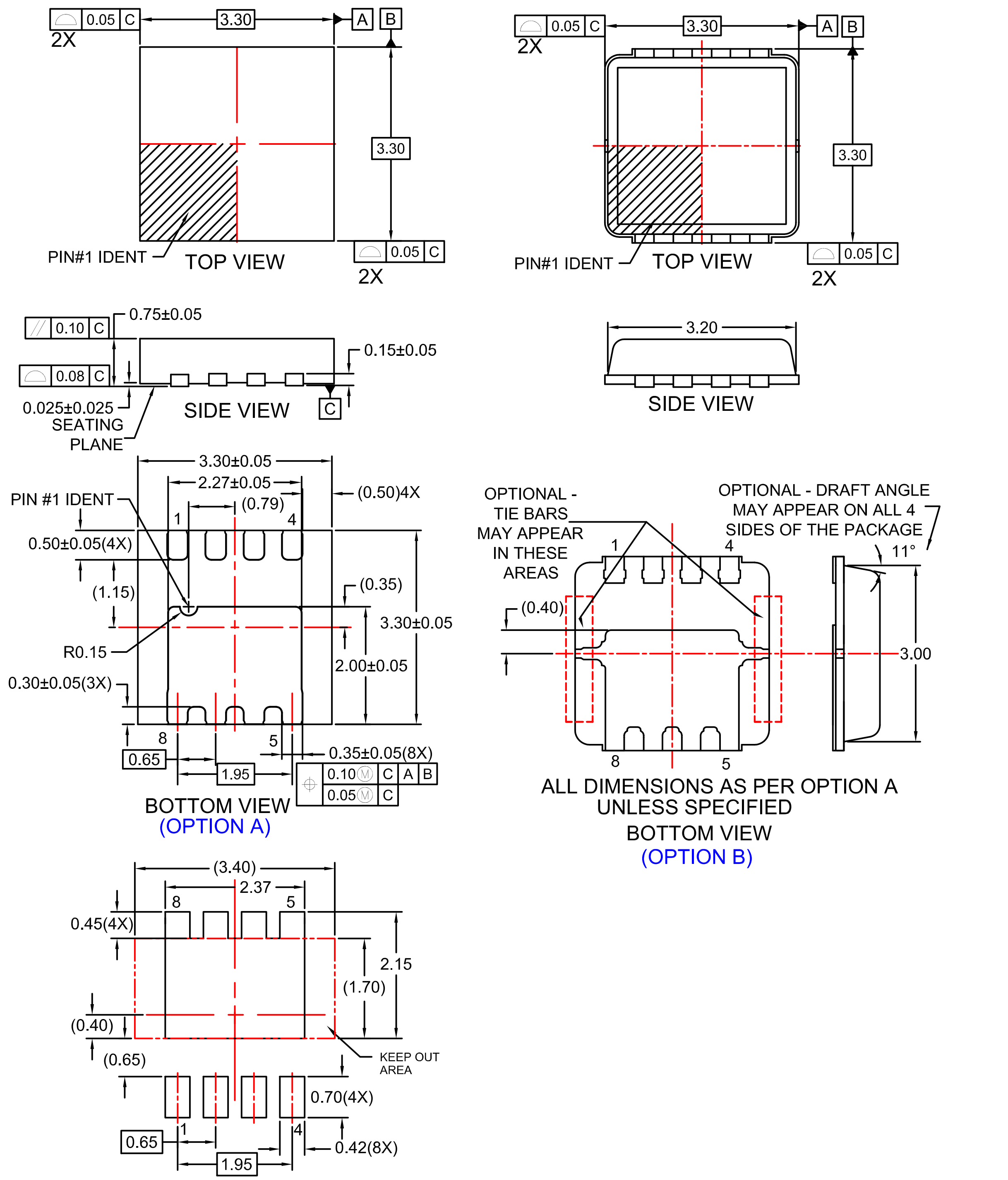
CASE 511DQ
ISSUE O

DATE 31 OCT 2016



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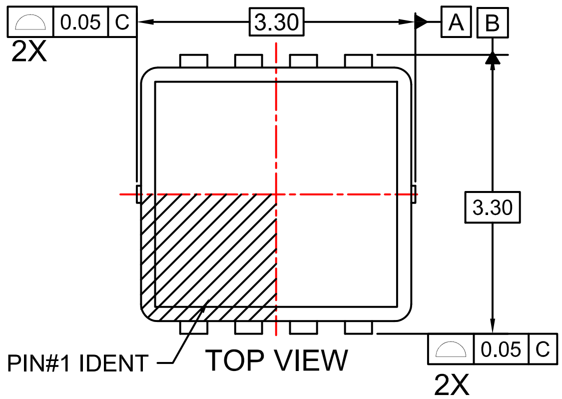
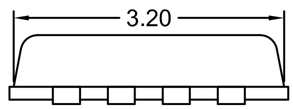
CASE 511DQ
ISSUE O

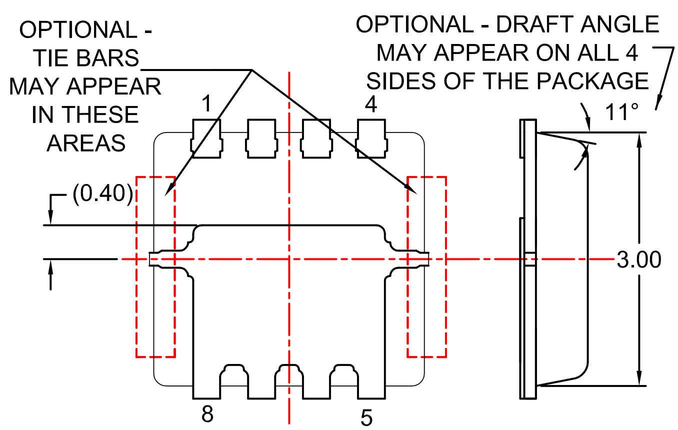
DATE 31 OCT 2016



TOP VIEW



SIDE VIEW



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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