

MOSFET – Single N-Channel, POWERTRENCH®

30 V, 9.0 A, 21 mΩ

FDMA7672

General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $R_{DS(on)}$ and gate charge provide excellent switching performance.

Features

- Max $R_{DS(on)}$ = 21 mΩ @ $V_{GS} = 10\text{ V}$, $I_D = 9.0\text{ A}$
- Max $R_{DS(on)}$ = 32 mΩ @ $V_{GS} = 4.5\text{ V}$, $I_D = 7\text{ A}$
- Low Profile – 0.8 mm Maximum – in the New Package MicroFET™ 2x2 mm
- This Device is Pb-Free, Halide Free and RoHS Compliant

Applications

- DC-DC Buck Converters

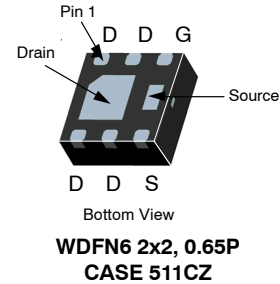
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	30	V
V_{GSS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous (Note 1a) $T_A = 25^\circ\text{C}$ – Pulsed	9 24	A
P_D	Power Dissipation (Note 1a) $T_A = 25^\circ\text{C}$ Power Dissipation (Note 1b) $T_A = 25^\circ\text{C}$	2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

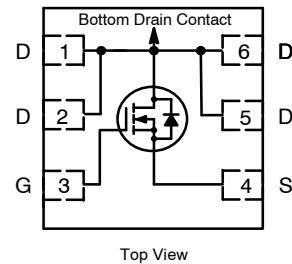
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

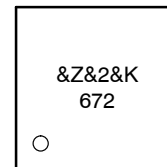
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	



PIN CONNECTIONS

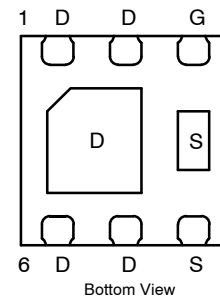


MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code (Year and Week)
- &K = 2-Digit Lot Run Code
- 672 = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDMA7672

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	–	16	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.0	2.1	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	–	–6	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 9.0 \text{ A}$	–	14	21	m Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$	–	20	32	
		$V_{GS} = 10 \text{ V}, I_D = 9 \text{ A}, T_J = 125^\circ\text{C}$	–	19	28	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 9.0 \text{ A}$	–	35	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	–	570	760	pF
C_{oss}	Output Capacitance		–	195	260	
C_{rss}	Reverse Transfer Capacitance		–	25	40	
R_G	Gate Resistance		–	1.5	–	

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_D = 9.0 \text{ A}$, $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	–	6	12	ns
t_r	Rise Time		–	2	10	
$t_{d(off)}$	Turn-Off Delay Time		–	14	25	
t_f	Fall Time		–	2	10	
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}, V_{DD} = 15 \text{ V}$, $I_D = 9.0 \text{ A}$	–	9.3	13	nC
		$V_{GS} = 0 \text{ V to } 4.5 \text{ V}, V_{DD} = 15 \text{ V}$, $I_D = 9.0 \text{ A}$	–	4.4	6	
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 15 \text{ V}, I_D = 9.0 \text{ A}$	–	1.9	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	1.5	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain-Source Diode Forward Current			2	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.0 \text{ A}$ (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 9.0 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	–	18	32	ns
Q_{rr}	Reverse Recovery Charge		–	5	10	nC

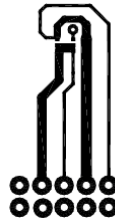
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) $52^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz. copper.



b) $145^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

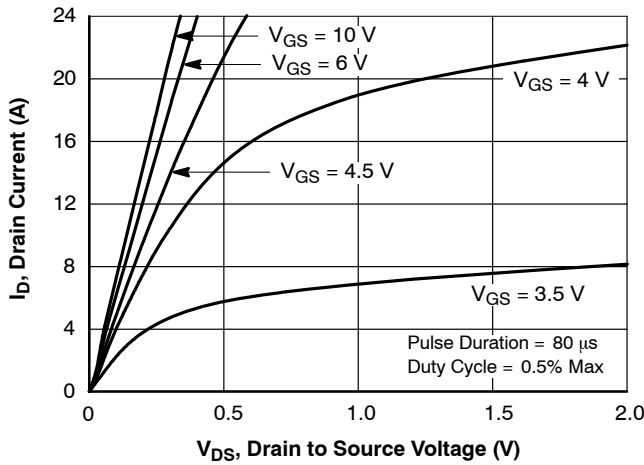


Figure 1. On-Region Characteristics

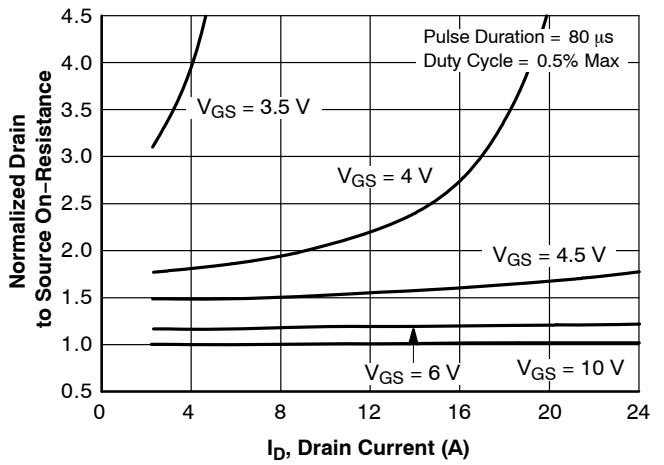


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

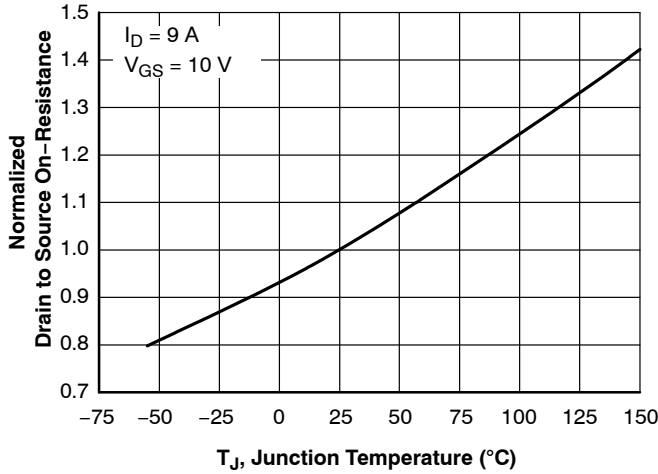


Figure 3. Normalized On-Resistance vs. Junction Temperature

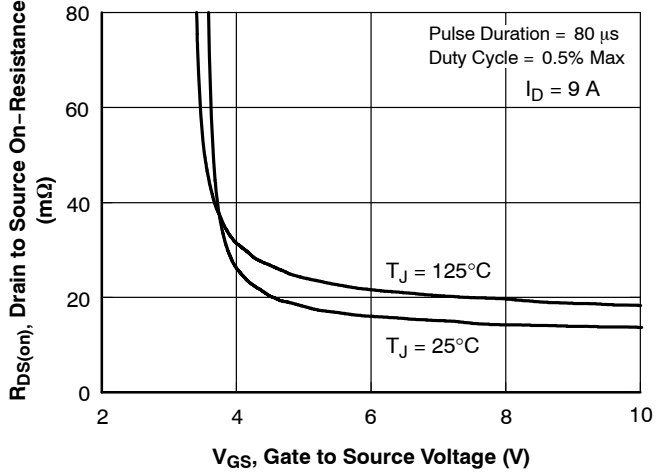


Figure 4. On-Resistance vs. Gate to Source Voltage

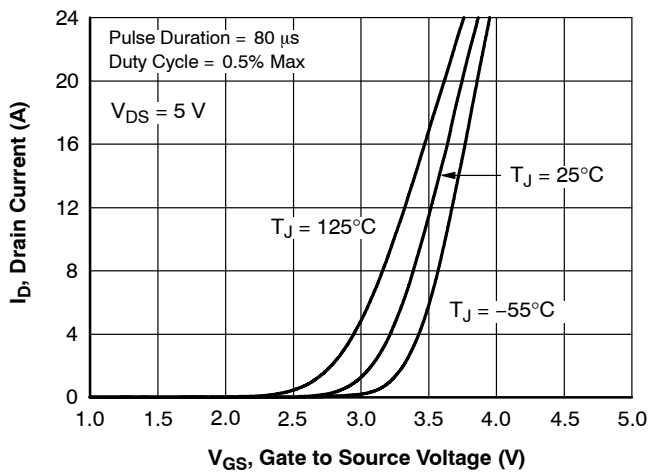


Figure 5. Transfer Characteristics

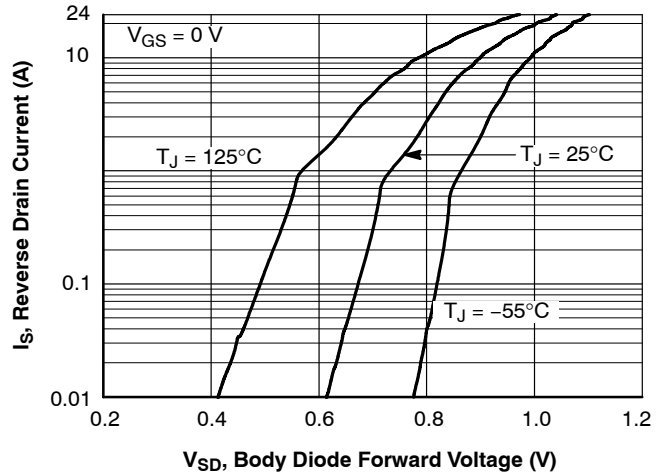


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

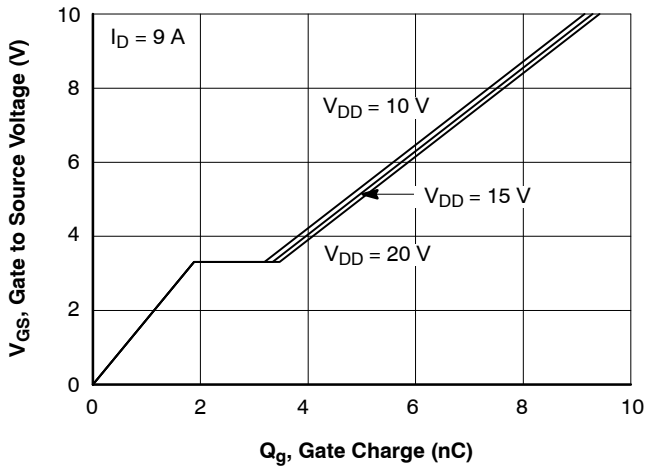


Figure 9. Gate Charge Characteristics

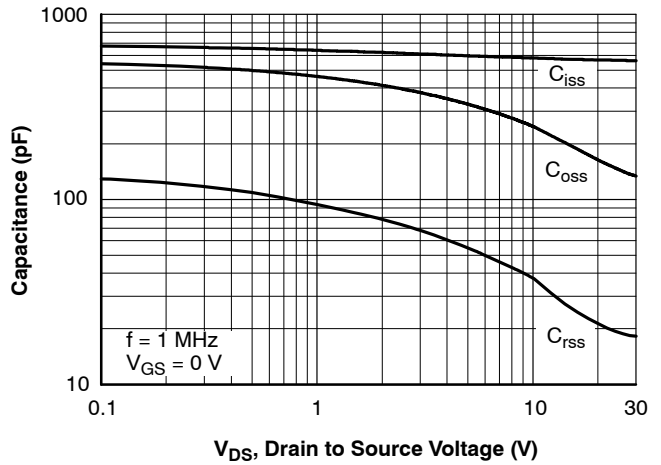


Figure 10. Capacitance vs. Drain to Source Voltage

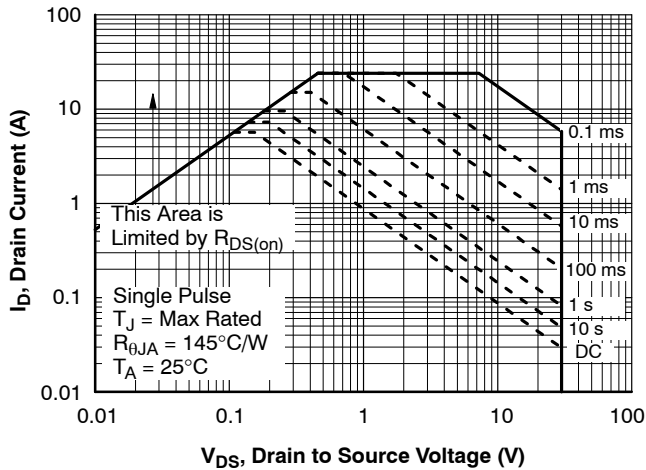


Figure 7. Forward Bias Safe Operating Area

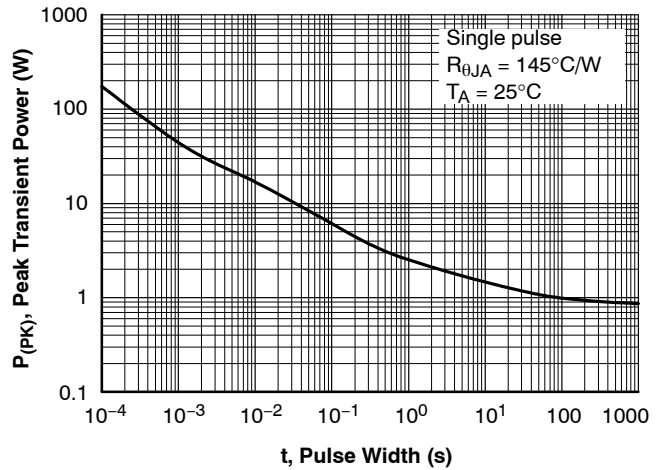


Figure 8. Single Pulse Maximum Power Dissipation

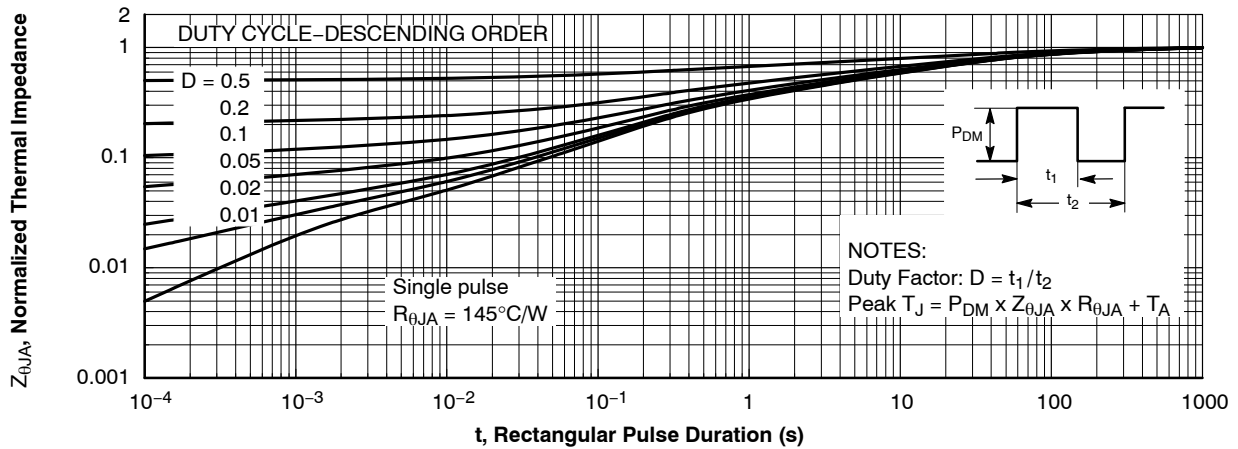


Figure 11. Transient Thermal Response Curve

FDMA7672

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMA7672	672	WDFN6 2x2, 0.65P (Pb-Free/Halide Free)	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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MECHANICAL CASE OUTLINE

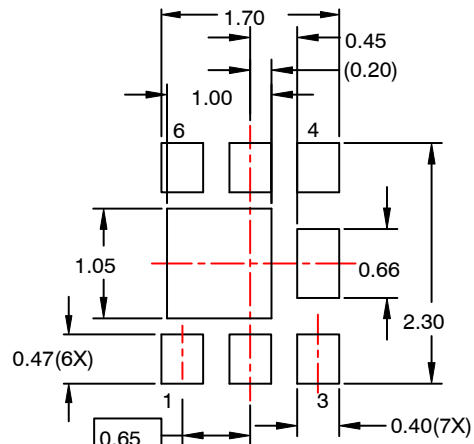
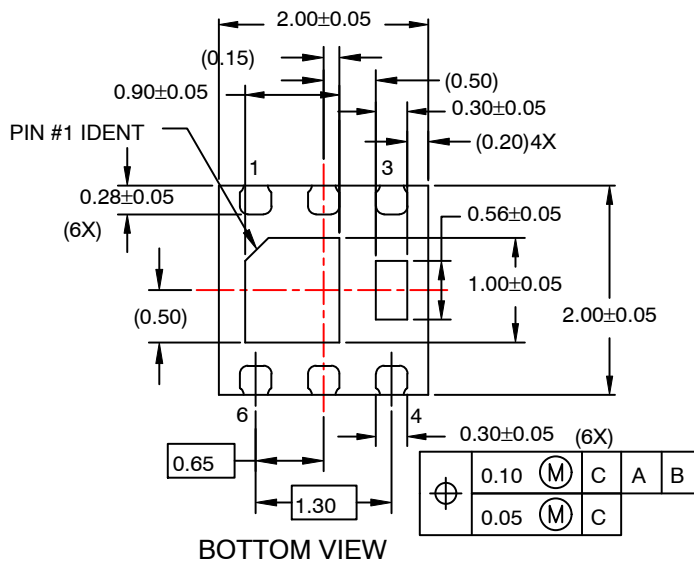
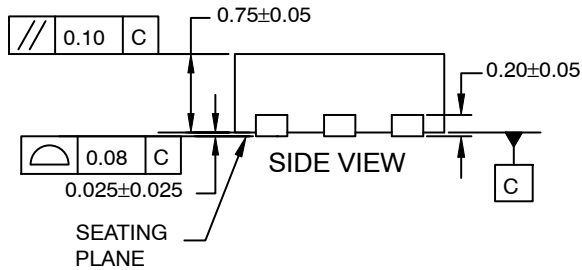
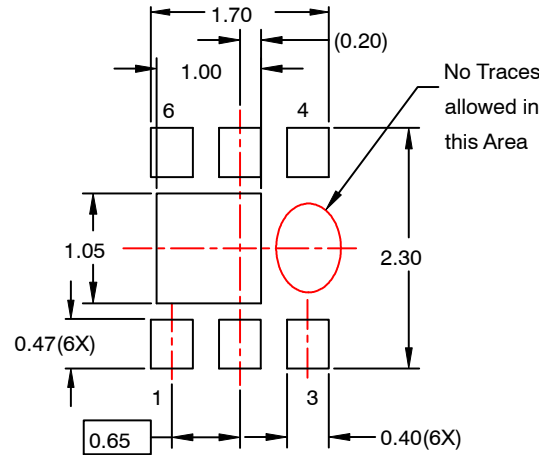
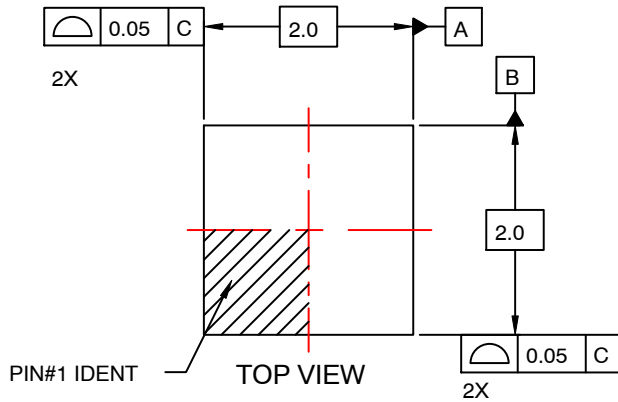
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

DATE 31 JUL 2016



RECOMMENDED LAND PATTERN OPT 1

RECOMMENDED LAND PATTERN OPT 2

NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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