

# MOSFET – Single, P-Channel, POWERTRENCH®

**-20 V, -7.8 A, 30 mΩ**

## FDMA510PZ

### General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET™ 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

### Features

- Max  $R_{DS(on)}$  = 30 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -7.8$  A
- Max  $R_{DS(on)}$  = 37 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -6.6$  A
- Max  $R_{DS(on)}$  = 50 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -5.5$  A
- Max  $R_{DS(on)}$  = 90 mΩ at  $V_{GS} = -1.5$  V,  $I_D = -2.0$  A
- Low Profile – 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 3 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

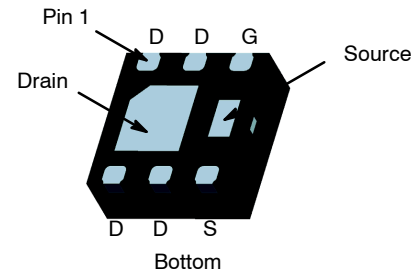
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	$\pm 8$	V
$I_D$	Drain Current		A
	– Continuous (Note 1a)	-7.8	
	– Pulsed	-24	
$P_D$	Power Dissipation (Note 1a)	2.4	W
	Power Dissipation (Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

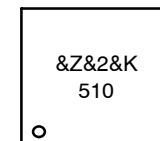
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
-20 V	30 mΩ @ -4.5 V	-7.8 A
	37 mΩ @ -2.5 V	
	50 mΩ @ -1.8 V	
	90 mΩ @ -1.5 V	



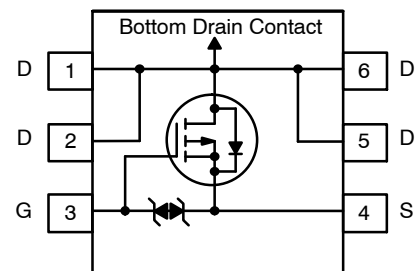
WDFN6 2x2, 0.65P  
 (MicroFET 2x2)  
 CASE 511CZ

### MARKING DIAGRAM



&Z = Assembly Plant Code  
 &2 = 2-Digit Date Code  
 &K = 2-Digits Lot Run Traceability Code  
 510 = Specific Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
FDMA510PZ	WDFN8 MicroFET 2X2 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

# FDMA510PZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C	-	-13	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V	-	-	±10	μA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-0.4	-0.7	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C	-	3	-	mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7.8 A	-	27	30	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -6.6 A	-	34	37	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -5.5 A	-	46	50	
		V <sub>GS</sub> = -1.5 V, I <sub>D</sub> = -2.0 A	-	60	90	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7.8 A, T <sub>J</sub> = 125°C	-	36	40	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = -5 V, I <sub>D</sub> = -7.8 A	-	26	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	1110	1480	pF
C <sub>oss</sub>	Output Capacitance		-	205	275	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	185	280	pF

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -7.8 A, V <sub>GS</sub> = -4.5 V, R <sub>GEN</sub> = 6 Ω	-	7	14	ns
t <sub>r</sub>	Rise Time		-	9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	125	200	ns
t <sub>f</sub>	Fall Time		-	64	103	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> = -5 V, I <sub>D</sub> = -7.8 A, V <sub>GS</sub> = -4.5 V	-	19	27	nC
Q <sub>gs</sub>	Gate to Source Charge		-	2.1	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	4.2	-	nC

### DRAIN-SOURCE CHARACTERISTICS

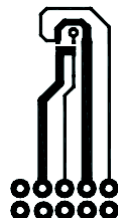
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	-	-	-2	A	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2 A	-	-0.8	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -7.8 A, di/dt = 100 A / μs	-	66	106	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	44	71	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design.



a. 52°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 145°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

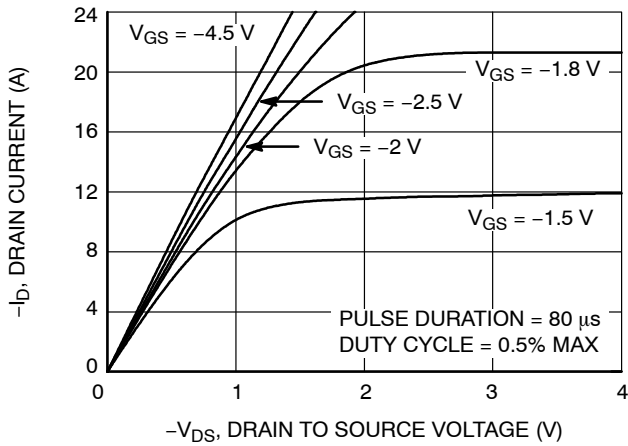


Figure 1. On-Region Characteristics

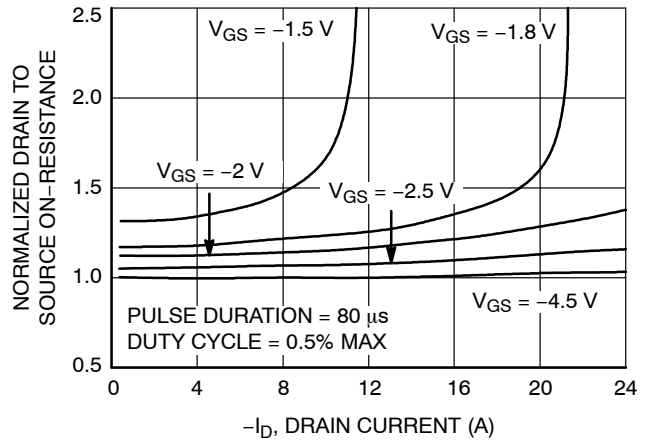


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

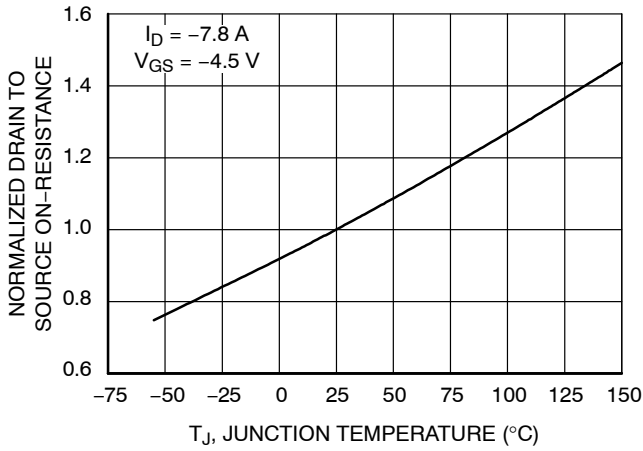


Figure 3. Normalized On-Resistance vs. Junction Temperature

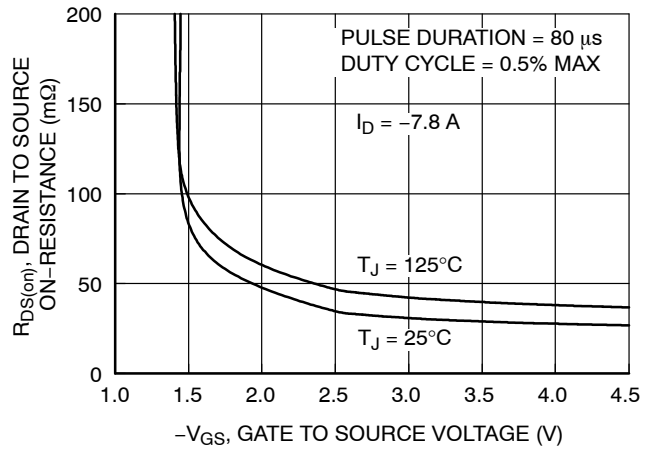


Figure 4. On-Resistance vs. Gate to Source Voltage

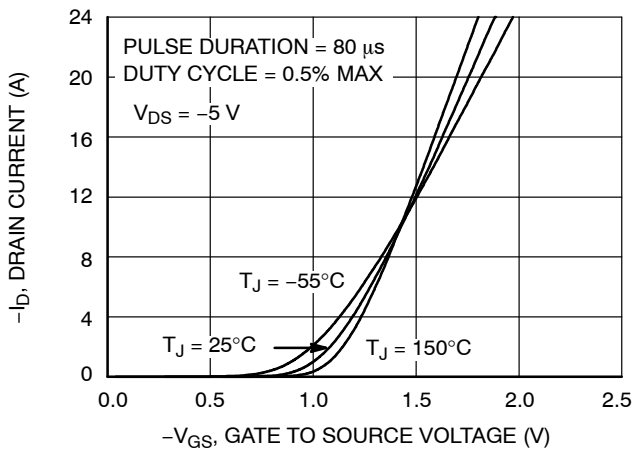


Figure 5. Transfer Characteristics

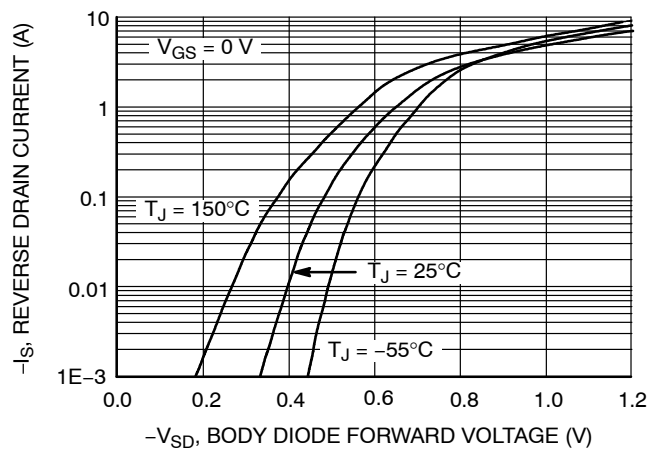


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

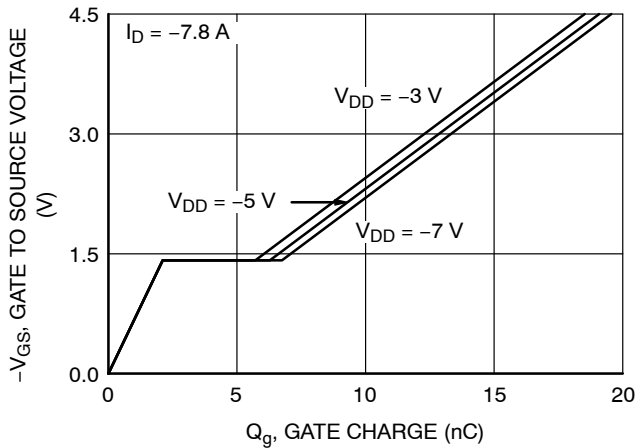


Figure 7. Gate Charge Characteristics

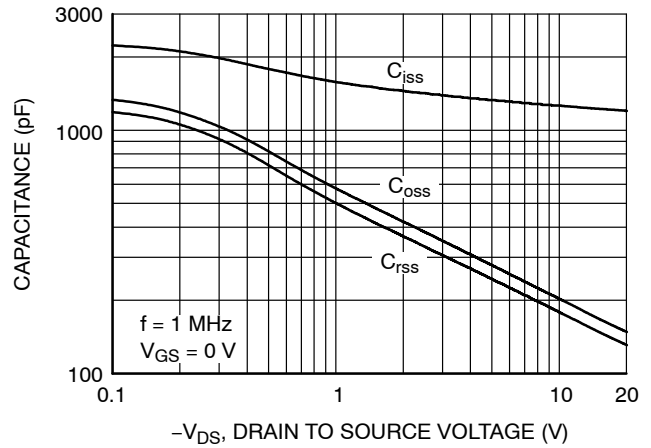


Figure 8. Capacitance vs. Drain to Source Voltage

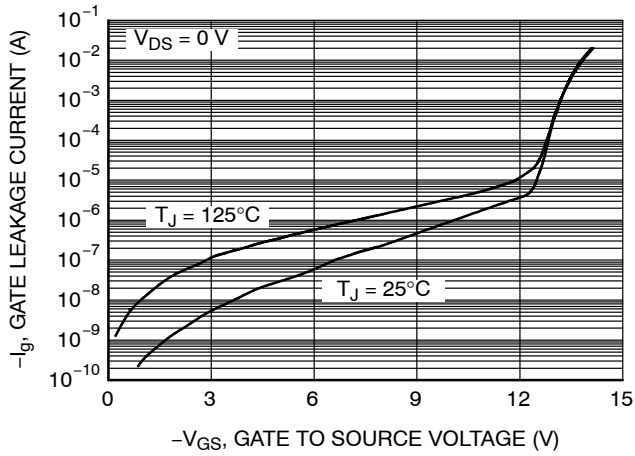


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

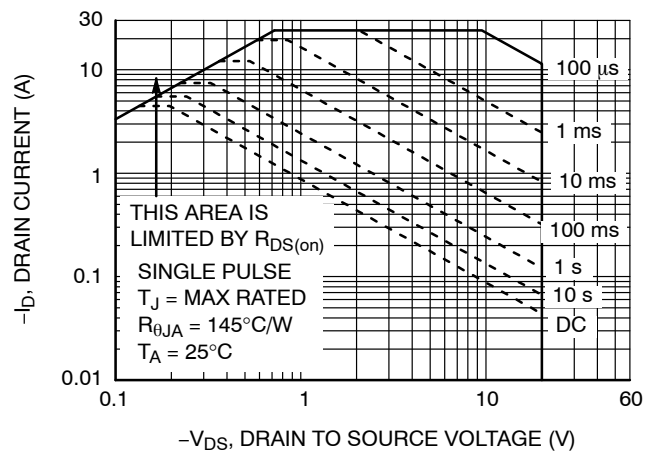


Figure 10. Forward Bias Safe Operating Area

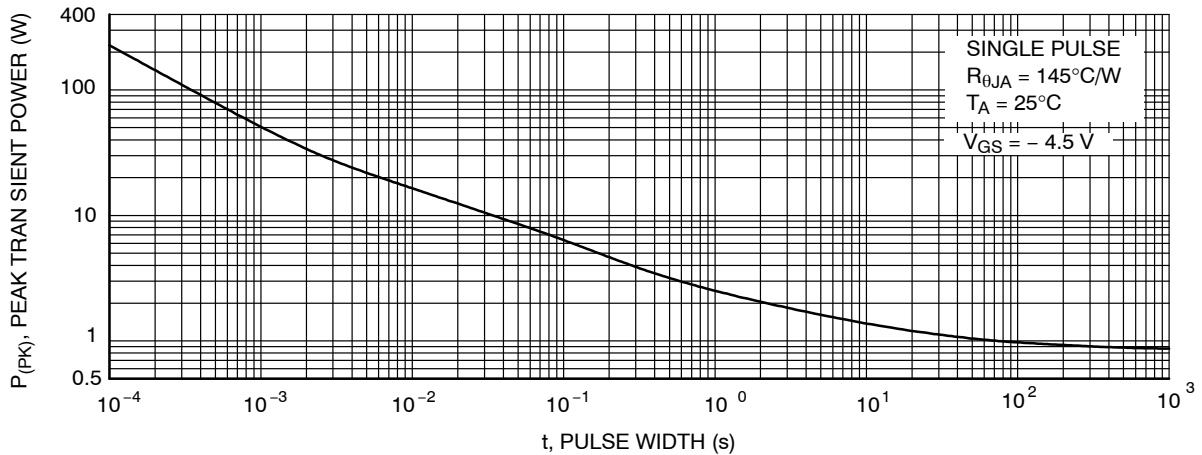
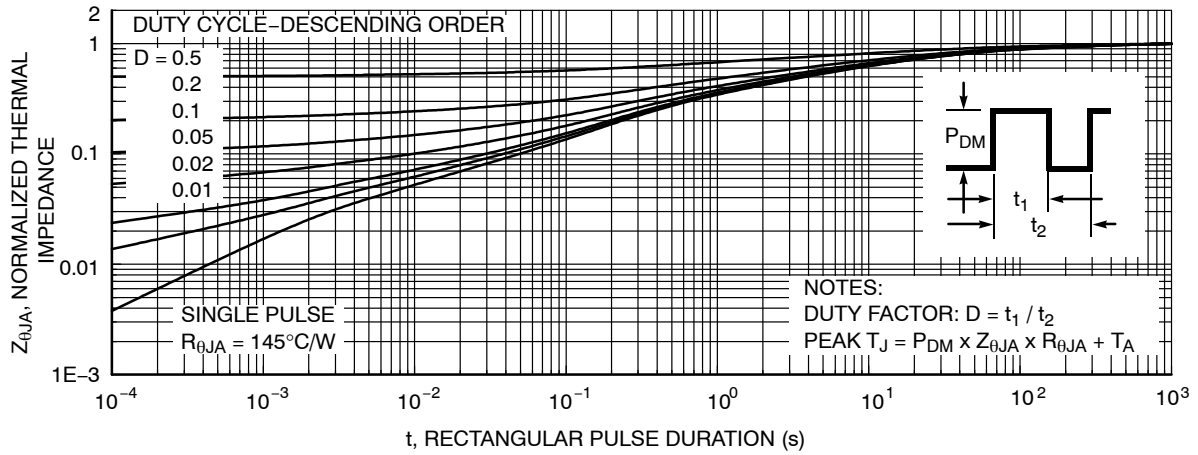


Figure 11. Single Pulse Maximum Power Dissipation

# FDMA510PZ

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)



**Figure 12. Transient Thermal Response Curve**

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# MECHANICAL CASE OUTLINE

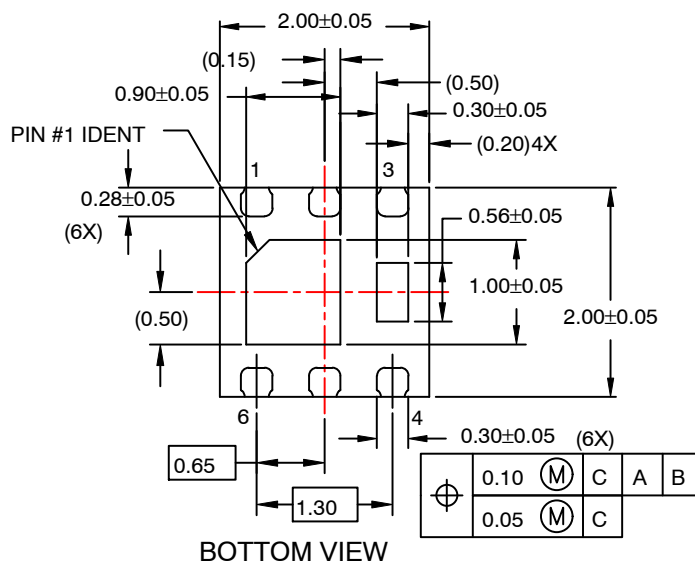
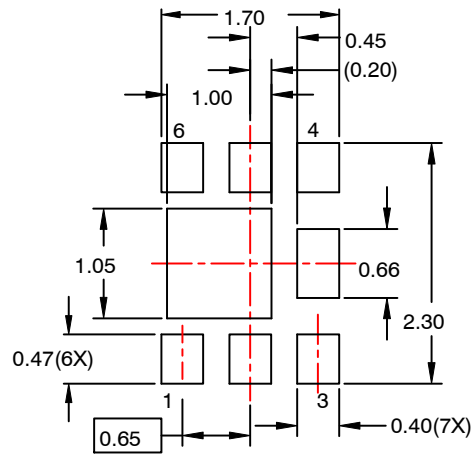
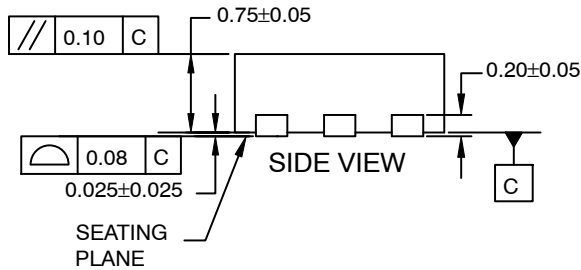
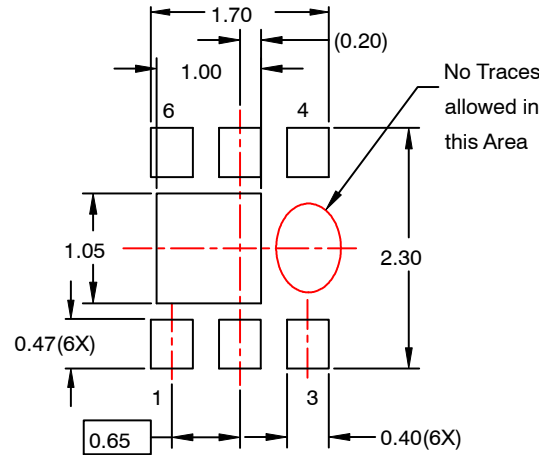
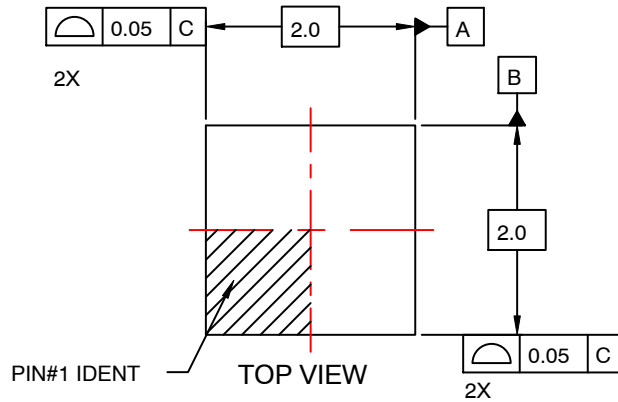
## PACKAGE DIMENSIONS

ON Semiconductor®



WDFN6 2x2, 0.65P  
CASE 511CZ  
ISSUE O

DATE 31 JUL 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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