

# FDFS6N548

## Integrated N-Channel POWERTRENCH<sup>®</sup> MOSFET and Schottky Diode

### Description

The FDFS6N548 combines the exceptional performance of ON Semiconductor's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in an SO-8 package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance. The independently connected Schottky diode allows its use in a variety of DC/DC converter topologies.

### Features

- Max  $r_{DS(on)}$  = 23 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 7\text{ A}$
- Max  $r_{DS(on)}$  = 30 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 6\text{ A}$
- $V_F < 0.45\text{ V @ } 2\text{ A}$   
 $V_F < 0.28\text{ V @ } 100\text{ mA}$
- Schottky and MOSFET Incorporated into Single Power Surface Mount SO-8 Package
- Electrically Independent Schottky and MOSFET Pinout for Design Flexibility
- Low Miller Charge

### Application

- DC/DC Conversion

### MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-to-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
I <sub>D</sub>	Drain Current	Continuous (Note 1a)	7
		Pulsed	30
P <sub>D</sub>	Power Dissipation	Dual Operation	2
		Single Operation (Note 1a)	1.6
E <sub>AS</sub>	Drain-Source Avalanche Energy (Note 3)	12	mJ
V <sub>R</sub> RM	Schottky Repetitive Peak Reverse Voltage	30	V
I <sub>O</sub>	Schottky Average Forward Current (Note 1a)	2	A
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

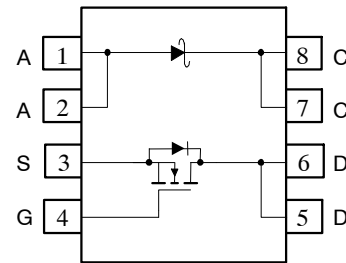
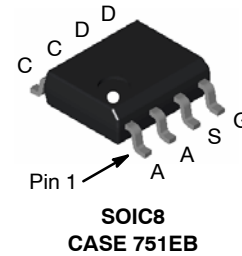
### THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W



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### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDFS6N548

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-to-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
ΔB <sub>V</sub> DSS/ ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		22		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V, T <sub>J</sub> = 125°C			250	
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

## ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.2	1.8	2.5	V
ΔV <sub>GS(th)</sub> / ΔT <sub>J</sub>	Gate-to-Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		-5		mV/°C
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A		19	23	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6 A		23	30	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A, T <sub>J</sub> = 125°C		26	31	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 7 A		20		S

## DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		525	700	pF
C <sub>oss</sub>	Output Capacitance			100	133	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			65	100	pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz		0.8		Ω

## SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 7 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		6	12	ns
t <sub>r</sub>	Rise Time			2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			14	25	ns
t <sub>f</sub>	Fall Time			2	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at 10 V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7 A, V <sub>GS</sub> = 10 V		9	13	nC
Q <sub>gs</sub>	Gate-to-Source Gate Charge			1.5		nC
Q <sub>gd</sub>	Gate-to-Drain "Miller" Charge			2		nC

## DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source-to-Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7 A (Note 2)		0.90	1.25	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 7 A, di/dt = 100 A/μs		23	35	ns
Q <sub>rr</sub>	Reverse Recovery Charge			14	21	nC

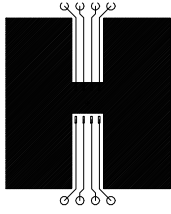
## SCHOTTKY DIODE CHARACTERISTICS

V <sub>R</sub>	Reverse Breakdown Voltage	I <sub>R</sub> = -1 mA	-30			V
I <sub>R</sub>	Reverse Leakage	V <sub>R</sub> = -10 V	T <sub>J</sub> = 25°C	-39	-250	μA
			T <sub>J</sub> = 125°C	-18		mA
V <sub>F</sub>	Forward Voltage	I <sub>F</sub> = 100 mA	T <sub>J</sub> = 25°C	225	280	mV
			T <sub>J</sub> = 125°C	140		
		I <sub>F</sub> = 2 A	T <sub>J</sub> = 25°C	364	450	
			T <sub>J</sub> = 125°C	290		

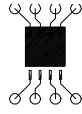
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## FDFS6N548

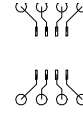
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in<sup>2</sup> pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty Cycle < 2.0%.  
3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1$  mH,  $I_{AS} = 5.0$  A,  $V_{DD} = 27$  V,  $V_{GS} = 10$  V.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

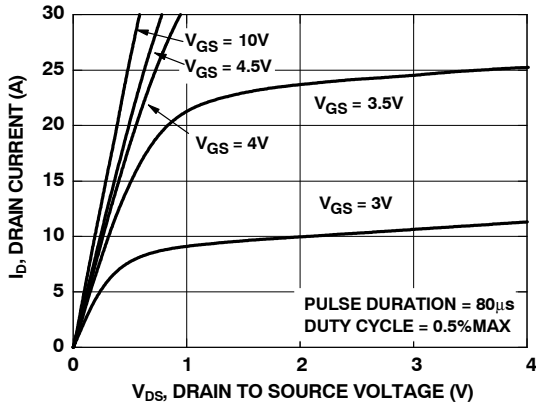


Figure 1. On Region Characteristics

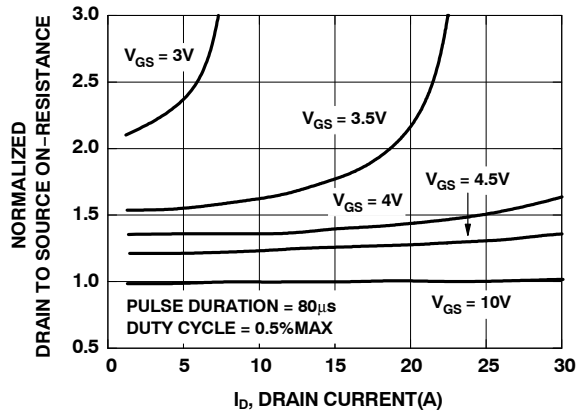


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

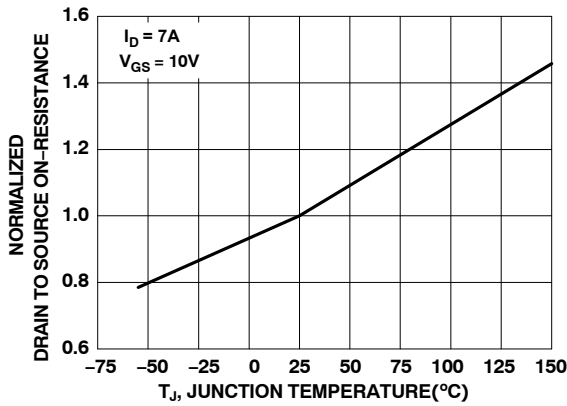


Figure 3. Normalized On-Resistance vs. Junction Temperature

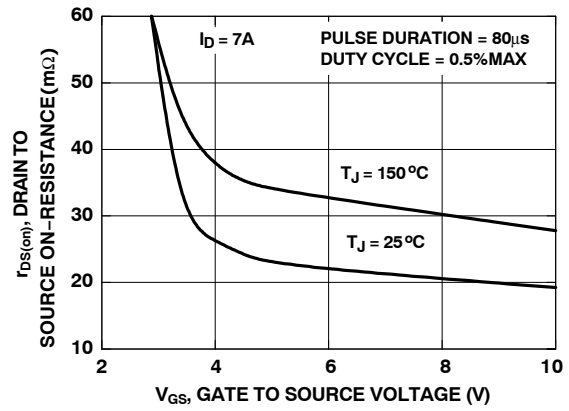


Figure 4. On-Resistance vs. Gate-to-Source Voltage

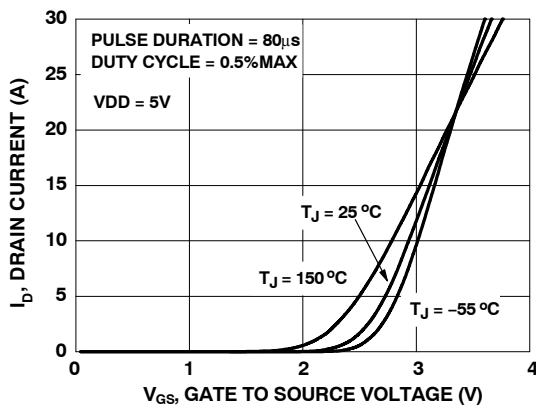


Figure 5. Transfer Characteristics

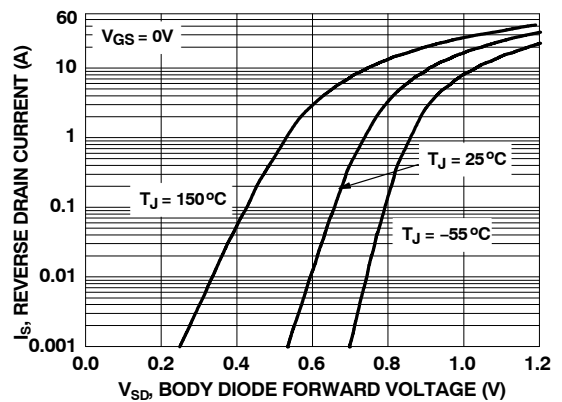


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

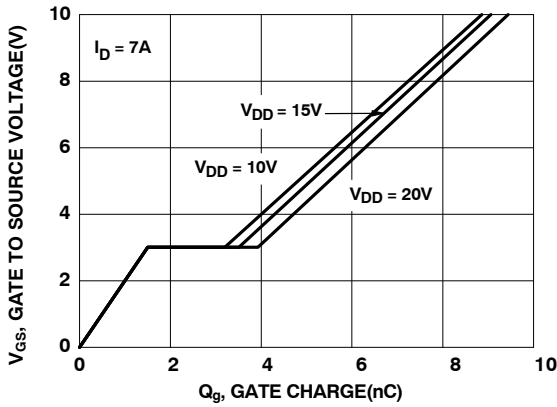


Figure 7. Gate Charge Characteristics

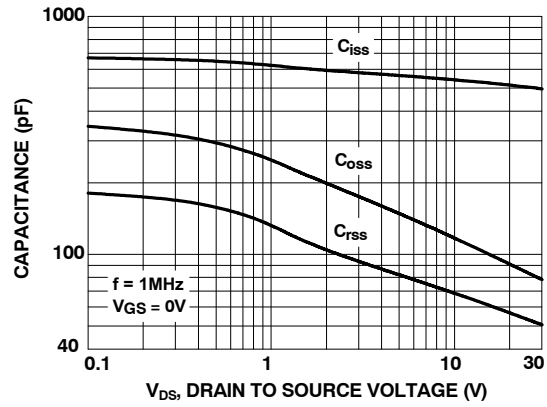


Figure 8. Capacitance vs. Drain-to-Source Voltage

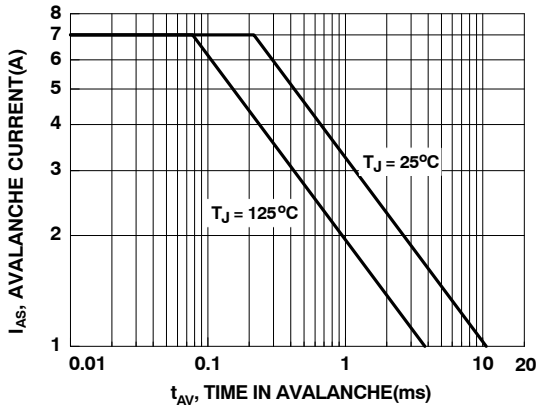


Figure 9. Unclamped Inductive Switching Capability

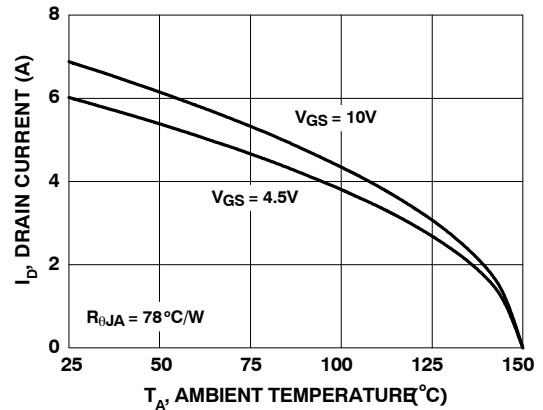


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

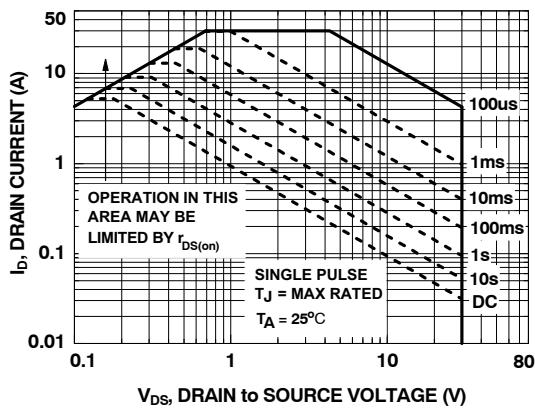


Figure 11. Forward Bias Safe Operating Area

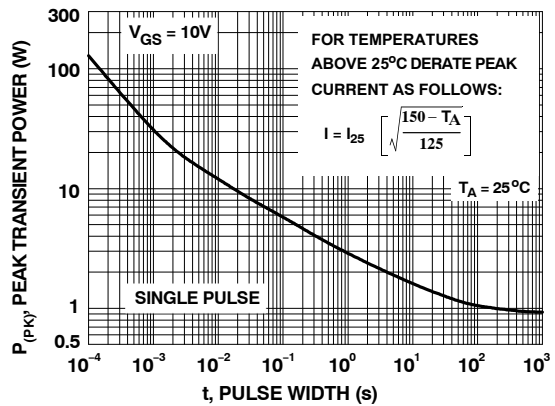


Figure 12. Single Pulse Maximum Power Dissipation

# FDFS6N548

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

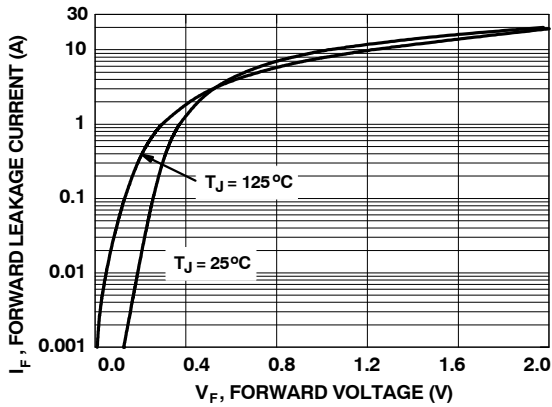


Figure 13. Schottky Diode Forward Characteristics

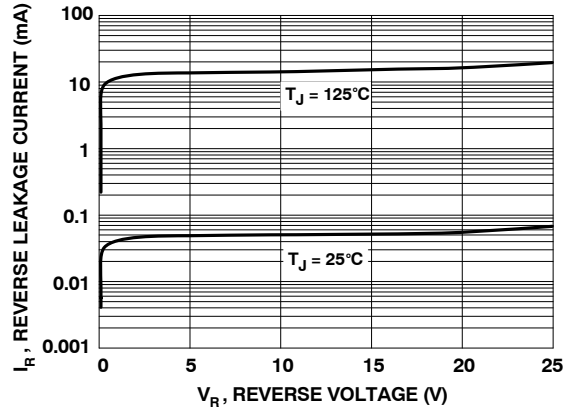


Figure 14. Schottky Diode Reverse Characteristics

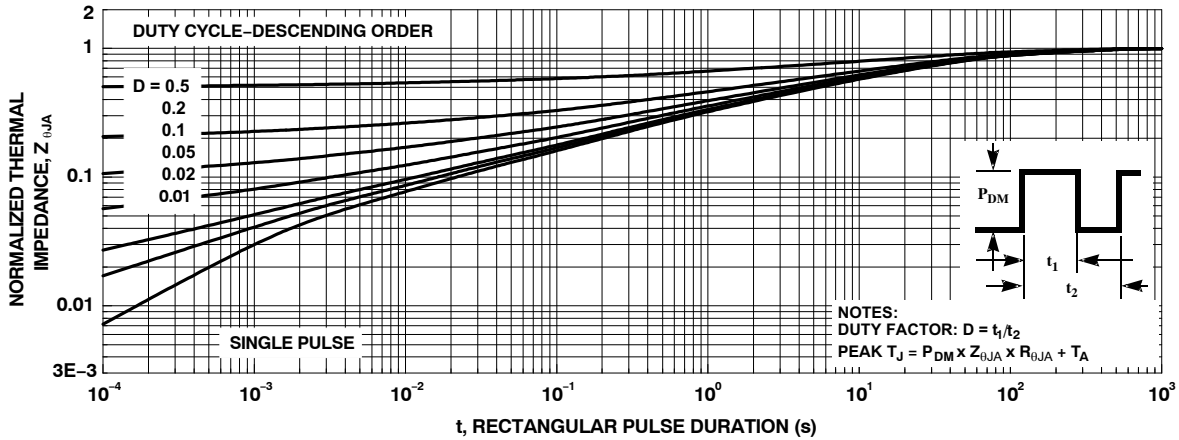


Figure 15. Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
FDFS6N548	FDFS6N548	SO-8	330 mm	12 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

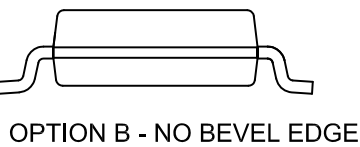
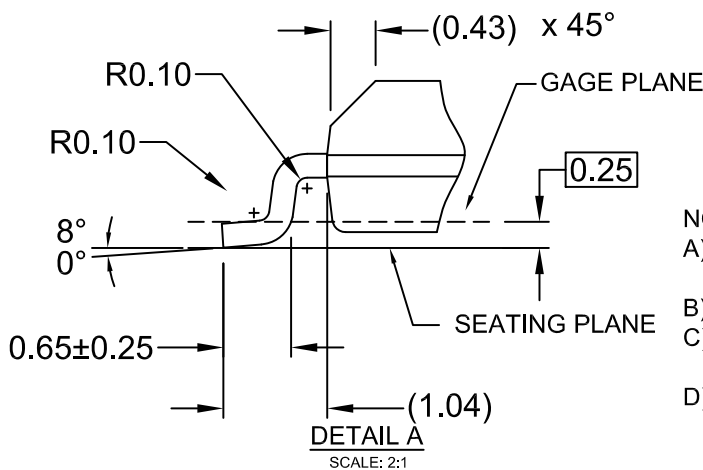
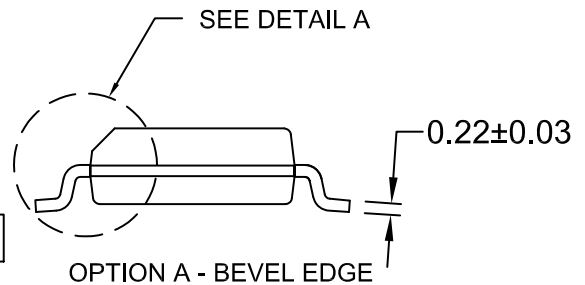
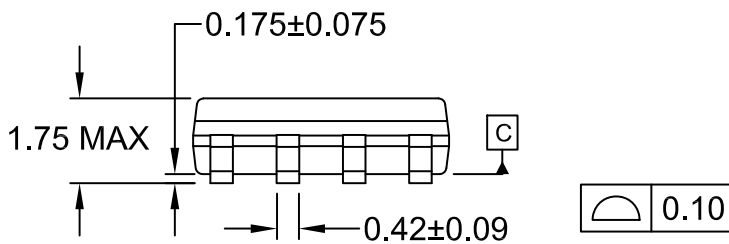
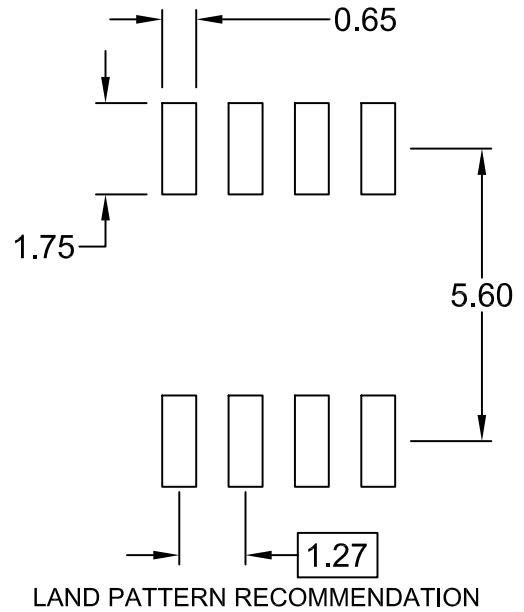
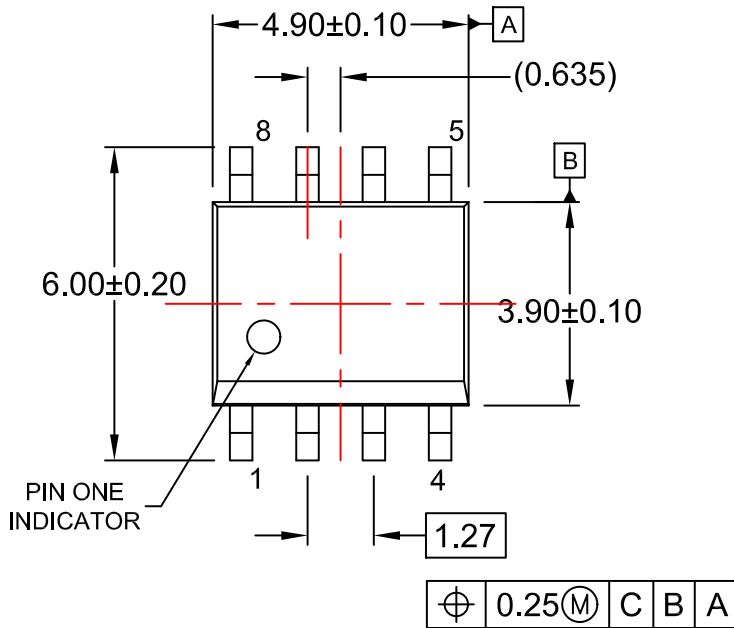
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

ON Semiconductor®



**SOIC8**  
**CASE 751EB**  
**ISSUE A**

DATE 24 AUG 2017



- NOTES:  
 A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.  
 D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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