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ON Semiconductor®

# FDD86369-F085

## N-Channel PowerTrench® MOSFET

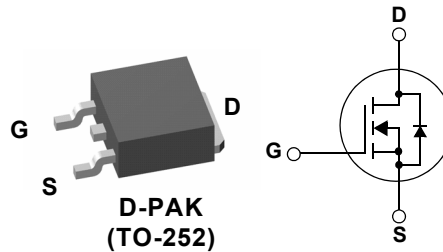
80 V, 90 A, 7.9 mΩ

### Features

- Typical  $R_{DS(on)}$  = 5.9 mΩ at  $V_{GS} = 10V$ ,  $I_D = 80 A$
- Typical  $Q_{g(tot)}$  = 34 nC at  $V_{GS} = 10V$ ,  $I_D = 80 A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

### Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems



### MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted.

| Symbol          | Parameter  | Ratings            | Units         |
|-----------------|--|--------------------|---------------|
| $V_{DSS}$       | Drain-to-Source Voltage                                  | 80                 | V             |
| $V_{GS}$        | Gate-to-Source Voltage                                   | ±20                | V             |
| $I_D$           | Drain Current - Continuous ( $V_{GS}=10$ ) (Note 1)      | $T_C = 25^\circ C$ | A             |
|                 | Pulsed Drain Current                                     | $T_C = 25^\circ C$ |               |
| $E_{AS}$        | Single Pulse Avalanche Energy (Note 2)                   | 29                 | mJ            |
| $P_D$           | Power Dissipation  | 150                | W             |
|                 | Derate Above $25^\circ C$                                | 1.0                | W/ $^\circ C$ |
| $T_J, T_{STG}$  | Operating and Storage Temperature                        | -55 to + 175       | $^\circ C$    |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case                     | 1.0                | $^\circ C/W$  |
| $R_{\theta JA}$ | Maximum Thermal Resistance, Junction to Ambient (Note 3) | 52                 | $^\circ C/W$  |

#### Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting  $T_J = 25^\circ C$ ,  $L = 14\mu H$ ,  $I_{AS} = 64A$ ,  $V_{DD} = 80V$  during inductor charging and  $V_{DD} = 0V$  during time in avalanche.
- 3:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

### Package Marking and Ordering Information

| Device Marking | Device        | Package       | Reel Size | Tape Width | Quantity  |
|----------------|---------------|---------------|-----------|------------|-----------|
| FDD86369       | FDD86369-F085 | D-PAK(TO-252) | 13"       | 16mm       | 2500units |

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|--------|-----------|-----------------|------|------|------|-------|
|--------|-----------|-----------------|------|------|------|-------|

### Off Characteristics

|            |                                   |   |    |   |           |               |
|------------|-----------------------------------|---|----|---|-----------|---------------|
| $B_{VDSS}$ | Drain-to-Source Breakdown Voltage | $I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$             | 80 | - | -         | V             |
| $I_{DSS}$  | Drain-to-Source Leakage Current   | $V_{DS} = 80\text{V}$ , $T_J = 25^\circ\text{C}$          | -  | - | 1         | $\mu\text{A}$ |
|            |                                   | $V_{GS} = 0\text{V}$ , $T_J = 175^\circ\text{C}$ (Note 4) | -  | - | 1         | $\text{mA}$   |
| $I_{GSS}$  | Gate-to-Source Leakage Current    | $V_{GS} = \pm 20\text{V}$                                 | -  | - | $\pm 100$ | $\text{nA}$   |

### On Characteristics

|              |                                  |  |     |      |      |                  |
|--------------|----------------------------------|--|-----|------|------|------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$                 | 2.0 | 2.7  | 4.0  | V                |
| $R_{DS(on)}$ | Drain to Source On Resistance    | $I_D = 80\text{A}$ , $T_J = 25^\circ\text{C}$              | -   | 5.9  | 7.9  | $\text{m}\Omega$ |
|              |                                  | $V_{GS} = 10\text{V}$ , $T_J = 175^\circ\text{C}$ (Note 4) | -   | 13.0 | 17.4 | $\text{m}\Omega$ |

### Dynamic Characteristics

|              |                               |   |   |      |    |             |
|--------------|-------------------------------|---|---|------|----|-------------|
| $C_{iss}$    | Input Capacitance             | $V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$ ,<br>$f = 1\text{MHz}$ | - | 2530 | -  | $\text{pF}$ |
| $C_{oss}$    | Output Capacitance            |   | - | 430  | -  | $\text{pF}$ |
| $C_{riss}$   | Reverse Transfer Capacitance  |   | - | 16   | -  | $\text{pF}$ |
| $R_g$        | Gate Resistance               | $V_{GS} = 0.5\text{V}$ , $f = 1\text{MHz}$                          | - | 2.2  | -  | $\Omega$    |
| $Q_{g(ToT)}$ | Total Gate Charge             | $V_{GS} = 0$ to $10\text{V}$  | - | 36   | 54 | $\text{nC}$ |
| $Q_{g(th)}$  | Threshold Gate Charge         | $V_{GS} = 0$ to $2\text{V}$   |   |      |    |             |
| $Q_{gs}$     | Gate-to-Source Gate Charge    | $V_{DD} = 64\text{V}$<br>$I_D = 80\text{A}$                         | - | 13   | -  | $\text{nC}$ |
| $Q_{gd}$     | Gate-to-Drain "Miller" Charge |   | - | 8.5  | -  | $\text{nC}$ |

### Switching Characteristics

|              |                |   |   |    |    |             |
|--------------|----------------|---|---|----|----|-------------|
| $t_{on}$     | Turn-On Time   | $V_{DD} = 40\text{V}$ , $I_D = 80\text{A}$ ,<br>$V_{GS} = 10\text{V}$ , $R_{GEN} = 6\Omega$ | - | -  | 70 | $\text{ns}$ |
| $t_{d(on)}$  | Turn-On Delay  |   | - | 13 | -  | $\text{ns}$ |
| $t_r$        | Rise Time      |   | - | 34 | -  | $\text{ns}$ |
| $t_{d(off)}$ | Turn-Off Delay |   | - | 22 | -  | $\text{ns}$ |
| $t_f$        | Fall Time      |   | - | 9  | -  | $\text{ns}$ |
| $t_{off}$    | Turn-Off Time  |   | - | -  | 46 | $\text{ns}$ |

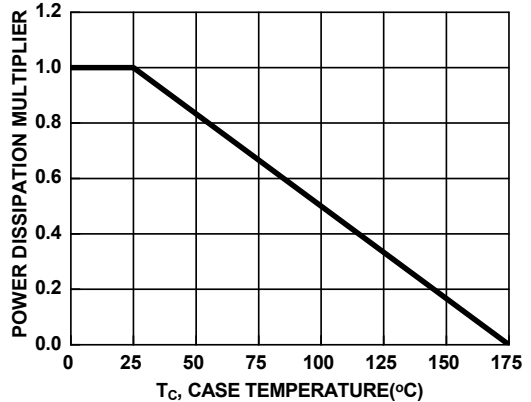
### Drain-Source Diode Characteristics

|          |                               |   |   |    |      |             |
|----------|-------------------------------|---|---|----|------|-------------|
| $V_{SD}$ | Source-to-Drain Diode Voltage | $I_{SD} = 80\text{A}$ , $V_{GS} = 0\text{V}$                | - | -  | 1.25 | V           |
|          |                               | $I_{SD} = 40\text{A}$ , $V_{GS} = 0\text{V}$                | - | -  | 1.2  | V           |
| $t_{rr}$ | Reverse-Recovery Time         | $I_F = 80\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | 49 | 64   | $\text{ns}$ |
| $Q_{rr}$ | Reverse-Recovery Charge       |   | - | 40 | 53   | $\text{nC}$ |

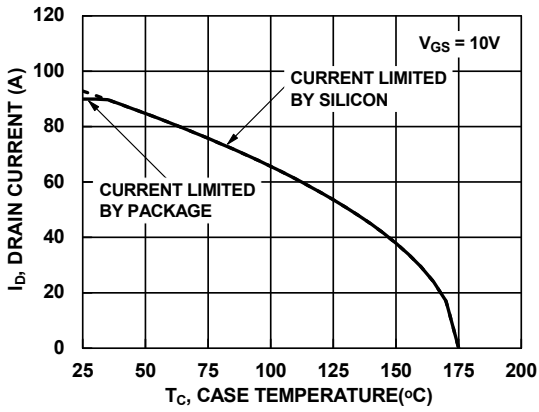
**Note:**

4: The maximum value is specified by design at  $T_J = 175^\circ\text{C}$ . Product is not tested to this condition in production.

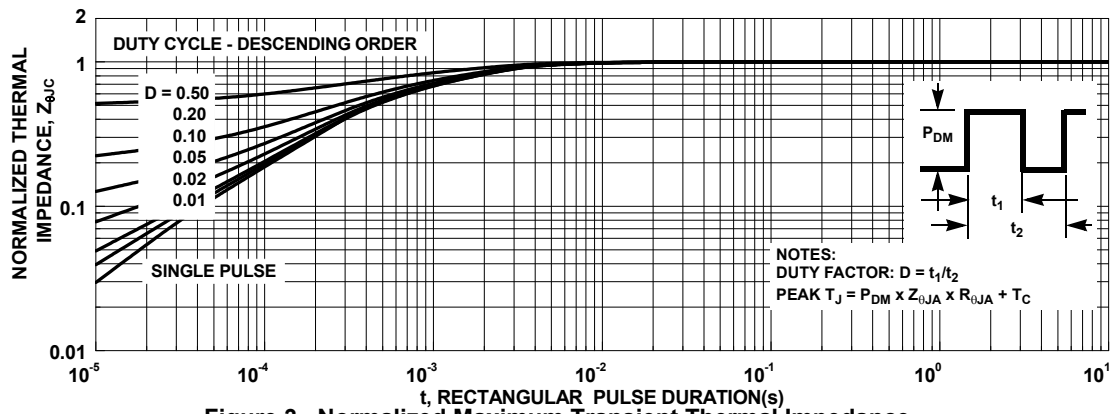
**Typical Characteristics**



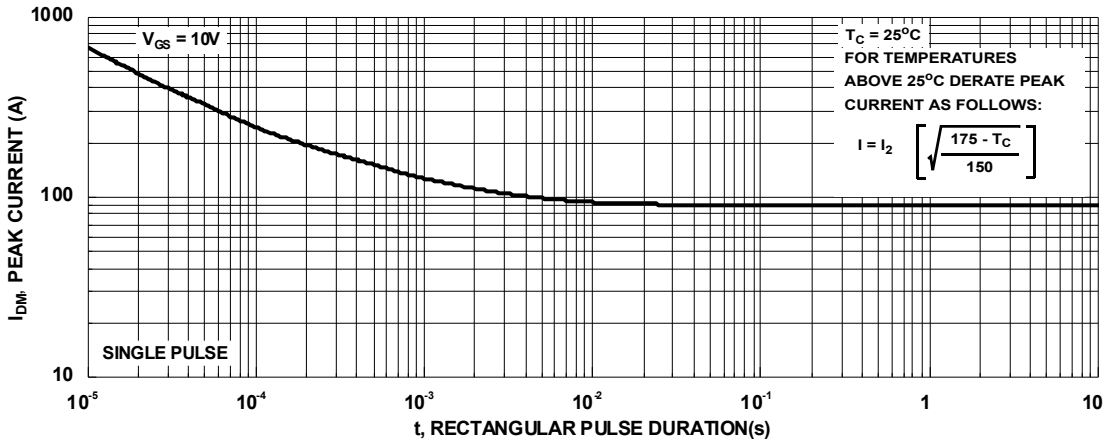
**Figure 1. Normalized Power Dissipation vs. Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**

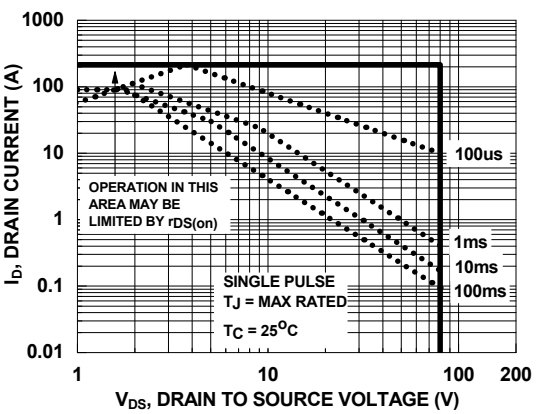


**Figure 3. Normalized Maximum Transient Thermal Impedance**

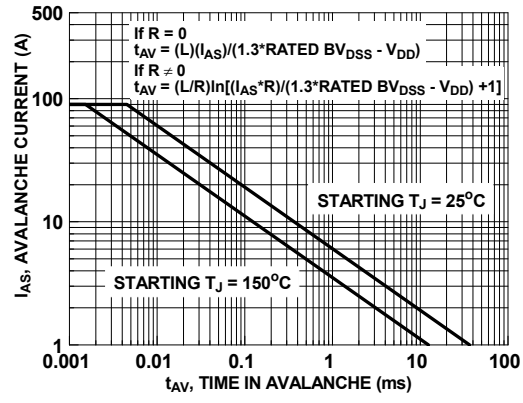


**Figure 4. Peak Current Capability**

**Typical Characteristics**

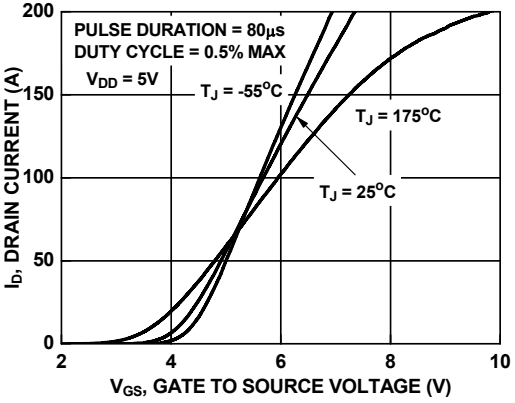


**Figure 5. Forward Bias Safe Operating Area**

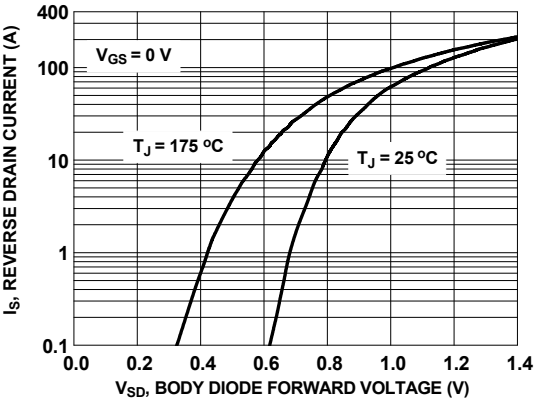


NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

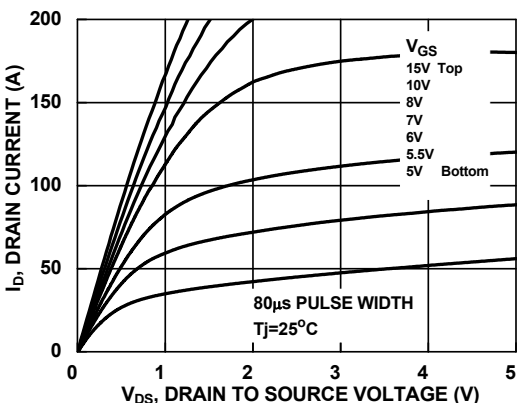
**Figure 6. Unclamped Inductive Switching Capability**



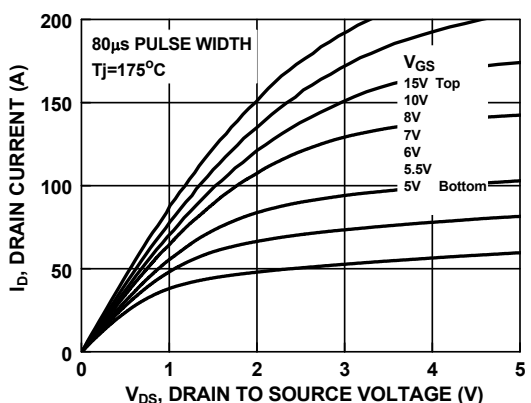
**Figure 7. Transfer Characteristics**



**Figure 8. Forward Diode Characteristics**

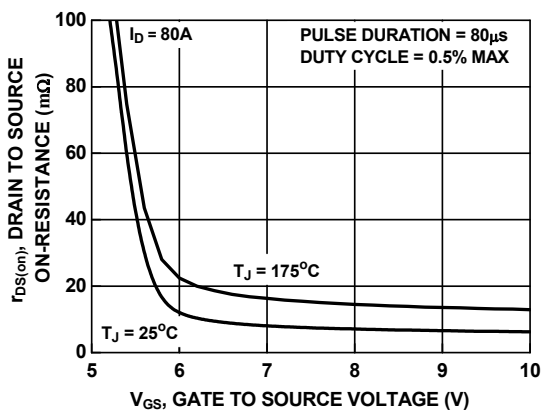


**Figure 9. Saturation Characteristics**

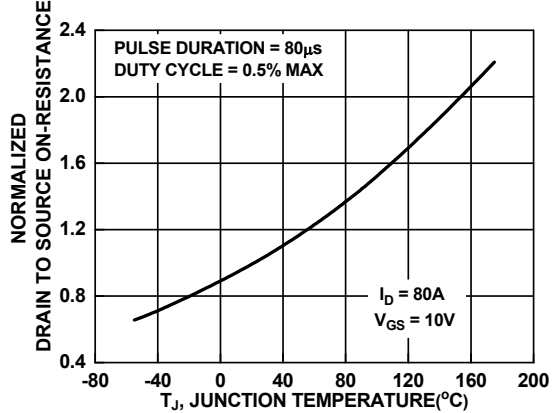


**Figure 10. Saturation Characteristics**

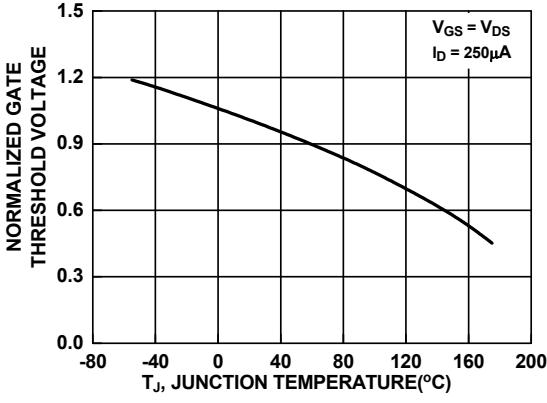
**Typical Characteristics**



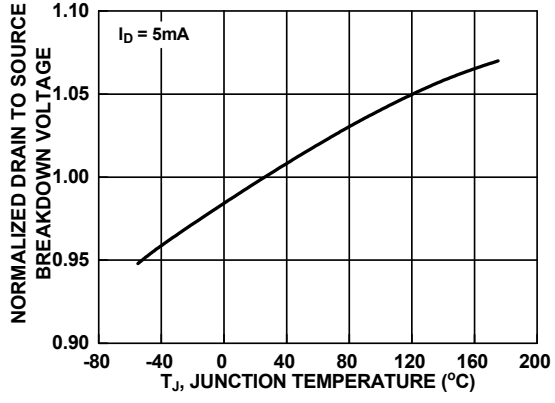
**Figure 11.  $R_{DS(on)}$  vs. Gate Voltage**



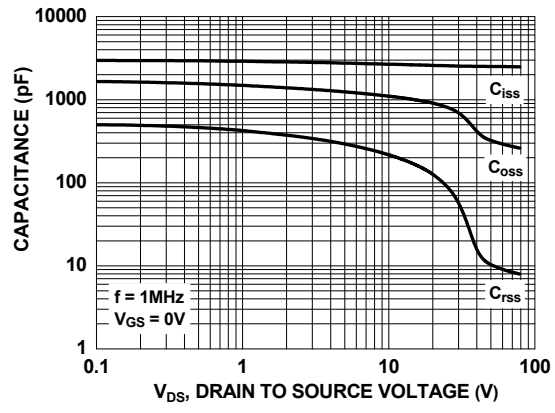
**Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature**



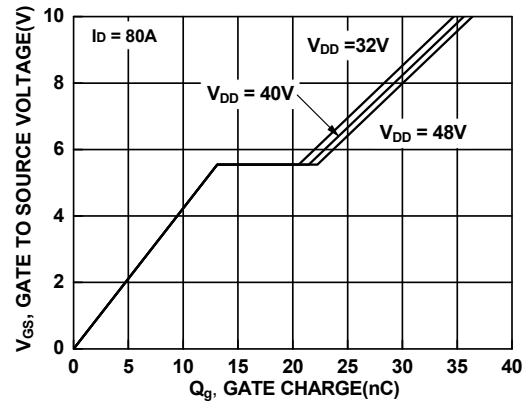
**Figure 13. Normalized Gate Threshold Voltage vs. Temperature**



**Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature**



**Figure 15. Capacitance vs. Drain to Source Voltage**



**Figure 16. Gate Charge vs. Gate to Source Voltage**

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