

# MOSFET – N-Channel, POWERTRENCH®

100 V

FDD3680

## General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{DS(ON)}$  specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

## Features

- 25 A, 100 V.  $R_{DS(ON)} = 46 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 51 \text{ m}\Omega @ V_{GS} = 6 \text{ V}$
- Low Gate Charge (38 nC Typical)
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low  $R_{DS(ON)}$
- High Power and Current Handling Capability

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

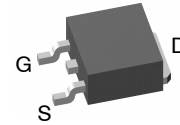
Symbol	Parameter	Ratings	Unit	
V <sub>DSS</sub>	Drain-Source Voltage	100	V	
V <sub>GSS</sub>	Gate-Source Voltage	+20	V	
I <sub>D</sub>	Drain Current – Continuous (Note 1)	25	A	
	Drain Current – Pulsed	100		
P <sub>D</sub>	Maximum Power Dissipation (Note 1)	68	W	
		(Note 1a)		3.8
		(Note 1b)		1.6
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +175	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

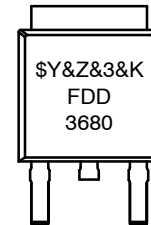
Symbol	Parameter	Ratings	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	2.2	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	°C/W

V <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
100 V	46 mΩ @ 10 V	25 A

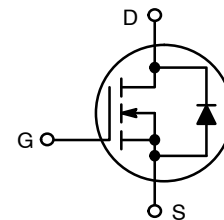


DPAK3 (TO-252 3 LD)  
CASE 369AS

## MARKING DIAGRAM



- \$Y = Logo
- FDD3680 = Device Code
- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code Format
- &K = 2-Digits Lot Run Traceability Code



N-Channel

## ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDD3680

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### DRAIN-SOURCE AVALANCHE RATINGS (Note 1)

W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 6.1 A	-	-	245	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Current		-	-	6.1	A

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	101	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	-	-	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	-	-	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	-	-	-100	nA

### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	2.4	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	-6.5	-	mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.1 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.1 A, T <sub>J</sub> = 125°C V <sub>GS</sub> = 6 V, I <sub>D</sub> = 5.8 A	-	32 61 34	46 92 51	mΩ
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	25	-	-	A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 6.1 A	-	25	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	-	1735	-	pF
C <sub>oss</sub>	Output Capacitance		-	176	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	53	-	pF

### SWITCHING CHARACTERISTICS (Note 2)

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 10 Ω	-	14	25	ns
t <sub>r</sub>	Turn-On Rise Time		-	8.5	17	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	63	94	ns
t <sub>f</sub>	Turn-Off Fall Time		-	21	34	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 6.1 A, V <sub>GS</sub> = 10 V	-	38	53	nC
Q <sub>gs</sub>	Gate-Source Charge		-	8.1	-	nC
Q <sub>gd</sub>	Gate-Drain Charge		-	9.2	-	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		-	-	2.9	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.9 A (Note 2)	-	0.73	1.3	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



- a. R<sub>θJA</sub> = 40°C/W when mounted on a 1 in<sup>2</sup> pad of 2oz copper.



- b. R<sub>θJA</sub> = 96°C/W on a minimum mounting pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS

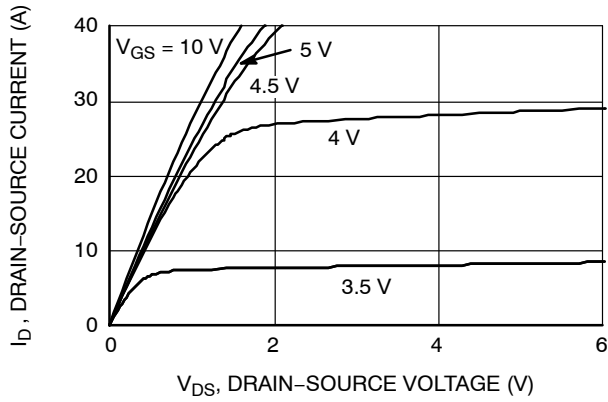


Figure 1. On-Region Characteristics

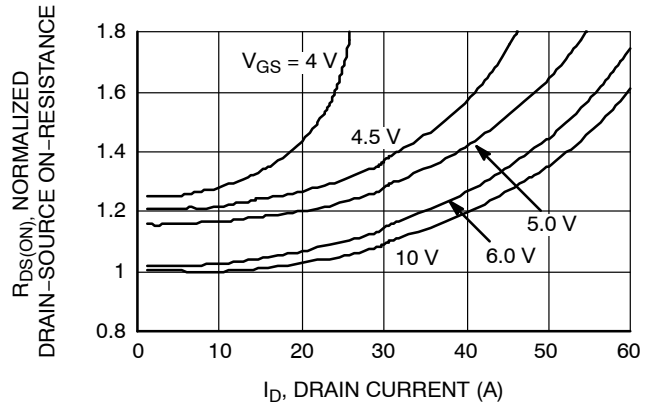


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

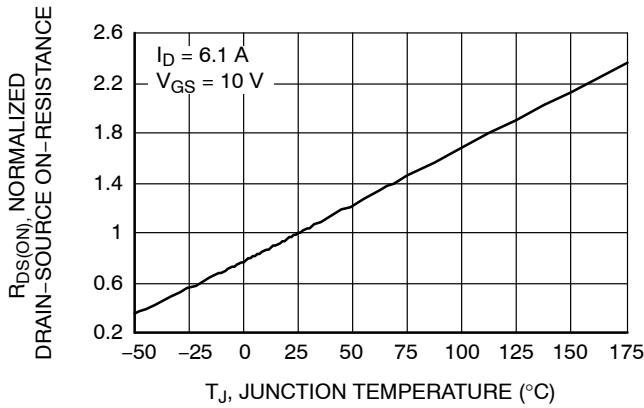


Figure 3. On-Resistance Variation with Temperature

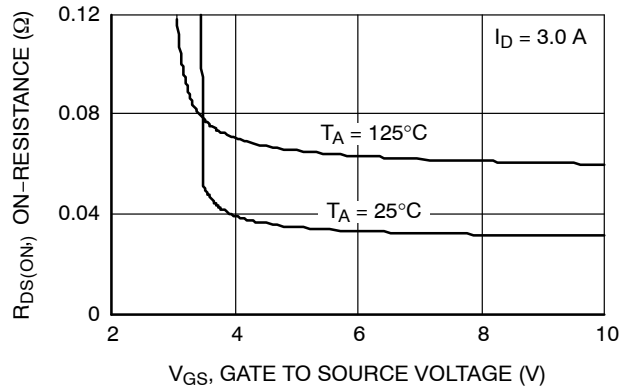


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

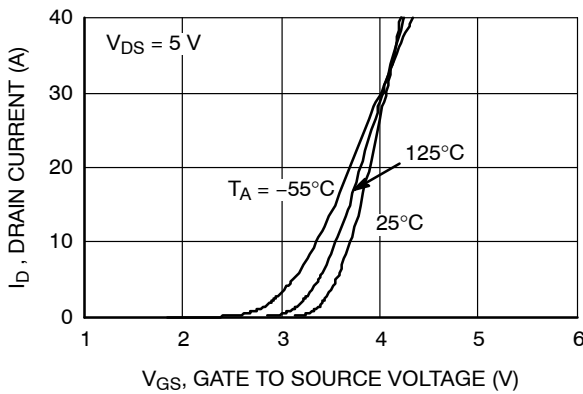


Figure 5. Transfer Characteristics

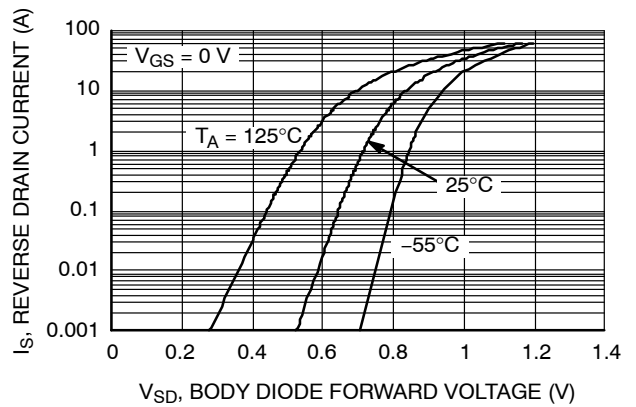


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

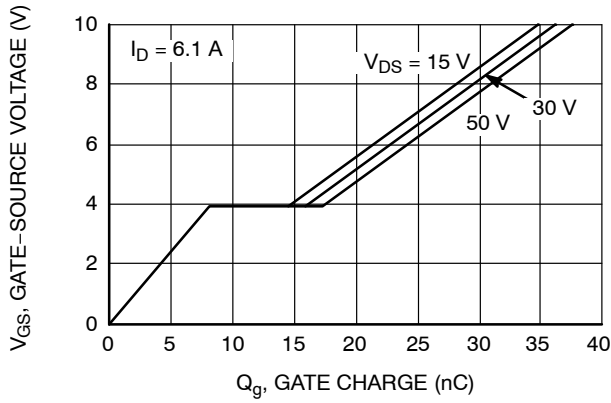


Figure 7. Gate Charge Characteristics

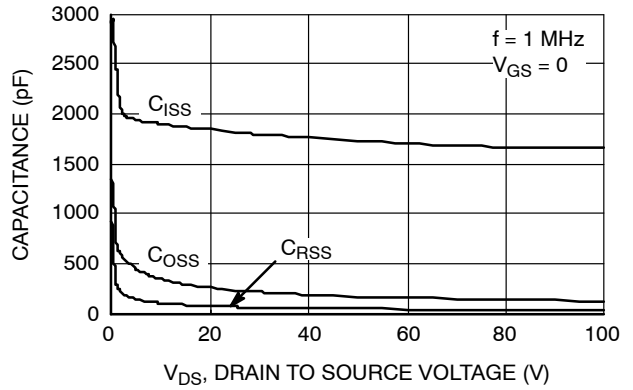


Figure 8. Capacitance Characteristics

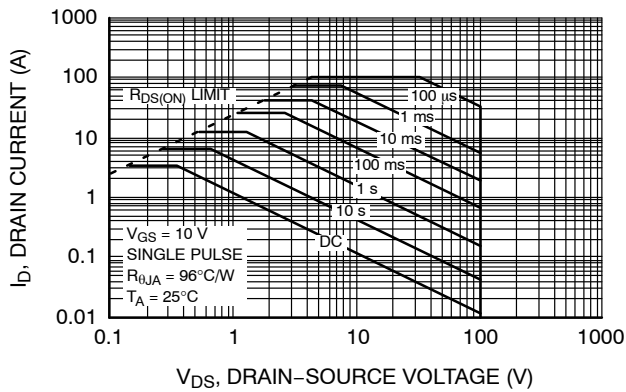


Figure 9. Maximum Safe Operating Area

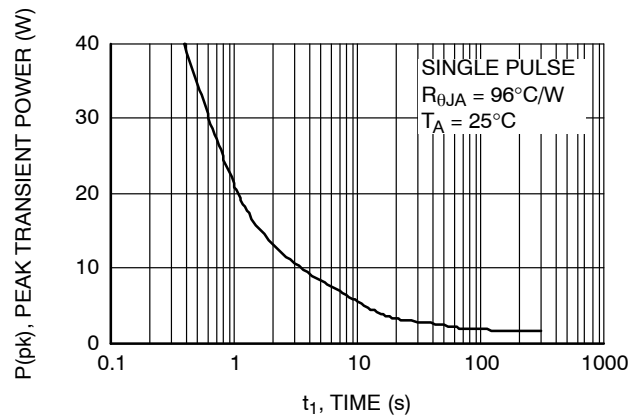


Figure 10. Single Pulse Maximum Power Dissipation

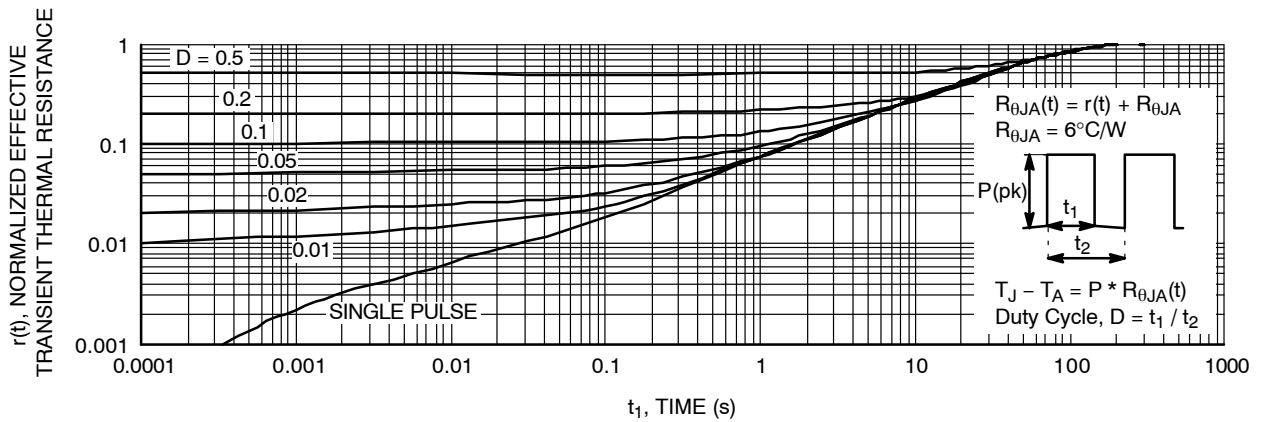


Figure 11. Transient Thermal Response Curve

(Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.)

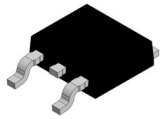
# FDD3680

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping <sup>†</sup>
FDD3680	FDD3680	DPAK3 (TO-252 3 LD)	13"	16 mm	2500 / Tape & Reel

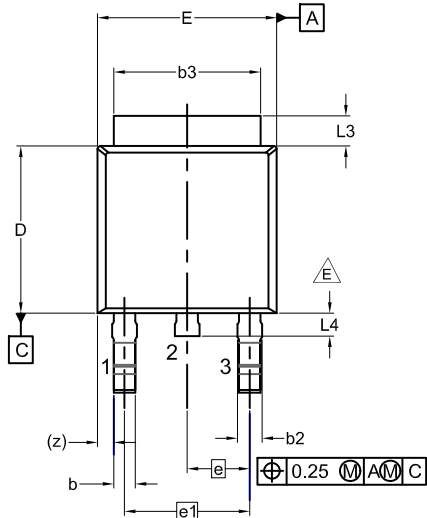
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

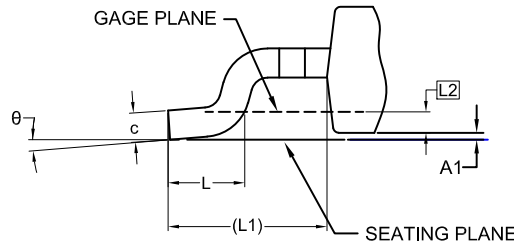


## DPAK3 (TO-252 3 LD) CASE 369AS ISSUE A

DATE 28 SEP 2022

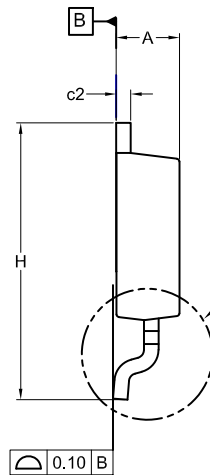
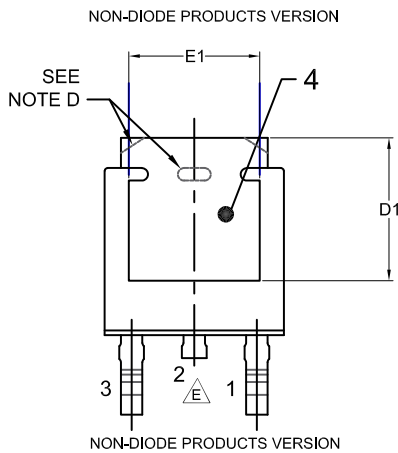


- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.  
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.  
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.  
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.  
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



**DETAIL A**  
(ROTATED -90°)  
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	-	-
E	6.35	6.54	6.73
E1	4.32	-	-
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	-	-	1.02
θ	0°	--	10°

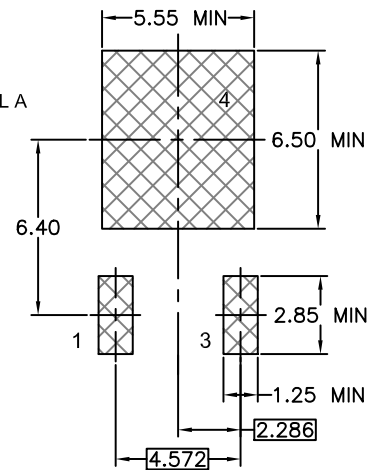


### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



### LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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