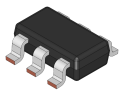
MOSFET – P-Channel, POWERTRENCH®

-20 V, -4 A, 100 mΩ

FDC642P-F085, FDC642P-F085P



TSOT23 6−Lead
CASE 419BL

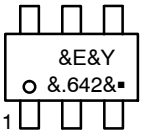
Features

- Typ $R_{DS(on)}$ = 52.5 mΩ at V_{GS} = −4.5 V, I_D = −4 A
- Typ $R_{DS(on)}$ = 75.3 mΩ at V_{GS} = −2.5 V, I_D = −3.2 A
- Fast Switching Speed
- Low Gate Charge (6.9 nC Typical)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- SUPERSOT™ −6 Package: Small Footprint (72% Smaller than Standard SO−8); Low Profile (1 mm Thick)
- AEC−Q101 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

Applications

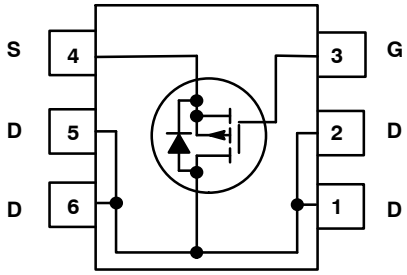
- Load Switch
- Battery Protection
- Power management

MARKING DIAGRAM



XXX = Specific Device Code
&E = Space Designator
&Y = Year of Production
&. = Pin One Identifier
▪ = Pb−Free Package

PINOUT



SUPERSOT™−6

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	−20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current – Continuous (V_{GS} = 4.5 V) – Pulsed	 −4 −20	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	72	mJ
P_D	Power Dissipation	1.2	W
T_J, T_{STG}	Operating and Storage Temperature	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J = 25°C, L = 14.1 mH, I_{AS} = −3.2 A

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	30	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 1in^2 Copper pad Area	103	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	−20	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V	–	–	−1	μA
		V_{DS} = −16 V, V_{GS} = 0 V, T_A = 150°C	–	–	−250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−0.4	−0.7	−1.5	V
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = −4.5 V, I_D = −4 A	–	52.5	65	mΩ
		V_{GS} = −2.5 V, I_D = −3.2 A	–	75.3	100	
		V_{GS} = 4.5 V, I_D = −4 A, T_J = 125°C	–	72.7	105	
g_{FS}	Forward Transconductance	V_{DD} = −5 V, I_D = −4 A	–	10	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = −10 V f = 1 MHz	–	630	–	pF
C_{oss}	Output Capacitance		–	160	–	pF
C_{rss}	Reverse Transfer Capacitance		–	65	–	pF
R_g	Gate Resistance	f = 1 MHz	–	4.4	–	Ω
$Q_{g(TOT)}$	Total Gate Charge at −4.5 V	V_{GS} = 0 V to −4.5 V, V_{DD} = −10 V, I_D = −4 A	–	6.9	9.0	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = −10 V I_D = −4 A	–	1.2	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	1.8	–	nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn−On Time	V_{DD} = −10 V, I_D = −1 A, V_{GS} = −4.5 V, R_{GS} = 6 Ω	–	–	23	ns
$t_{d(on)}$	Turn−On Delay Time		–	7.3	–	ns
t_r	Rise Time		–	5.5	–	ns
$t_{d(off)}$	Turn−Off Delay Time		–	23.2	–	ns
t_f	Fall Time		–	9.6	–	ns
t_{off}	Turn−Off Time		–	–	53	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = −1.3 A	–	–	−1.25	V
		I_{SD} = −0.65 A	–	–	−1.0	
t_{rr}	Reverse Recovery Time	I_{SD} = −1.3 A, dI_{SD}/dt = 100 A/μs	–	17	22	ns
Q_{rr}	Reverse Recovery Charge		–	5.6	7.3	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size†	Tape Width	Quantity
FDC642P	FDC642P−F085	SSOT−6	7”	8 mm	3000 Units
FDC642P	FDC642P−F085P	SSOT−6	7”	8 mm	3000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

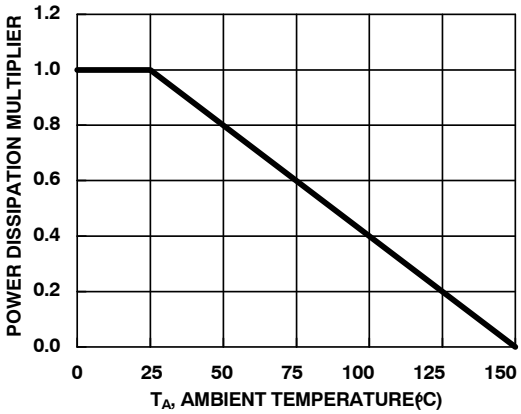


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

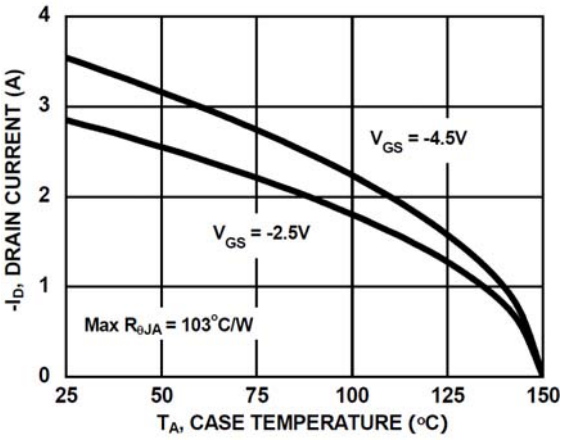


Figure 2. Maximum Continuous Drain Current vs. Ambient Temperature

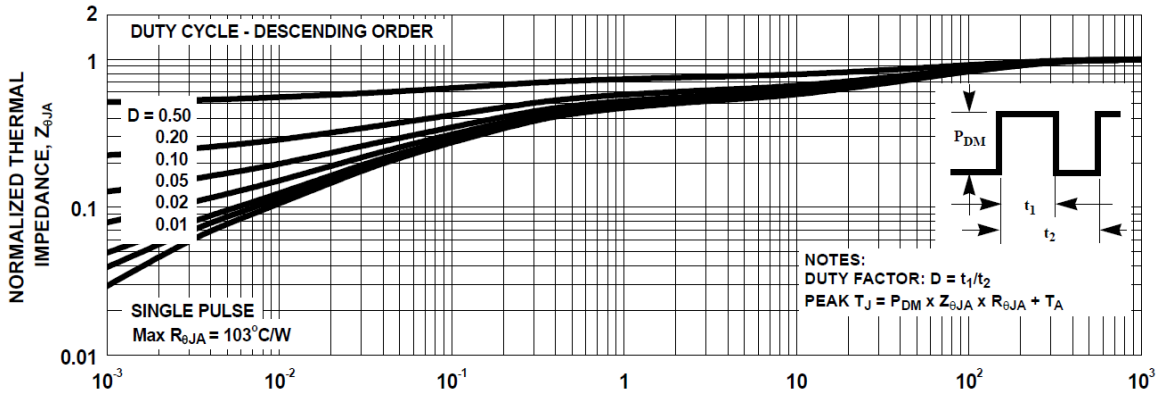


Figure 3. Normalized Maximum Transient Thermal Impedance

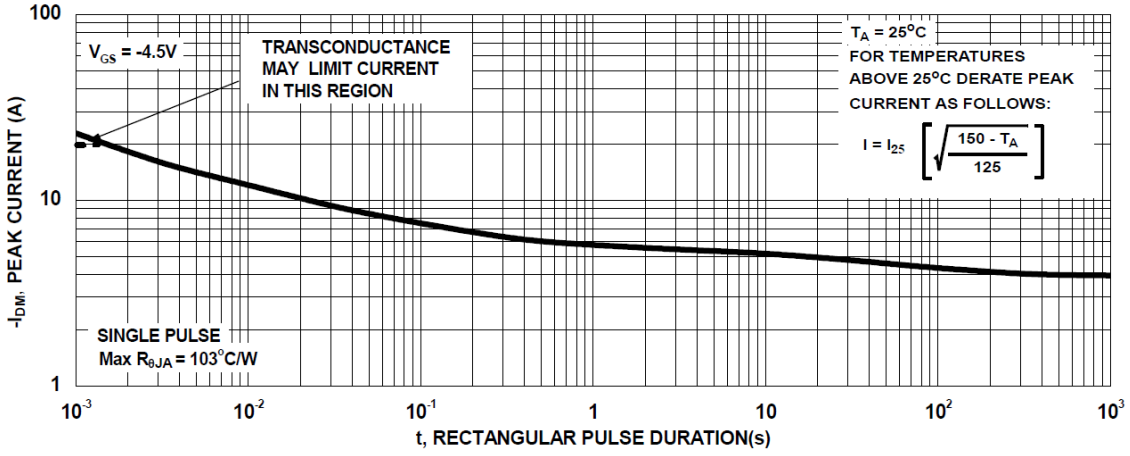


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS continued)

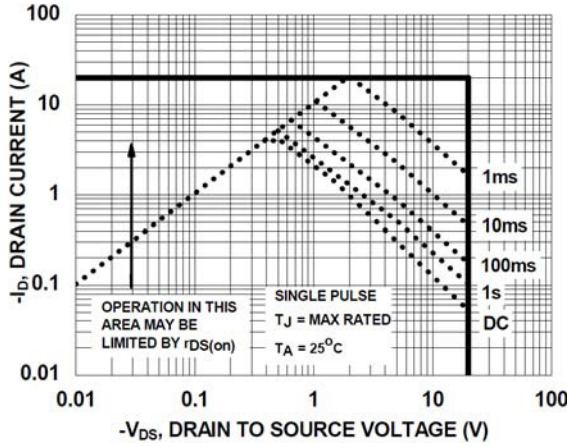


Figure 5. Forward Bias Safe Operating Area

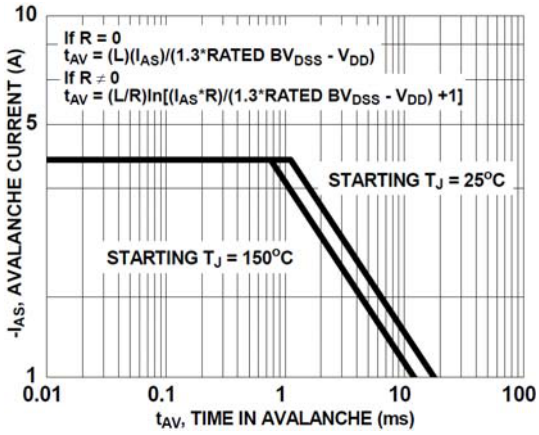


Figure 6. Unclamped Inductive Switching Capability

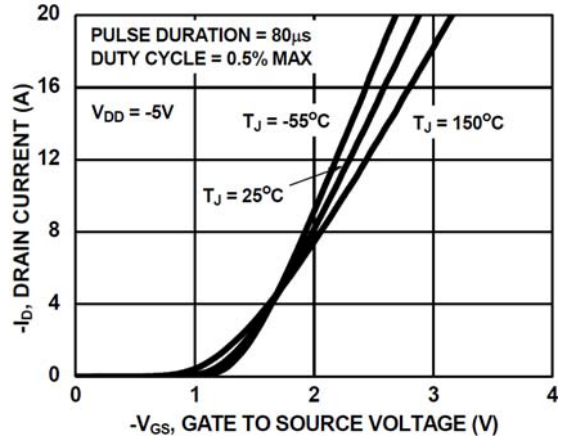


Figure 7. Transfer Characteristics

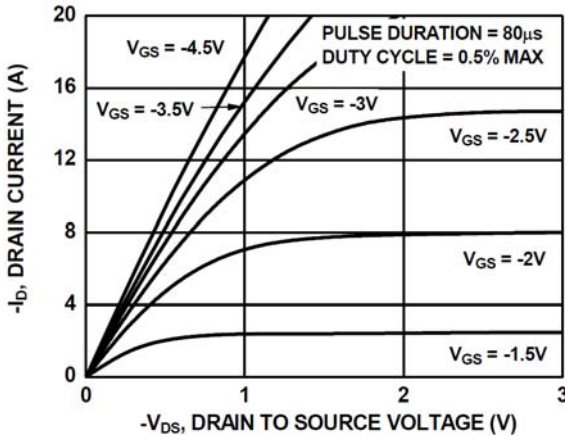


Figure 8. Saturation Characteristics

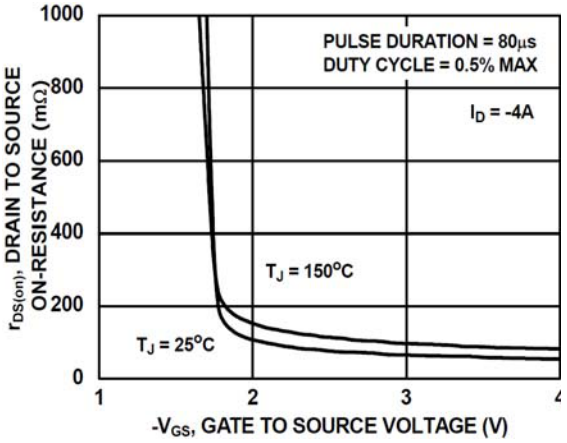


Figure 9. Drain to Source On−Resistance Variation vs. Gate to Source Voltage

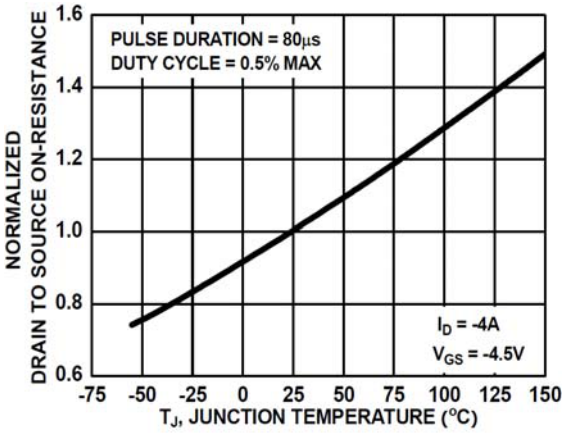


Figure 10. Normalized Drain to Source On−Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS T_J = 25°C unless otherwise noted (continued)

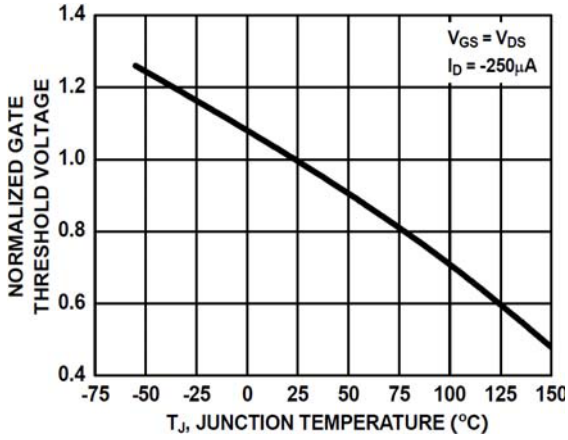


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

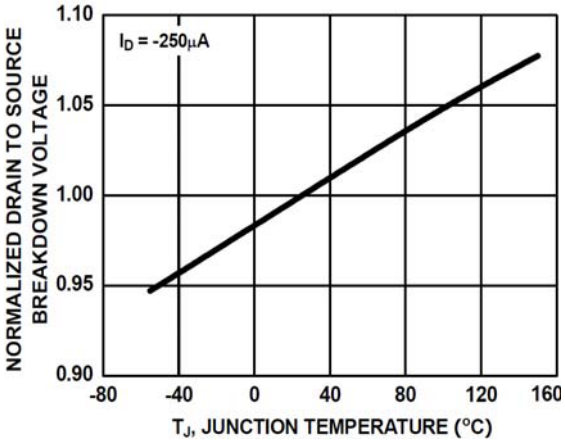


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

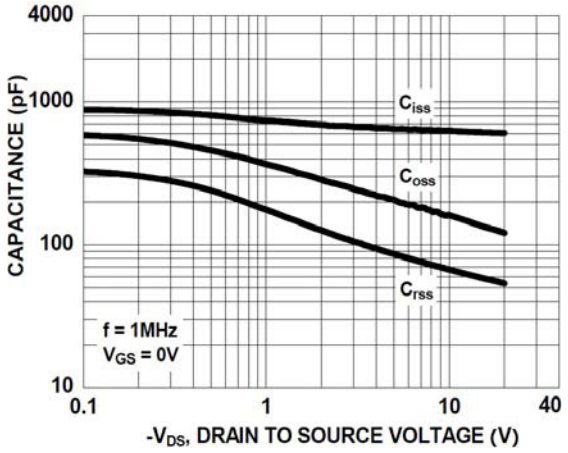


Figure 13. Capacitance vs. Drain to Source Voltage

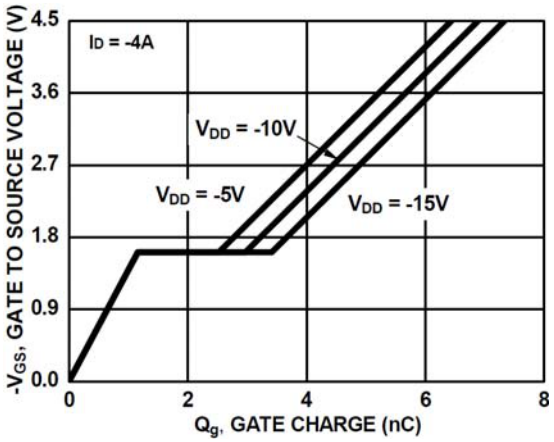


Figure 14. Gate Charge vs. Gate to Source Voltage

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

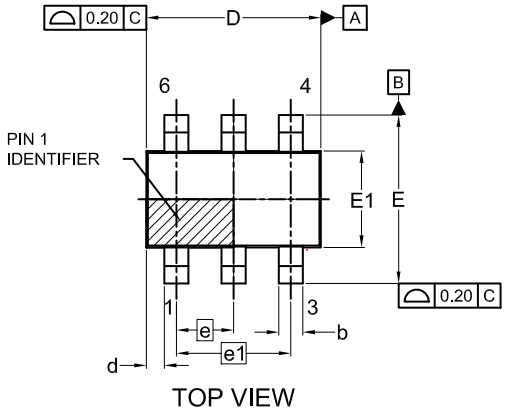
ON Semiconductor®

1

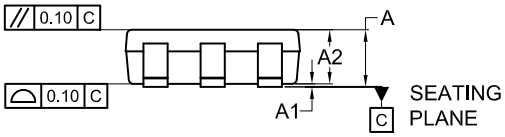
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

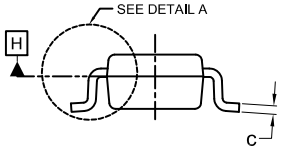


TOP VIEW

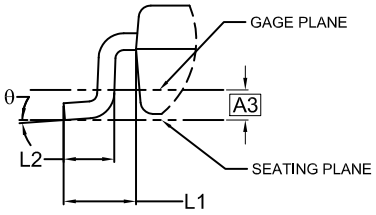


FRONT VIEW

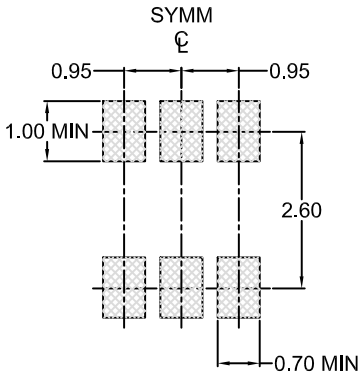
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

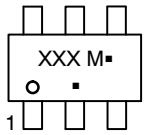
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON83292G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

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